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# [F04] Timepix4 timing performance and first beam test results

*Thursday 27 October 2022 10:00 (30 minutes)*

Timepix4 is the latest generation in the Timepix family of ASICs. It has a pixel matrix of 512 by 448 pixels with a size of 55 by 55 μm, where each individual pixel measures the arrival time of the hits via leading edge discrimination. The TDC is constructed of four phase-shifted 640 MHz clocks to achieve a time bin size of 195 ps and a nominal time resolution of 60 ps. Besides the time of arrival, also the time-over-threshold (ToT) is measured to determine the amount of integrated signal charge. The charge-sensitive amplifier in the front-end has a constant discharge current to establish a linear relationship between the ToT and signal charge. For signals of more than 4000 electrons, the ToT resolution is better than 5%. The ASIC can be tiled on four sides, and can handle a rate of 360 Mhits/cm²/s. The time resolution of both the digital and analog front-end has been determined using lab measurements and will be presented. A beam telescope has been constructed and is in the early stages of operation. Test beam results acquired at the SPS will also be presented.

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