Vertexing and tracking semiconductor detectors for the ILC

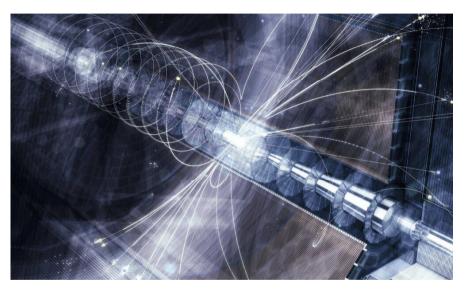
H. Wennlöf on behalf of The ILC Detector Community

27/10 -22

Outline

ilc international linear collider

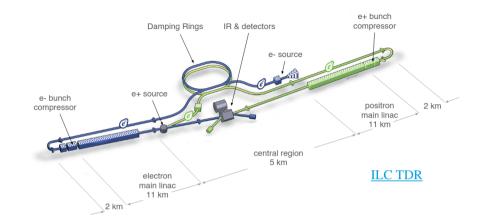
- The International Linear Collider
- ILC detector tracking concepts
 - Challenges and requirements
- Silicon technologies for vertexing and tracking
 - Current and emerging developments
- Tools for R&D
- Detector support and infrastructure
- Summary and conclusions

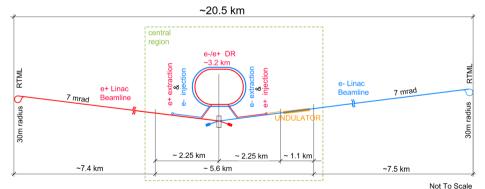


https://linearcollider.org/

The International Linear Collider

- Proposed 20 km long **linear accelerator**, suggested site is Kitakami mountains in Japan
- Initial baseline centre-of-mass energy of **250 GeV**, but upgradeable to 1 TeV
- Colliding **polarised beams** of electrons and positrons
 - 80% e⁻ polarisation, 30% e⁺
- Creates a high-precision complement to the LHC and HL-LHC
 - Well-known initial state
 - Relatively small backgrounds (no QCD)
 - Precise detectors
 - High-luminosity Higgs factory

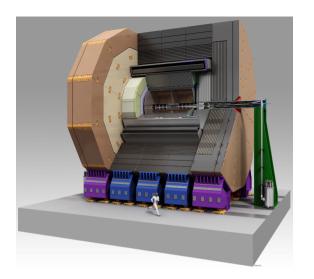




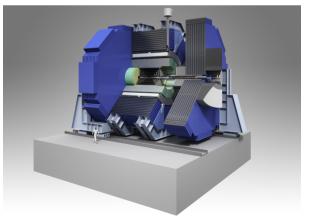
https://arxiv.org/pdf/1903.01629.pdf

Detector concepts

- **Two detectors** envisaged for a single IP, in a push-pull configuration
 - Allows for **complementarity** and result **cross-checking**
- Two main detector concepts; ILD (International Large Detector) and SiD (Silicon Detector)
 - This talk focused on the silicon tracking subsystems of the detectors
- Both based on the "**particle flow**" paradigm optimised combination of tracking and calorimetry
 - Highly segmented detectors and sophisticated reconstruction techniques, of both charged and neutral particles
 - Dedicated fast timing layers in tracker are considered and actively studied, to aid in particle identification
- High magnetic field to improve momentum resolution and get rid of beamstrahlung electrons



ILD concept



SiD concept

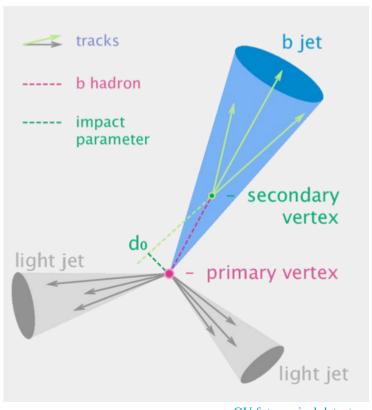
ILC tracking detector requirements

- Precision measurements are demanding on vertexing and tracking detectors
 - Momentum resolution: needs large lever arm, and minimal scattering
 - Vertex position resolution: needs excellent detector resolution, and minimal scattering
 - High **bandwidth** needed to cope with expected data rate;
 O(50-100 MHz/cm²)
- Physics studies for lepton colliders provide requirement guidelines
- Table on the right shows requirements compared to LHC experiment requirements
- Notably: **lower material budget** and **better resolution** required at the ILC, but **radiation is less of an issue**
 - Similar to **heavy-ion experiments** (ALICE, EIC); can benefit from synergies!

	ILC	(HL-)LHC (ALTAS/CMS)
Single-point res.	≤ 3 - 7 µm	5 - 30 μm
Time resolution	~1 ns (SiD), ~1 µs (ILD)	25 ns
Material budget (vertexing)	$\sim 0.15\% \text{ X/X}_0 \text{ per layer} + 0.14\% \text{ X/X}_0 \text{ beampipe}$	10 - 15% X/X ₀ total
Material budget (tracking)	10 - 15% X/X ₀ total	30 - 40% X/X ₀
Min. granularity	< 20 x 20 μm	50 x 50 μm
Radiation tolerance	$< 10^{11} \text{n}_{\text{eq}}/\text{cm}^2 \text{/year}$ O(100 krad/year) TID	$\sim 10^{16} n_{eq} / cm^2$
Power consumption	Average of < 20 mW/cm ²	

Vertexing and flavour tagging

- Pixel detectors at collider experiments are closest to the interaction point
- Crucial for most analyses;
 - Primary vertex reconstruction
 - Low-p_T track reconstruction (< 100 MeV/c)
 - Vertex/jet charge determination
- Useful for **flavour tagging**
 - Identifying quarks (b and c) by locating secondary decay vertices
- Requires **excellent pointing resolution** to resolve impact parameter, and **low material budget** to maintain both pointing and momentum resolution

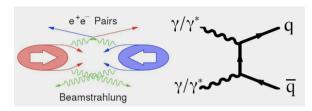


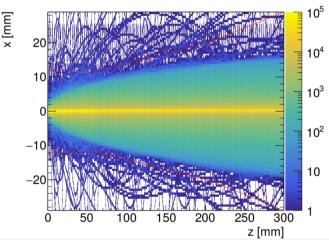
QU future pixel detectors

Beam-induced background and bunch structure

- Running conditions (small beams) lead to "**beamstrahlung**" beam-beam interactions generating e⁺-e⁻-pairs or hadrons
 - Generates significant rate of **background particles**
 - Incoherent e⁺-e⁻-pairs lead to **high vertex detector occupancy**; ~6 hits per cm² per bunch crossing
 - Problem mitigated by high sensor granularity, good time resolution, and/or several storage cells enabling readout during quiet times

- The ILC will operate in **bunch trains**
 - 1312 bunches per train, ~550 ns apart
 - Repetition rate of 5 Hz -> \sim 199 ms between trains
- Low duty cycle: triggerless frame-based readout possible
- Possibility for power-pulsing; switch detector components off between trains to reduce heat dissipation

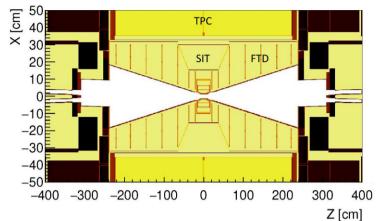




Cone of background from incoherent e⁺e⁻-pairs; https://arxiv.org/pdf/2203.07622.pdf

ILC tracking detector concepts - ILD

- The ILD vertexing and tracking detectors combine silicon (SIT, FTD) and gas-based (TPC) detectors
 - **Silicon detectors** focus of this talk
 - Innermost layers and disks consist of silicon pixel sensors, outer tracker is a time projection chamber
 - Single layer of silicon (strip) detectors covers the outside of the TPC, providing a high-granularity final tracker position, improving momentum resolution
- The ILD solenoidal field will be 3.5 4 T
 - A high magnetic field helps with momentum resolution and rejection of beamstrahlung particles
 - Low-energy e⁺e⁻-pairs spiral within the beampipe
- Requirements for vertexing layers:
 - Single-point resolution < 3 μm
 - Less than $0.15\% \text{ X/X}_0$ per layer
 - Low power consumption to minimise cooling needs

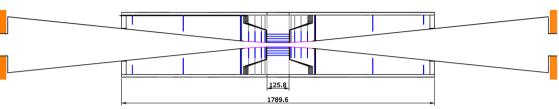


ILD tracker layout; https://arxiv.org/pdf/2003.01116.pdf

- Design of silicon parts:
 - 3 vertexing (double) layers, focused on resolution
 - 2 tracking layers, bridging gap to TPC
 - 7 disks in the forward and backward directions for extended coverage
- Possible silicon technologies:
 - CMOS pixels, DEPFET pixels, Fine-pixel CCD, SOI

ILC tracking detector concepts - SiD vertexing

- The SiD vertexing and tracking detectors are fully silicon-based
- Solenoidal field will be 5 T
- Requirements for vertexing layers:
 - Single-point resolution $< 5 \mu m$
 - Implies a pixel size < 17 μm for single-pixel events, can be larger with charge sharing
 - Less than $0.3\% \text{ X/X}_0$ per layer
 - Power consumption < 20 mW/cm² to allow for air cooling
 - Time-stamp bunch crossings (big difference compared to ILD vertexing)

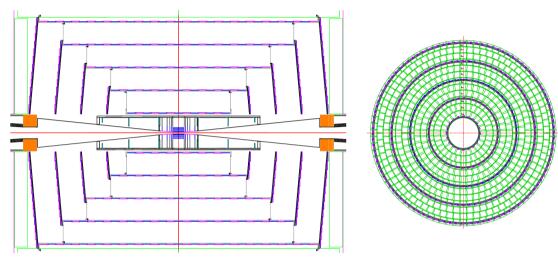


SiD vertexing layer layout; https://arxiv.org/pdf/1306.6329.pdf

- Design of silicon parts:
 - 5 vertexing layers, focused on resolution
 - 4 disks in the forward and backward directions for extended coverage
- Possible silicon technologies:
 - CMOS pixels

ILC tracking detector concepts - SiD tracking

- Requirements for tracking layers:
 - Single-point resolution < 7 μm
 - Less than $15\% \text{ X/X}_0$ total
 - Good momentum resolution
 - Time-stamp bunch crossings
- Design of silicon parts:
 - 5 tracking layers of varying lengths
 - Outermost layer 300 cm long
 - Outermost barrel layer radius 122 cm
 - 4 disks in the forward and backward directions for extended coverage
- Possible silicon technologies:
 - Silicon strip sensors, CMOS pixels
 - Trend towards CMOS pixels everywhere



SiD tracking layer layout; https://arxiv.org/pdf/1306.6329.pdf

- Tracker prototype: the <u>LYCORIS</u> beam telescope at the DESY II test beam facility, based on silicon strip sensors
- Performance expected to improve using CMOS pixels

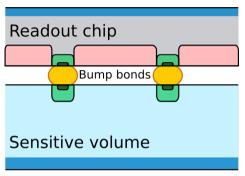
Silicon technologies for vertexing and tracking at the ILC

Note: this is an <u>overview</u> of a few select sensor types; not all developments can be covered in this talk

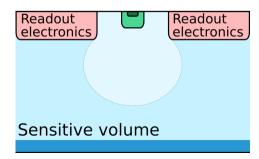
Silicon sensor technologies - broadly

- Two main categories;
 - Hybrid sensors
 - Monolithic sensors
- Hybrid sensors have **physically separated parts**; sensitive volume and readout electronics in separate chips
 - Allows for **separate optimisation** of sensor and readout
 - Parts **bonded together** by e.g. bump bonds
 - Allows extensive on-pixel functionality using mixed-mode CMOS circuits
- Monolithic active pixel sensors (MAPS) combine sensitive volume and readout electronics in a single wafer
 - This enables lower material budget, reduced complexity, and reduced production cost compared to hybrid sensors
 - A low material budget is essential for precise relatively low-energy particle tracking applications
 - Allows less sophisticated readout electronics compared to hybrid sensors (space constraints and transistor type constraints)

Hybrid sensor sketch

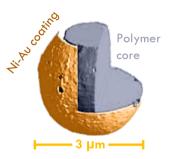


Monolithic sensor sketch

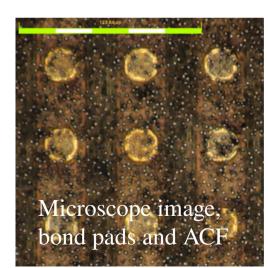


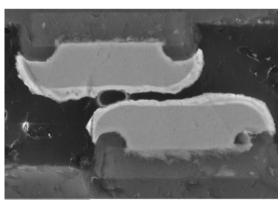
Hybrid sensors using Anisotropic Conductive Film

- Hybrid sensor interconnects limit pixel size bump bonds must make a solid connection but not touch each other
- Anisotropic conductive film (ACF) is a possible workaround
 - Adhesive film with **conductive microparticles**
 - Randomly distributed in film
 - Activated when compressed and deformed under bond pads
- Widely used in display industry
- Testing and R&D for use in particle physics ongoing



Conductive microparticle



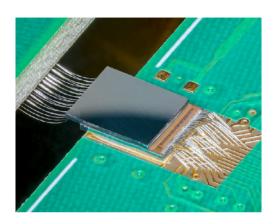


SEM cross-section

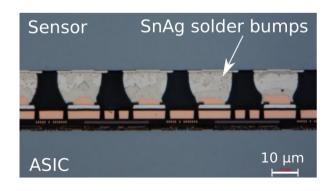
CLICpix2 hybrid prototype

- Pixel readout chip for small pixel pitch and fast time tagging
 - 128x128 pixels, with a $25x25 \mu m^2$ pixel size
 - 65 nm CMOS process
- Developed for use at **linear e**+**e**-**collider experiments**
- Power-pulsing capabilities
- Provides per-pixel charge measurement and time-ofarrival
- Challenge: small-pixel interconnect bonding
 - Low yield with bump bonds, ACF may facilitate
- Challenge: achieving 3 µm resolution with thin sensors
 - Material budget needs to be kept low





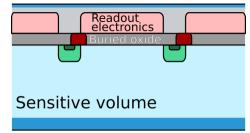
CLICpix2 bump-bonded to sensor



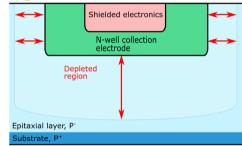
Monolithic sensors

- Three common ways of incorporating full CMOS readout electronics and sensitive volume in a single piece of silicon, while keeping electronics shielded:
- Silicon-on-insulator (SOI)
 - Insulation oxide layer separates sensor and electronics, connected via vias
- Large collection electrode MAPS
 - Readout electronics located in wells **inside** the collection electrode
- Small collection electrode MAPS
 - Utilising a **quadruple-well** technology
 - Readout electronics shielded by deep wells outside the collection electrode
- MAPS advantages: simplified construction, can use commercial CMOS imaging processes (cheaper large-scale production)

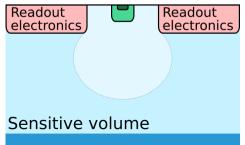
SOI sketch



Large collection electrode sketch

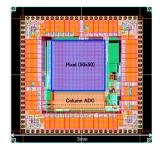


Small collection electrode sketch

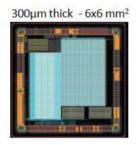


SOI sensors

- Thin and fast, can be fully depleted
- Challenge: complex production process, connecting sensitive volume to readout electronics
- Several SOI developments targeting linear collider experiments, for example
 - **SOFIST** prototypes in LAPIS 200 nm process
 - 20x20 μm² pixel size, demonstrated excellent single-point resolution (~1.3 μm)
 - See talk by A. Ishikawa
 - IPHC and KEK LAPIS **SOI test chip**
 - Complementary developments to SOFIST
 - Double-tier 3D developments at IPHC
 - Cracow SOI test chip in LAPIS 200 nm process
 - 30x30 μm² pixel size, single-point resolution down to ~1.5 μm



SOFIST prototype

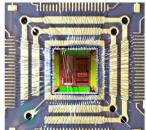


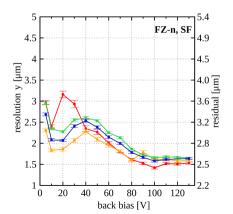


<u>IPHC/KEK</u> SOI test chip, and double-tier 3D developments

<u>Cracow SOI</u> test chip, resolution in y for different clustering methods



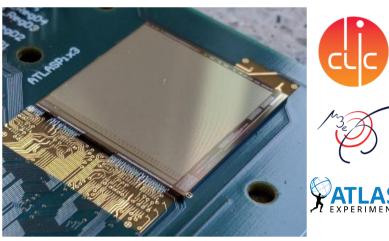


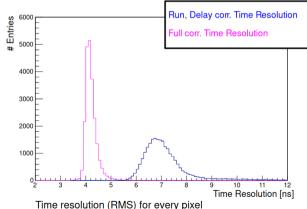


DESY.

Large collection electrode MAPS

- Full CMOS readout electronics inside collection electrode
- Allows high bias voltage
 - Large depleted volume, fast and large signal
- Challenges: large collection electrode leads to
 - Large input **capacitance**
 - Increased power consumption
- Technology used in e.g. the **Mu3e experiment** (MuPix variants)
- Example development: **ATLASpix3**
 - Made in a 180 nm CMOS process, with a pixel pitch of 50x150 μm²
 - Chip size of 2.2x2.0 cm²
 - Power consumption of 140 mW/cm²
 - Time resolution down to ~4 ns



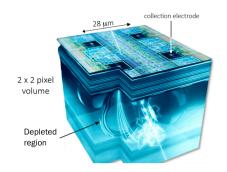


ATLASpix3 results

Uncorrected 6.7ns +- 0.5ns ToT corrected 4.1ns +- 0.1

Small collection electrode MAPS - 180 nm CIS

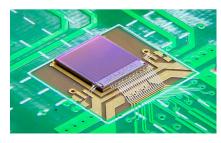
- Many fully-integrated sensors developed in the TowerJazz 180 nm CMOS imaging technology
- **ALPIDE:** Used in the recent ALICE ITS upgrade
 - First large-area MAPS detector at the LHC, pixel size ~29x27 μm²
- **MIMOSIS:** Prototype for the CBM-MVD
 - Targets a 5 μm spatial resolution, 5 μs time resolution, 0.05% X/X₀, 70 MHz/cm² bandwidth (improved w.r.t. ALPIDE)
 - Pixel size 27x30 μm²
 - 4 prototypes planned, the third being submitted around this time
- CLICTD: Targets linear collider developments
 - $-37.5 \times 30 \,\mu\text{m}^2$ pixel size, spatial resolution ~4.5 $\,\mu\text{m}$, time resolution ~5 ns
- **PSIRA** proposal: Targets linear collider developments, specifically ILD vertex
 - Evolution of the MIMOSIS design
- MALTA developments: see talk by <u>H. Pernegger</u>



Artistic view of ALPIDE



The MIMOSIS-1 prototype





CLICTD

Sensor design - optimising signal collection



Fast signal formation and **complete charge collection** crucial for efficiency and time resolution

Deep P-well.

Substrate, P+

shielding electronics

- Requires **depleted** sensor volume
- Layout modifications aid in this; adding a deep planar pn-junction allows for depletion under deep p-wells

N-blanket layout

Further modifications can add **lateral field components** to improve charge collection from edges (note: **reduces charge sharing**)

Blanket layer of n-doped silicon, creating a **deep planar junction**

N-well collection

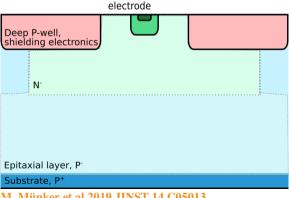
electrode

- Modifications used in several of the developments on the previous slide
- Standard layout

DESY.

- ALPIDE-like
- Incoming particle N-well collection electrode Deep P-well, shielding electronics e/h h/ee/h e/h e/h Epitaxial laver, P Substrate, P+ S. Senyukov et al. doi:10.1016/j.nima.2013.03.017
- W. Snoeys et al. doi:10.1016/j.nima.2017.07.046

- N-gap layout
 - Blanket n-layer with gaps at pixel edges



N-well collection

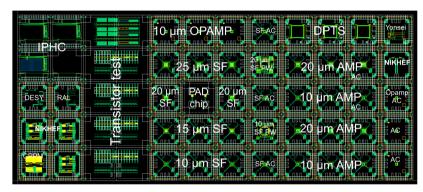
M. Münker et al 2019 JINST 14 C05013

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Increasing logic density: new CMOS technology nodes



- Recently, the **65 nm** CMOS imaging process has become available for use in monolithic sensor developments, building on from the 180 nm developments
- Allows for a **higher logic density**
 - Smaller pixels or more in-pixel functionality
- Allows for **lower overall power consumption**
 - Reduces cooling need
- Allows for larger wafers
 - With **stitching**, this implies **larger sensors**



First monolithic 65 nm submission, MLR1

- Technology envisioned to be used for the next **ALICE inner tracker upgrade** sensor (ITS3), see talks by <u>F. Carnesecchi</u> and <u>P. Becht</u>
- Currently a **multi-institute effort** ongoing in characterising the technology
 - It is so far **unused in particle physics applications**. It is **crucial** to test it
 - First prototypes are available, and second sensor submission recently finalised

DESY.

The Tangerine project (Towards next generation silicon detectors)

- Helmholtz Innovation Pool project, aims to **develop and investigate particle detection** sensors in new silicon technologies
- Work Package 1 of the project, based at DESY, pertains to **monolithic active pixel sensors** in a novel CMOS imaging technology (**65 nm**)
 - The project encompasses all aspects of sensor developments: electronics design, sensor design, prototype test chip characterisation
- The goal is development of a sensor with **high precision and low material**
 - Spatial resolution below 3 μm
 - Time resolution of **less than 10 ns**
 - Very **low material budget**, corresponding to at most 50 μ m of silicon (0.05% X/X₀)
 - Per-pixel charge measurement
- Primary initial goal: development of a sensor for telescope use, for testbeams
 - This will demonstrate the capabilities of the 65 nm technology in a particle physics context
- Longer-term goal: potential usage at e⁺e⁻-collider experiments

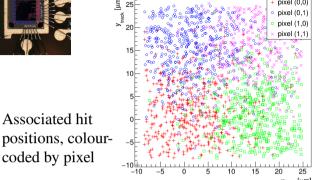


Tangerine project results

- Tangerine MLR1 sensor mainly for testing a newly designed charge-sensitive amplifier
 - Successfully done in labs and at testbeams
- Sensor contains a 2x2 pixel matrix with a pixel size of 16.3x16.3 µm², also investigated at testbeams
- **Second prototype submission** recently done
 - Will investigate a new full in-pixel analogue front-end
 - Larger pixels (25x35 µm²) in the **n-gap layout**, with **varying** gap sizes
- Part of the project is an extensive simulation campaign
 - Using generic doping profiles, a combination of TCAD and Monte Carlo simulations can give accurate predictions of the performance of different sensor layouts and configurations
 - Arrays of sensors have also been simulated, e.g. beam telescopes using future Tangerine sensors



The Tangerine MLR1 prototype

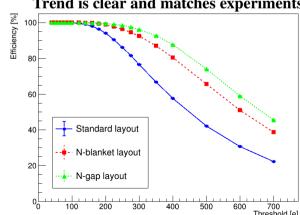


coded by pixel

Associated hit

Simulation of different sensor layouts, showing the efficiency vs threshold.

Trend is clear and matches experiments



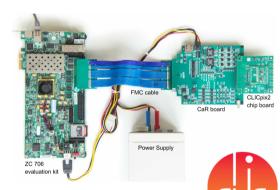
Tools for testing and characterisation used in the community

Tools for testing and characterisation

- Linear collider R&D has helped create many widely-used tools
- Beam telescopes and improvements thereof
- **EUDAQ2** data acquisition framework
- AIDA-2020 Trigger Logic Unit
- Readout systems
 - Caribou; versatile DAQ system, minimising effort of new sensor integration
- Reconstruction software
 - Corryvreckan; flexible and light-weight modular framework for test beam data reconstruction
- Simulation software
 - **Allpix Squared**; modular framework capable of **Monte Carlo** simulations of the **full chain** of signal formation in a semiconductor detector
 - Detailed simulation of **charge carrier propagation** gives realistic signal estimates



EUDET-type beam telescope



Caribou DAQ setup





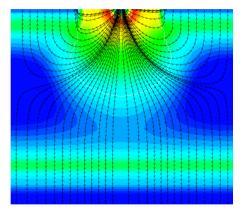
Allpix Squared



Detailed sensor simulations

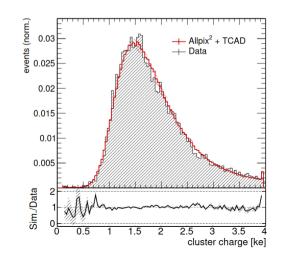
- Electric fields in MAPS are often **highly non-linear**, so detailed simulations are required for understanding them
 - Performed using "technology computer-aided design" (TCAD)
 - Numerically solves Poisson equations using sensor doping information
- **High-statistics Monte Carlo simulations** can be performed using Allpix Squared
 - Simulates **charge deposition** (via interface to Geant4), charge carrier **creation** <u>small collection electrode MAPS</u> and in-sensor **propagation**, and finally **digitisation**
 - Complex geometries are possible, including different pixel shapes and passive material, and simulations are relatively fast
 - Electric fields and doping concentrations can be imported from TCAD
- Together TCAD and Allpix Squared are a **powerful combination**!

 Detailed sensor behaviour and performance can be simulated **accurately** with **high statistics**





Electric field strength and streamlines in TCAD, and comparison of simulation and experiment for small collection electrode MAPS



Developments in detector support and infrastructure

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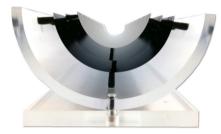
Detector support and infrastructure

ALICE

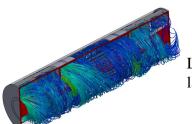
- Vertexing and tracking development is **not only sensors**
 - Material budget needs to be minimised; cooling, cabling, and structural support taken into account
- Forced air-flow cooling very attractive for the ILC
 - No added cooling material, but low power dissipation needed
 - Care needs to be taken to minimise vibrations and direct the air correctly
- Integrated **micro-channel cooling** is an alternative
 - Channels in CMOS sensor substrate, carrying cooling medium
 - Implemented in MALTA variant
- Support structure developments in carbon fiber and carbon foam can be used
 - Recent developments in e.g. Belle II, ALICE ITS, CBM@FAIR useful also for the ILC



- Eliminating majority of material: ALICE ITS3
 - Stitching allows creation of **wafer-scale** sensors
 - Thinning makes silicon **flexible** can bend large sensors around the beampipe
 - Low power allows for air cooling material budget becomes only silicon and local carbon foam support



<u>ALICE ITS3</u> three-layer large-sensor mockup (see talk by <u>L. Lautner</u>)



Linear collider vertexing layers air flow simulation

Summary and conclusions

Summary and conclusions

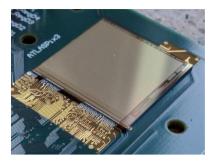
ATLAS EXPERIMENT

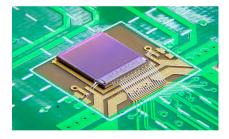






- Silicon detectors at linear colliders have **unique challenges**
 - Ultra-low material budget
 - Low sensor thickness and low power consumption essential
 - High spatial and temporal resolution sensors
- Several design goals are already achieved, but **no current sensor meets all demands simultaneously**
 - This presentation covered a **selection** of developments, not time to cover all of them (3D sensors, DEPFETs, FPCCD, LGADs, ...)
- Trend is towards "pixels everywhere"
 - New hybridisation technologies can overcome hybrid limitations
 - Monolithic sensors in novel CMOS imaging technologies show great promise
- ILC detectors can benefit from synergies with heavy-ion experiments
- Linear collider R&D offers great opportunity to use and develop new technologies
 - R&D of inner tracking systems generic enough to also cover other Higgs factory requirements (e.g. for FCC-ee detectors)







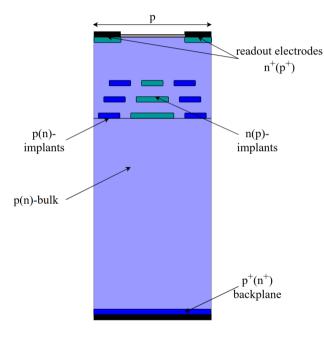
Backup slides



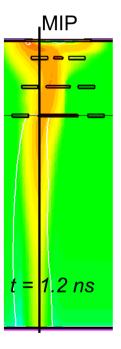


Enhanced Lateral Drift Sensors (ELADs)

- Optimising the sensor part of a hybrid for improved charge collection
- Position resolution without charge sharing limited to pixel pitch / √12
- ELADs aim to **enhance charge sharing** by adding **deep implants** in the sensor
 - Introduces lateral electric fields
 - Shaping the electric field to get linear charge sharing between pixels (theoretical optimum)
- Charge sharing improves position resolution via interpolation
 - Charge-weighted mean position
 - Cluster size of 2 gives optimal resolution
- Challenges: complex production process, and low-field regions have to be avoided



ELAD layout

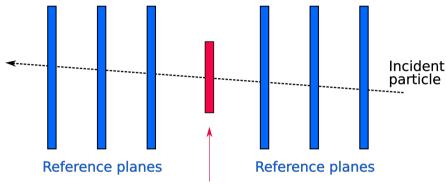


Simulation of the charge cloud of a MIP in an ELAD

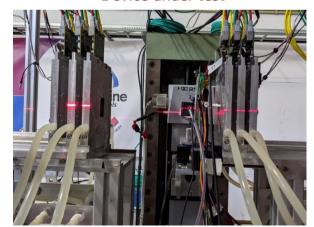
Testbeam setup

- The device under test is surrounded by reference planes (which form a telescope)
- A beam of particles is shot through the reference planes and the device under test
- A reference track is reconstructed by using particle hit data from the reference detector planes

- Device under test placed between reference planes
 - Can thus find particle position at device under test from using the reconstructed track



Device under test

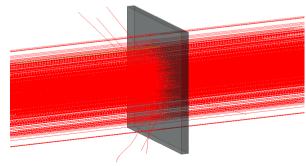


High-statistics Monte Carlo simulations using Allpix²

- Using **Allpix**² to generate incident particles and simulate their energy deposits in a **pixellated sensor model** (via an interface to GEANT4)
 - Each pixel in the sensor model contains the electric fields and doping concentrations from TCAD
- Deposited energy generates electron-hole pairs, and the individual **charge carrier propagation** is simulated
- This finally gives the **charge** per incident particle event that reaches the collection electrode **in each pixel**
- A threshold is then set in simulations, to exclude pixels that would not produce a hit with this threshold level
 - Noise is also added to the signal in this step
- The Monte Carlo truth information is stored along with the simulated per-pixel output, and analysis is performed

- Allpix² allows the simulation of a particle hit to be performed quickly, and thus makes it practical to generate many particles hitting many different sensor positions
 - High-statistics data are obtained
 - Makes it relatively easy to test and compare different configurations and setups
- The framework is well-tested and validated against known data and experiments, e.g. for small collection electrode MAPS sensors:

https://www.sciencedirect.com/science/article/pii/S0168900220303181?via %3Dihub



Particle beam passing through a single sensor, in Allpix²

DESY.