













Development of the radiation hard MALTA CMOS sensor for tracking applications

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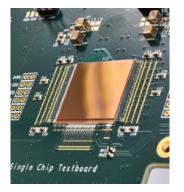
Vertex 2022, October 24-28, 2022, Tateyama, Japan

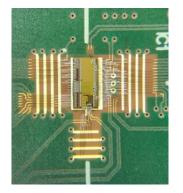


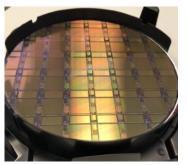
The timeline of MALTA developments

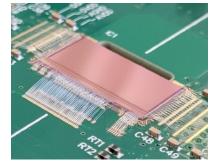
H2020 MSCA ITN "STREAM"

AIDA Innova and CERN EP R&D







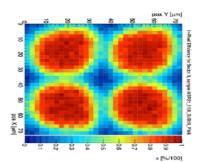


Jan 2021



MALTA1 & MLVL

Jan 2018
Asynchronous readout

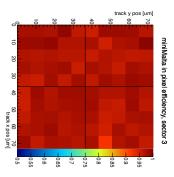


Design optimisation for better lateral field

Mini-MALTA

Jan 2019

Process and mask modification



Full efficiency after 1e15 n/cm²

MALTA C

Aug 2019

Czochralski substrates

Split 7

Oct 2020

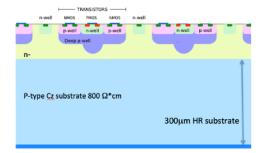
Reduced noise and increased gain

MALTA 2 Mini-MALTA 3

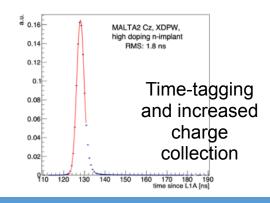
IALIA Z WIIII WALIA

Oct 2022

Data serialization and time tagging



Substrate and process optimisation





The MALTA Sensor and basic specifications

The "MALTA" Sensor

- Asynchronous readout architecture for high hit rate capability with 40bit parallel data bus for hit address and timing readout
- Data streaming for trigger less operation
- Sensor-to-Sensor high-speed signal transmission (no-Flex system integration for minimal X₀)

| 36.4x36.4 μm ² |
|---------------------------------|
| 512x512 /18.3x18mm ² |
| >> 100MHz/cm ² |
| ~2ns |
| >100Mrad |
| $>10^{15} n_{eq}/cm^2$ |
| |

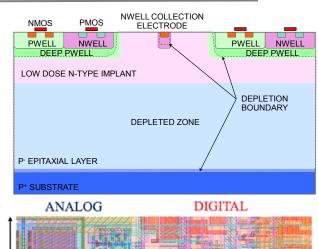


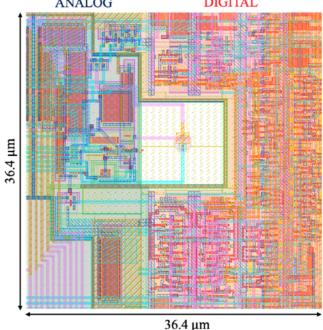
- Developed as radiation hard tracker for HL-LHC application
 - originally developed with specifications for ATLAS ITK Outer layer
 - Radiation hardness for a low noise CMOS sensor is key development goal



The MALTA Pixel design

- Small electrode design 3x3um collection electrode in depleted pixel
 - minimal capacitance (<5fF)
 - Threshold ~100e- and ENC noise < 10e-
- Sensor thickness can be optimised for application
 - epitaxial 30um active in 50um thick sensors for minimal material
 - thicker Cz substrate for larger signal or soft X-ray sensitivity (100 to 300um)
- Sensor Matrix power consumption
 - 1uW/pixel analog
 - 70mW/cm² analog
 - ~10mW/cm² @ 100MHz hit rate (digital power minimised as no clock in matrix)

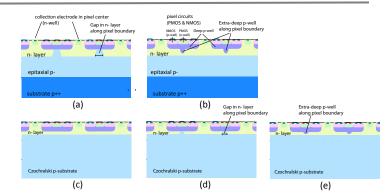




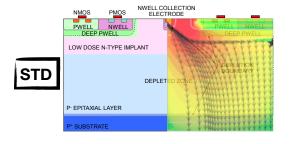


MALTA sensor process (TJ180nm CIS)

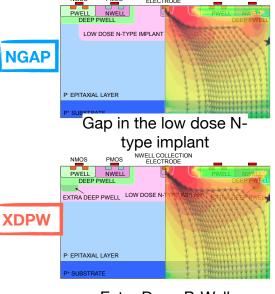
- produced in Tower 180nm CIS process
 - optimisation of implantations with foundry
 - produced on epitaxial and Czochralski substrates



Additional process modifications can increase E-field in pixel corners, further reducing charge collection tails.

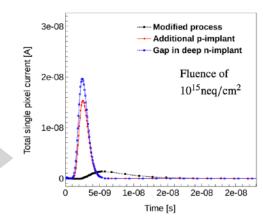


M. Munker, JINST 14 (2019) C05013



NWELL COLLECTION

Extra Deep P-Well

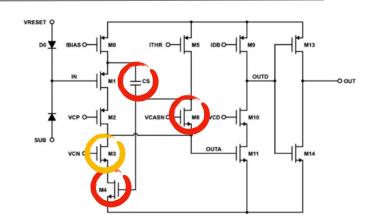


- * faster charge collection
- substantial improvement in radiation hardness due to better charge collection

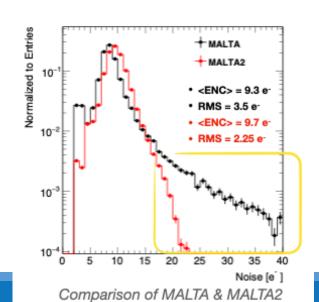


Improved Front-End - MALTA2 sensor

- Same matrix design with asynchronous hit transmission and improved FE:
 - lower noise & higher gain by enlarged transistors & cascode stage
 - enables operating the chip at lower threshold (down to O(100) e-) by significantly reducing noise tail (RTS noise)
 - increases sensitivity to small signal
 - higher radiation tolerance (Ref. <u>JINST 15 (2020) 02</u>):
 with same configuration MALTA1 FE threshold = 340
 el. c.f. MALTA2 FE = 200 el.
 - substantially improves efficiency @ 1x10¹⁵ n_{eq}/cm²:
 MALTA1 FE=87%, MALTA2 FE =98%



<u>IEEE Trans. Nucl. Sci.</u>, vol. 69, no. 6, pp. 1299-1309, June 2022



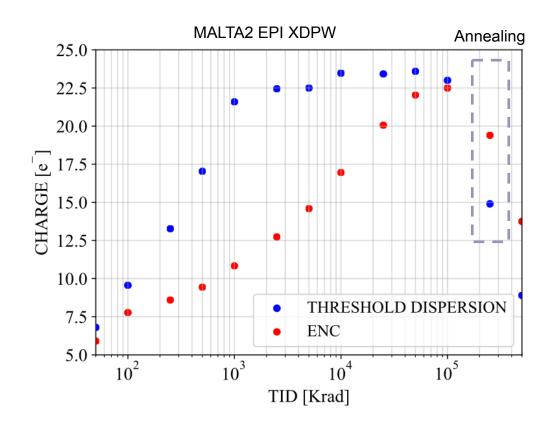
at compatible threshold (~340 e-)



Front-end performance before/after TID 100Mrad

- MALTA 2 sensor irradiated with X-ray to 100Mrad
 - characterise FE threshold and noise through threshold scans

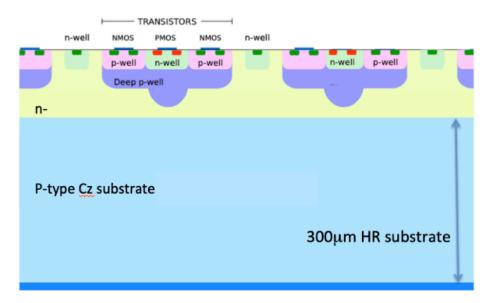
- threshold dispersion
 - starts at ~ 7e- and increases until 10Mrad, then saturates ~22e-
- ENC
 - starts at ~ 6e- and increases to ~22e-
- 24h@R/T Annealing reduces threshold dispersion and ENC





Substrate choice: MALTA sensor on Czochralski p-type

- Possibility of processing on high resistivity Czochralski substrate
 - p-type Cz substrates with resistivity of >4 kΩ·cm
 - Can operate at 50V reverse bias for larger depletion (~100um)
 - Aim for higher radiation hardness
- Implement the same design and process modifications
 - Continuous n-layer (standard), gap in the n-layer (n-gap), extra deep p-well
- To deplete large fraction of HR substrate: need to separate p-well from p-type substrate
 - influenced by n-layer doping as well as details of NGAP width of XDPW implant width & doping depth
 - Have optimised in TCAD and with foundry process experts

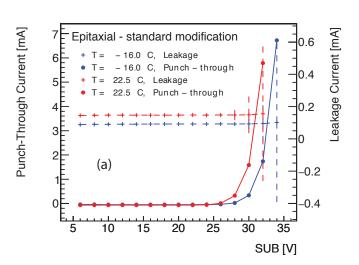


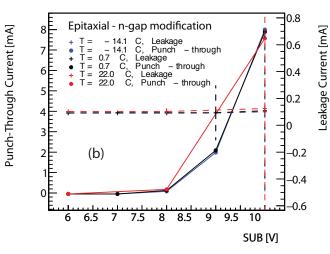
H. Pernegger, NIM A 986 (2021) 164381

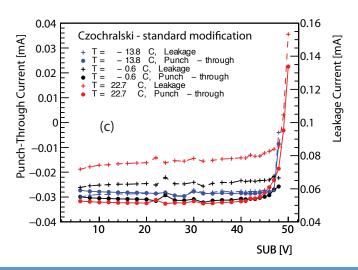


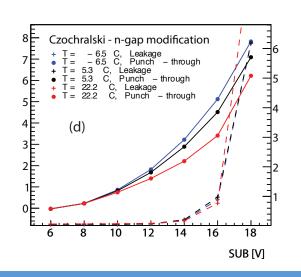
Substrate bias voltage: Epitaxial & Czochralski

- Measured
 punch-through
 on MALTA1 on
 HR Cz substrate
- before irradiation
- continuous nlayer well separates the pwell from psubstrate
- NGAP/XDPW reduce possible substrate voltage









Leakage Current [mA]



Punch-Through Current [mA]

Substrate bias voltage: Epitaxial & Czochralski

- After irradiation (1e15 neutrons/cm2)
- Separation between p-well and substrate improves
- Large operation voltages (~50V) are also possible with NGAP/ XDPW which improves depletion and charge collection after irradiation

Cz continuous n-layer epitaxial N-gap n-layer Cz N-gap Punch-Through Current [mA] Punch-Through Current [mA] Punch-Through Current [mA] T= -16.1C Leakage = -15.3C Leakage T= -16.1C Punch through T= -6.7C Leakage T= -15.3C Punch through T= -6.7C Punch through Epitaxial - n-gap modification Czochralski - standard modificatior Czochralski - n-gap modification irradiated 1015n/cm2 irradiated 1015n/cm2 irradiated 1015n/cm2 (b) (c) 0.26 20 30 40 50 SUB [V] SUB [V] SUB [V]

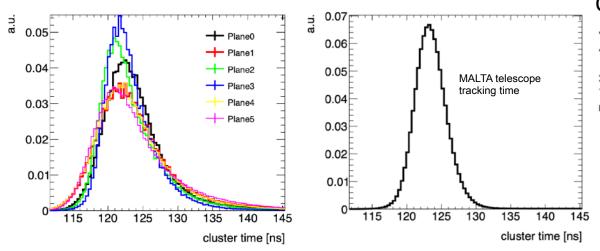


eakage Current [mA

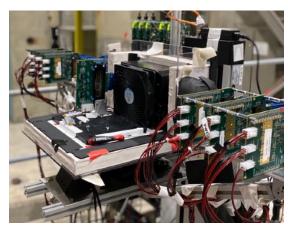
MALTA Testbeam Telescopes & Beam tests

- Custom MALTA telescope with fast read-out, online monitoring, and cold box for irradiated samples
 - Up to 7 planes + DUT or 6 planes + 2 DUT
 - Triggering directly out of MALTA planes
 - Scintillator for better time reference
 - Continuous operation in 2021 and 2022
- Track reconstruction better than 6 um position and ~2 ns timing

Cluster arrival time in different planes:

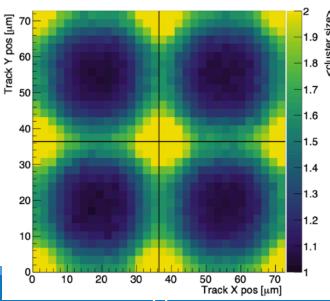


M. Van Rijnbach BTTB 2022



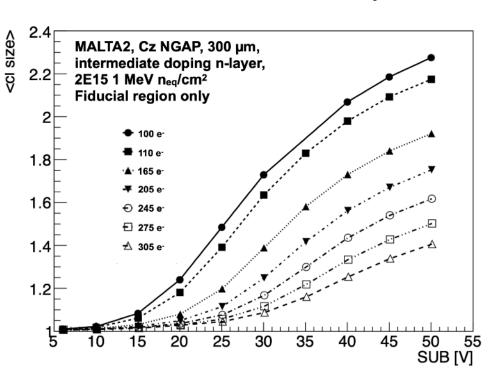
MALTA telescope at SPS

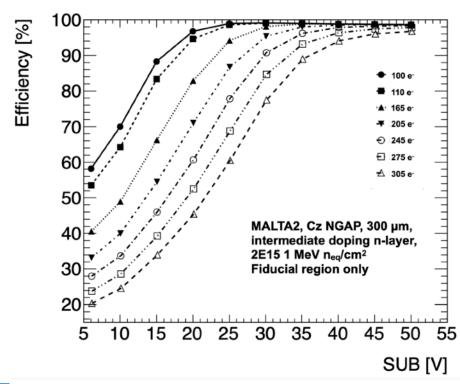
Cluster size versus hit position (Cz)



NIEL Irradiated MALTA2 sensors

- Good performance of Cz samples at 2x10¹⁵ n/cm²
- Sensor back with conductive glue to PCB for more uniform substrate biasing
- Cluster size increases with substrate voltage
 - Maximum at ~2.2 at 50 V at 100 e-
- After 2x10¹⁵ n/cm² efficiency better than 98% at 50 V bias at threshold = 100 e-



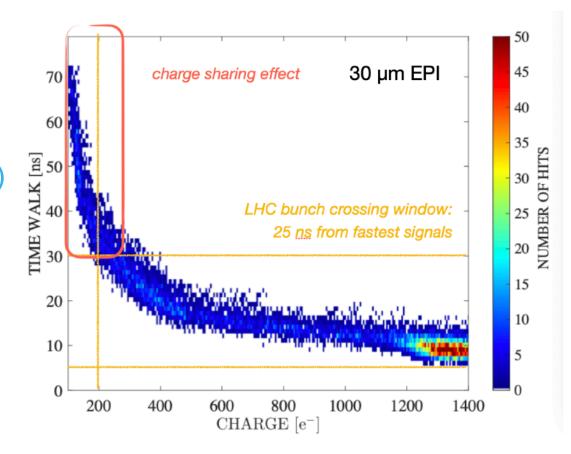




Timing properties of MALTA2 sensor FE

FE time-walk measured on special pixels with analog output

- Sensor measured with 90Sr source
- 90% of hits (not clusters!) arrive within 25ns
 - late hits are small hits from shared clusters
- In-time threshold ~ 200e-



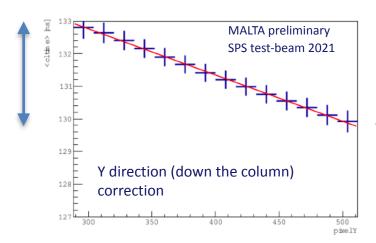
IEEE Trans. Nucl. Sci., vol. 69, no. 6, pp. 1299-1309, June 2022



Timing properties of MALTA2 matrix

Signals discriminated in pixel and transmitted through pixel logic

down column to periphery



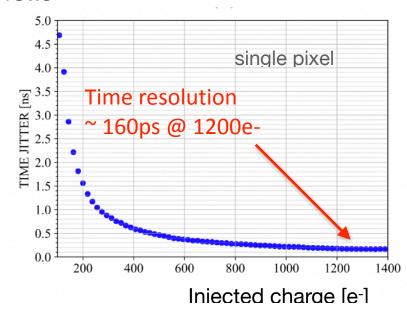
sensor pixel circuit

... periphery

column propagation time

~3ns for 224 rows

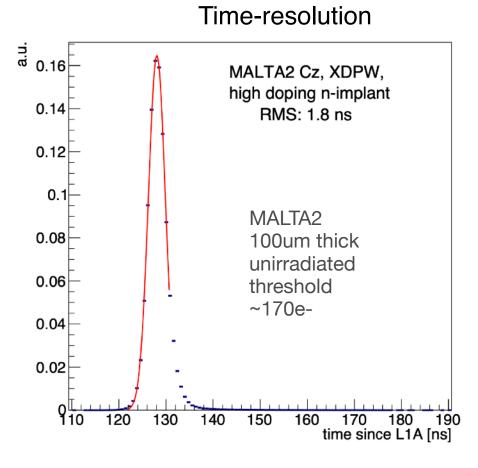
- Measure Time resolution with injected pulses
 - Total jitter from FE to DAQ is dominated by FE
 - Jitter varies from 4.7ns @ 100e- to 160ps @>1200e-
 - Uniform across the chips





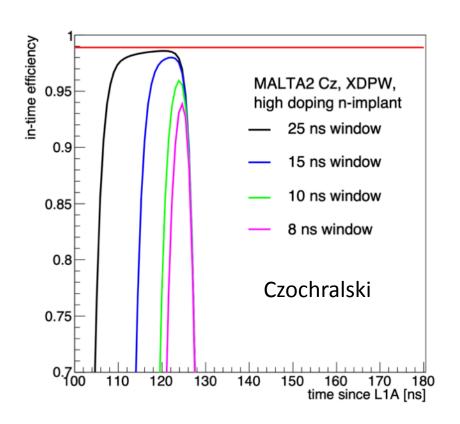
MALTA2 Time resolution in beam tests

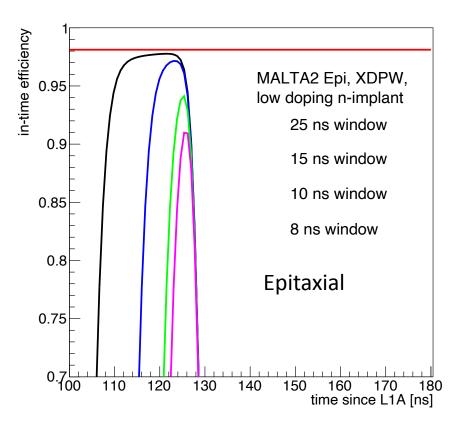
- Time of arrival of leading hit in the cluster w.r.t. scintillator reference
 - Included scintillator jitter:
 0.5 ns
 - Signal latching at FPGA:3.125/sqrt(12) = 0.9 ns
- Timing resolution integrated on full chip 1.8 ns r.m.s. including above system contribution
- Time resolution unfolded ~
 1.45 ns
 - propagation along column corrected





MALTA2 In-time efficiency in beam tests

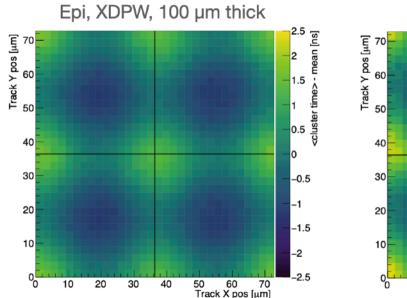


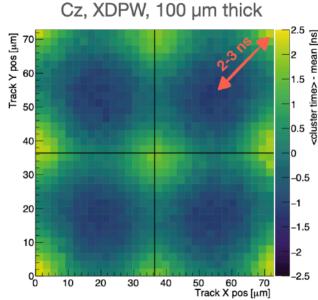


- In-time efficiency 98% in 25ns (LHC) time window & 95% in 10ns time window
- Better in-time efficiency on Cz substrates (higher signal amplitude)



MALTA2 Timing versus hit position in pixel



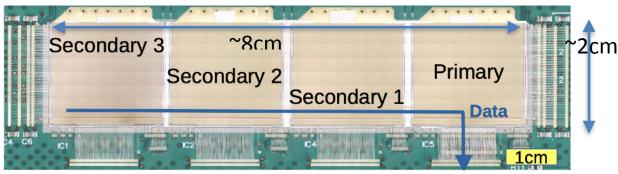


- Induced current signal from hits under deep-p-well in pixel corner is delayed by ~2ns wrt hits close to the electrode
 - this is due to the very non-uniform weighting field in small electrode pixel designs and their drift field & velocity
 - This has been confirmed by simulation (TCAD, Weightfield2 with MALTA doping profiles)
- FE Time-walk adds to this due to smaller signals in pixel corners due to charge sharing



MALTA Modules with multiple sensors

- Develop module concepts for the MALTA sensor as part of EP RD WP 1.3
 - low material budget assemblies
 - direct signal transmission from sensor to sensor

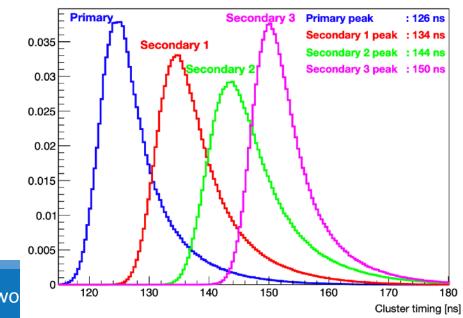


F. Dachs / Elba 2022

Testbeam with 4-chip module:

Cluster time for hits in chips

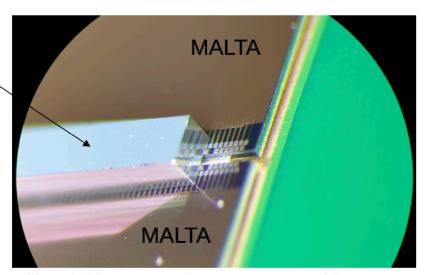
- Built modules with up to 4 sensors, tested in Lab and beam tests
- Daisy chain data of several sensors into single output
- Chip to chip readout works: hit address & timing information transmits well to primary and DAQ





MALTA Module assemblies with silicon bridges

- No wire bonds use silicon bridges to interconnect signal and power
- Bridges are produced in same TJ180nm process and can include active components like regulators (sensor powering) or amplifiers/ buffers (signal transmission)
- A flip chip process is used to place a silicon interposer (silicon bridge) between adjacent MALTA chips for data and power transfer
- Silicon bridge processed as part of the engineering run
 - Potential to adapt design to use silicon bridge for:
 - Logic
 - Additional Power delivery
- Interconnection is realized using Anisotropic conductive film (ACF)
 - J. Weick / TWEPP 2022



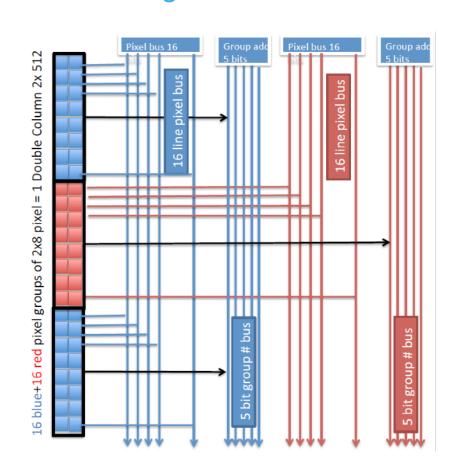
Silicon bridge connection two MALTA 1 chips





Outlook: MALTA3 with integrated hit time tagging

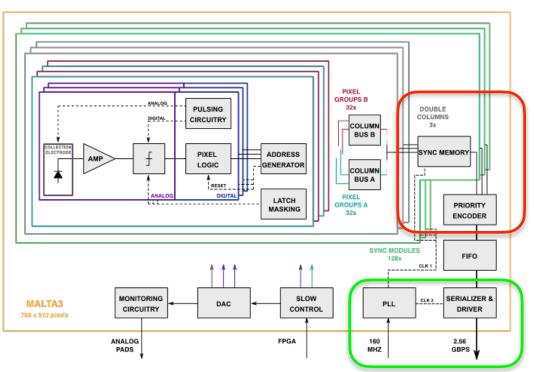
- MALTA matrix is based on asynchronous signal transmission
- Hits are stored using in-pixel flip-flops and transmitted asynchronously over high-speed buses to the endof-column logic (digital periphery)
- No clock distribution over the active matrix to reduce power consumption and maintain hit-time information
- For MALTA1 and MALTA2 the signals are aggregated on 40bit parallel bus
- Time stamping is currently done in FPGA





Outlook: MALTA3 with integrated hit time tagging

- Integrate time-stamping and data serialiser directly on sensor in periphery
- Developed in same TJ180 process as MPW chip (submission 2023)
- Modular 24-column block design to scale to desired sensors matrix size up to fullreticle size (2x3 cm)
- Improved timing reference pulse and masking
- Time-stamping of signals on-chip
- Time-stamping logic@ 1.28GHz
- Serialized highspeed output



Block diagram of MALTA3

STFC "Precise" chip (PLL & serialiser already demonstrated on silicon)

synchronisation memory & readout logic

New for MALTA3 5-bit fine time

D. Dobrijevic TWEPP 2022



LHCb UPGRADE 2 - Upstream Tracker upgrade



 LHCb plans to upgrade its Upstream Tracker and Mighty Tracker with MAPS (LV-CMOS and HV-CMOS)

• MALTA is consider as LV-CMOS candidate for the Upstream Tracker

given the UT requirements:

- NIEL 0.5 to 3 x10¹⁵ n/cm²
- desired time resolution < 3 ns
- required pixel size < 50x150um

 high rate capability and data stream of MALTA as trigger input



- S. Panebianco / Saclay
- J. Wang / Syracuse

ECAL



CERN/LHCC 2021-012

Summary

- The MALTA sensor is being developed as radiation hard monolithic CMOS sensors for future trackers
 - The MALTA sensor is based on small electrode pixels and a trigger less asynchronous readout architecture
 - We have achieved 98% efficiency after 2x10¹⁵ n/cm² NIEL irradiation and good FE performance after 100Mrad
 - The MALTA sensors allows time-tagging of clusters with a time resolution of 1.8 ns for trackers in 40MHz to 100MHz bunch crossing experiments
- Develop multi-sensor MALTA Modules with new assembly techniques aiming at low-mass implementation and high data rate
- For MALTA3 implement on-sensor time-tagging and data serialisation to enable system integration for asynchronous matrix readout in future experiments

