# R&D status of monolithic SOI pixel sensor for vertex detector

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On behalf of the SOIPIX collaboration

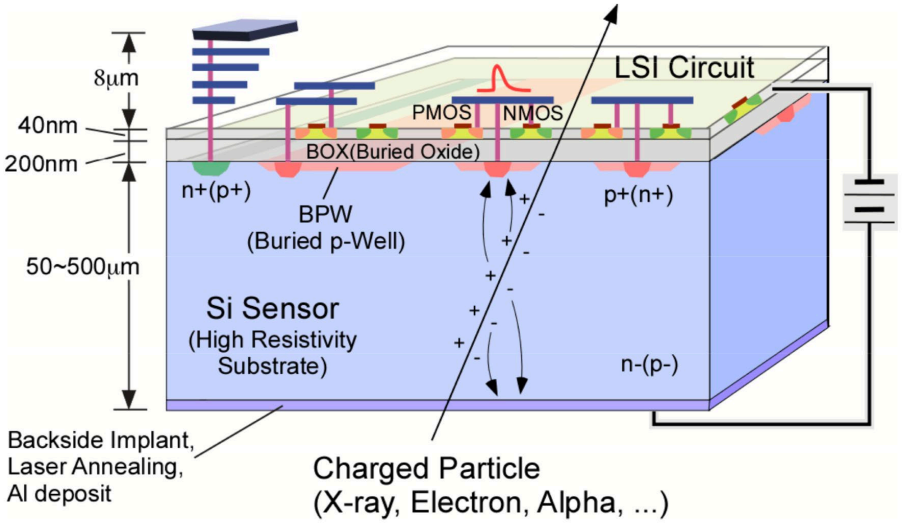
SOIPIX
Silicon-On-Insulator Pixel Detector Project

24th-28th October
VERTEX 2022
Tateyama Resort Hotel, Japan

科研費
KAKENHI

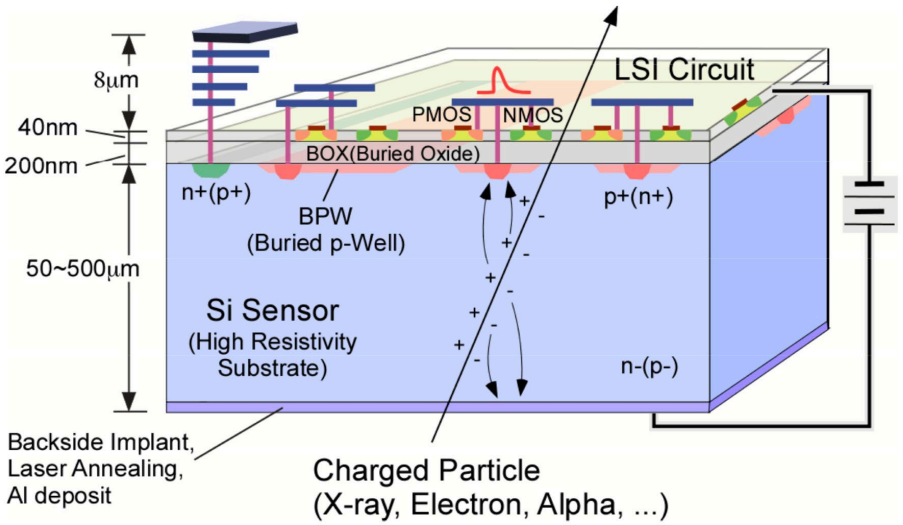
# Silicon on Insulator Pixel Detector (SOIPIX)

- SOIPIX
  - $SiO_2$ BOX insulator layer is sandwiched between CMOS circuit layer and high resistive silicon substrate layer
  - High resistive silicon substrate layer is a good radiation sensor
  - Complicated high density circuit can be fabricated since circuit layer is isolated from sensor layer.
  - Circuit layer and sensor layer are connected with through-silicon Vias.



# Silicon on Insulator Pixel Detector (SOIPIX)

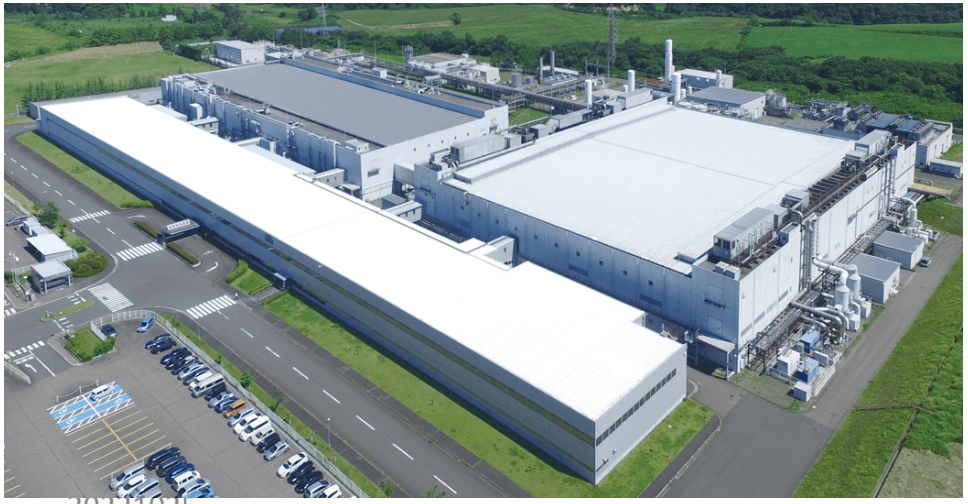
- SOIPIX
  - Fast
  - Small parasitic capacitance
  - Low power consumption
  - Complicated circuit can be fabricated in a pixel
- Suitable for high energy physics application



# Lapis Semiconductor

- 0.2um Low Leakage Fully Depleted SOI CMOS
- We have been collaborating with them since 2005.
  - 20km from Tohoku Univ to Miyagi factory
  - Many Pixel sensors are developed
    - SOPHIAS, XRPIX, PIXOR, CNTPIX, FPIX etc
    - X-ray, IR, particle physics, stress test

Production line is fully controlled with Robots. Good for production of small quantity and also for HEP level mass production.



# Lapis 0.2um FD-SOI Pixel Process

| | |
|---|---|
| Process | 0.2 μm Low-Leakage Fully-Depleted SOI CMOS<br>1 Poly, 5 Metal layers.<br>MIM Capacitor (1.5 fF/um$^2$), DMOS<br>Core (I/O) Voltage = 1.8 (3.3) V |
| SOI wafer (single) | Diameter: 200 mmϕ, 720 μm thick<br>Top Si : Cz, ~10 Ω-cm, p-type, ~40 nm thick<br>Buried Oxide: 200 nm thick<br>Handle wafer: Cz (n) ~700 Ω-cm,<br>FZ(n) > 2k Ω-cm, FZ(p) ~ 7 k Ω-cm etc. |
| Backside process | Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating |

# Closer look at the SOI structure

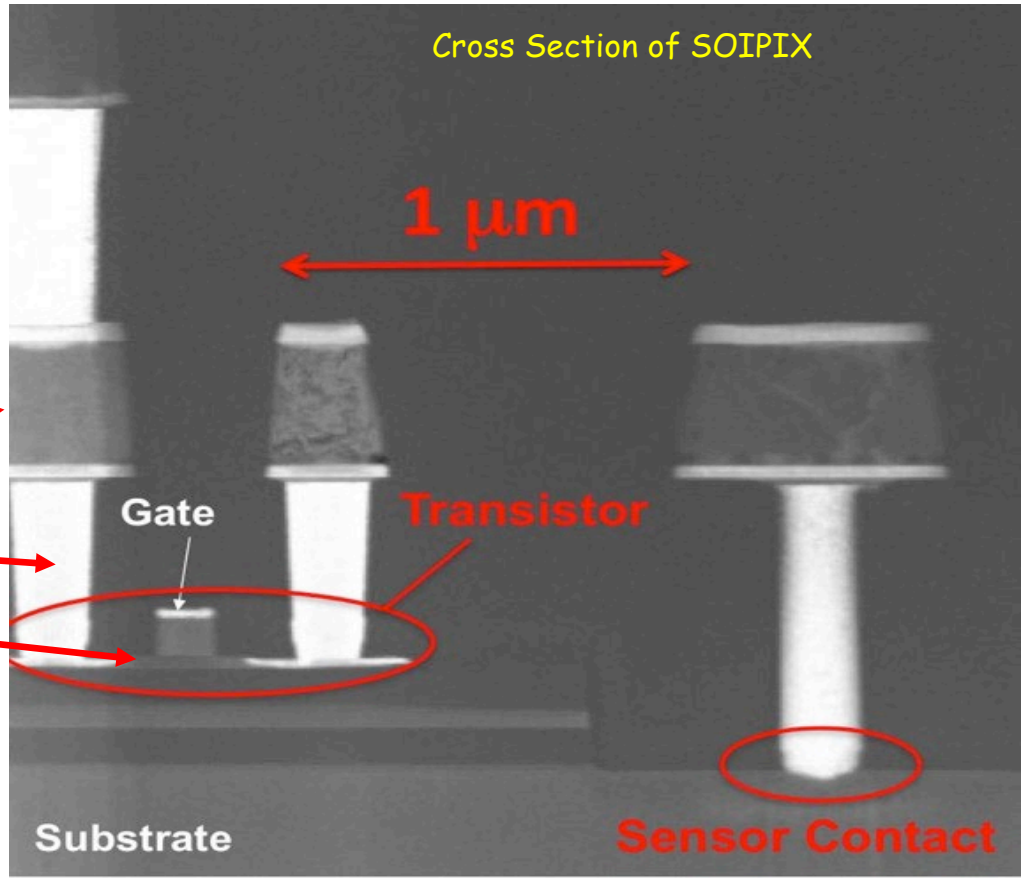
Aluminum metal layer

Tungsten Plugs

Transistor (40 nm thick Silicon)

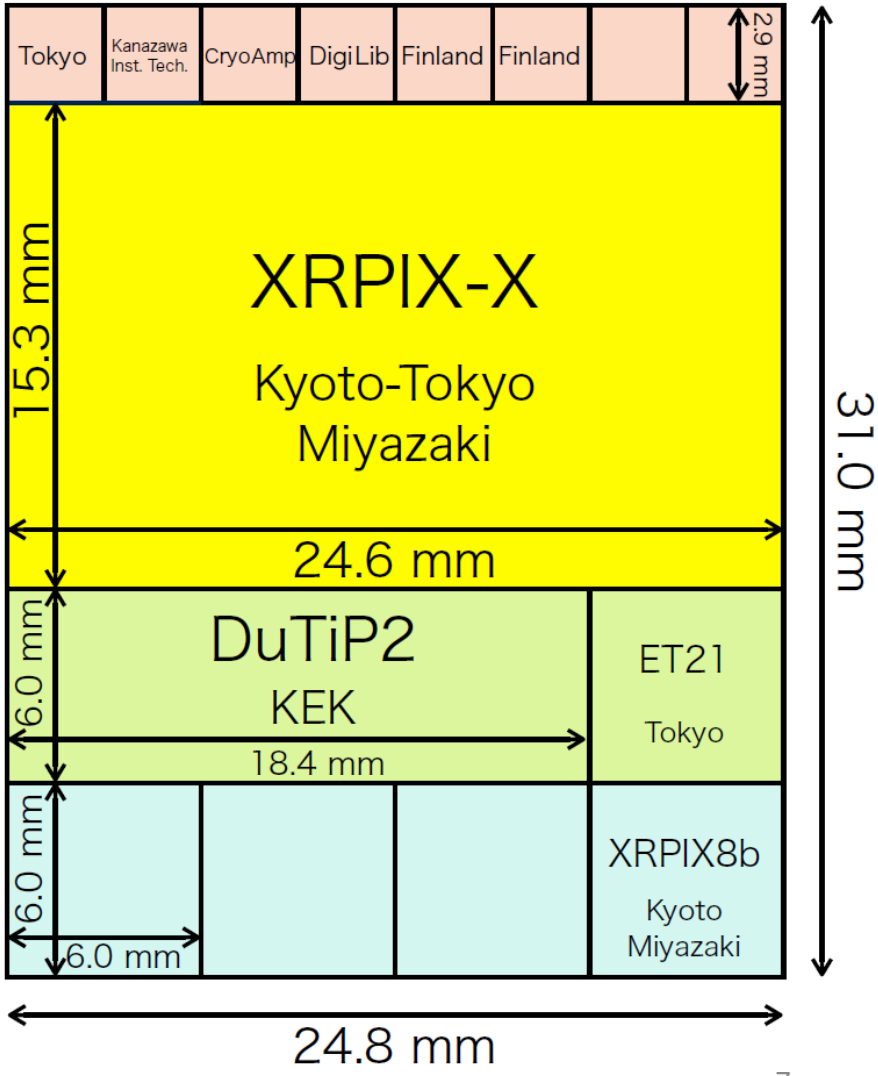
$SiO_2$ layer (140-200 nm)

Substrate (Sensor Silicon)



# MPW Runs

- About once per year, KEK holds a Multi-Project Wafer (MPW) run.
  - Multi-sensors in a single set of reticle.
- Last time, 15 projects joined the MPW run.
  - KEK, Japanese Universities, Companies, Finland.
- If you want to submit your chip to the MPW run, please contact Arai-san



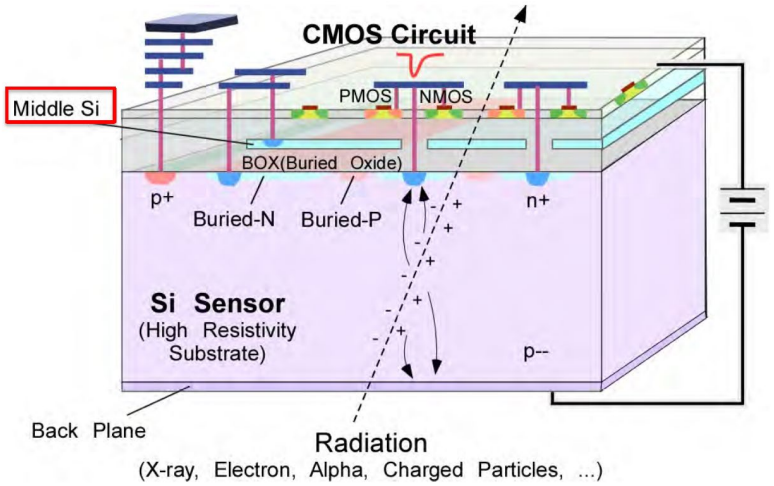
# Developments

- Recent or Important Developments
  - Double SOI – TID tolerance
  - 3D integration – Pixel size reduction keeping circuit functionality
  - Active Merge – Circuit area reduction
  - Digital Library and Automatic Routing – common tools
  - Stitching – Bigger sensors

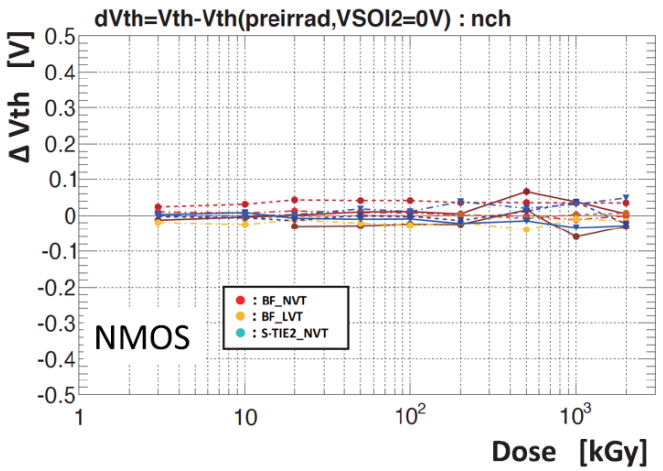
T-Micro
Advanced 3D-IC & MEMS Technologies

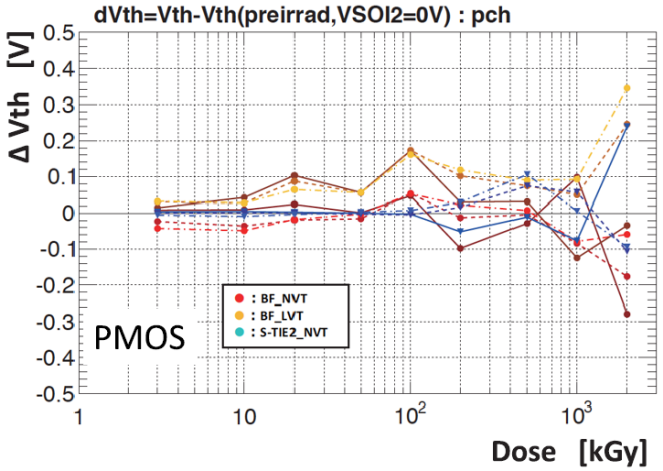
# Double SOI

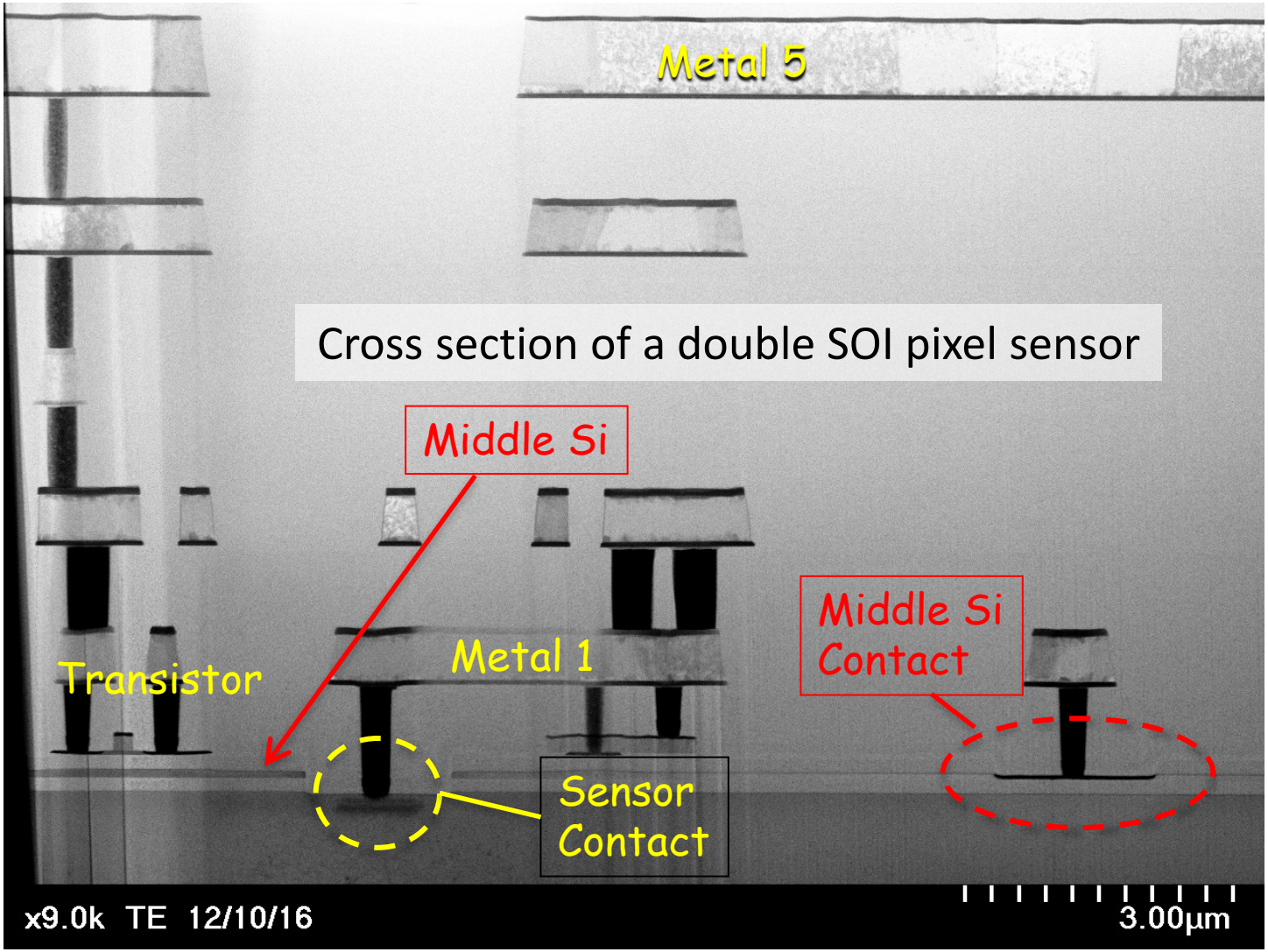
- TID
  - Holes trapped by BOX generate E-field affects the circuit
- compensated by Double SOI
  - Additional silicon layer in BOX layer.
  - LV applied to the layer compensates the E-field generated by holes
  - Upto 2MGy was tested with transistor TEG.




Kazuhiko Hara et al, PoS(Vertex2014)033

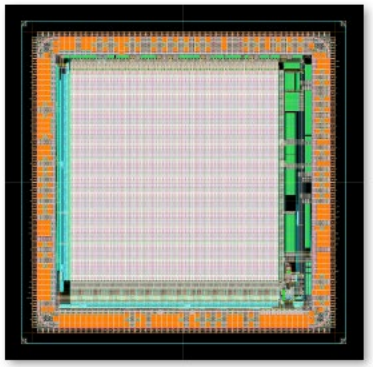



Metal 5
Cross section of a double SOI pixel sensor
Middle Si
Middle Si
Contact
Transistor
Metal 1
Sensor
Contact
x9.0k TE 12/10/16
3.00µm

# 3D Integration

SOFIST3



- SOFIST3 for ILC Vertex
  - Pixel size requirement 20um
  - Real size 30um
- Need to reduce the pixel size
  - ➔ 3D integration
  - Two SOI chips are connected by Au micro bump
    - Complicated circuit in smaller pixel

T-Micro
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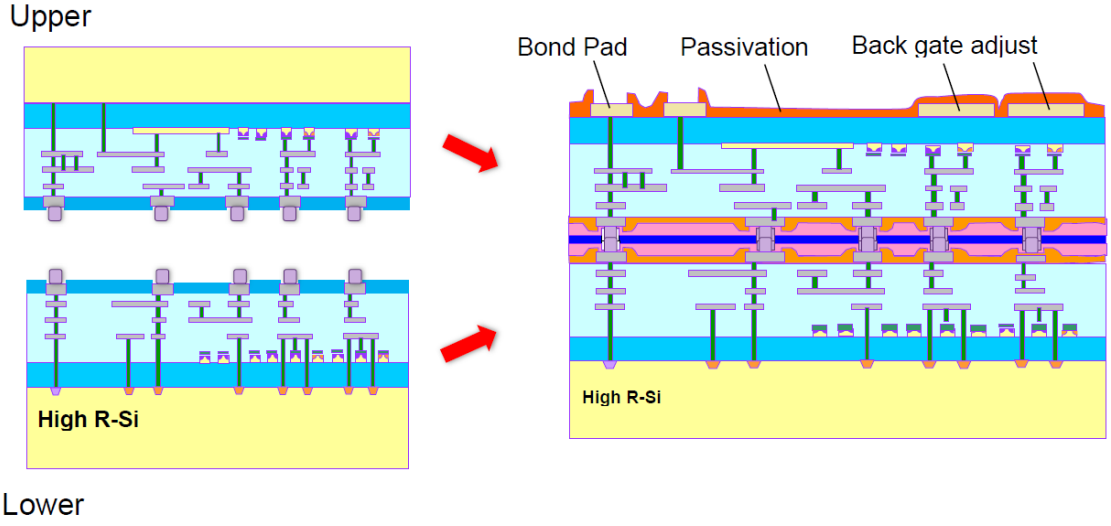
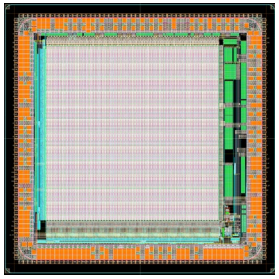


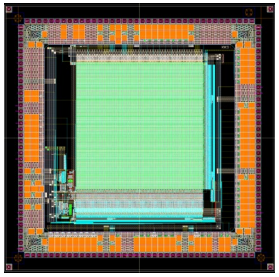
# SOFIST4 3D

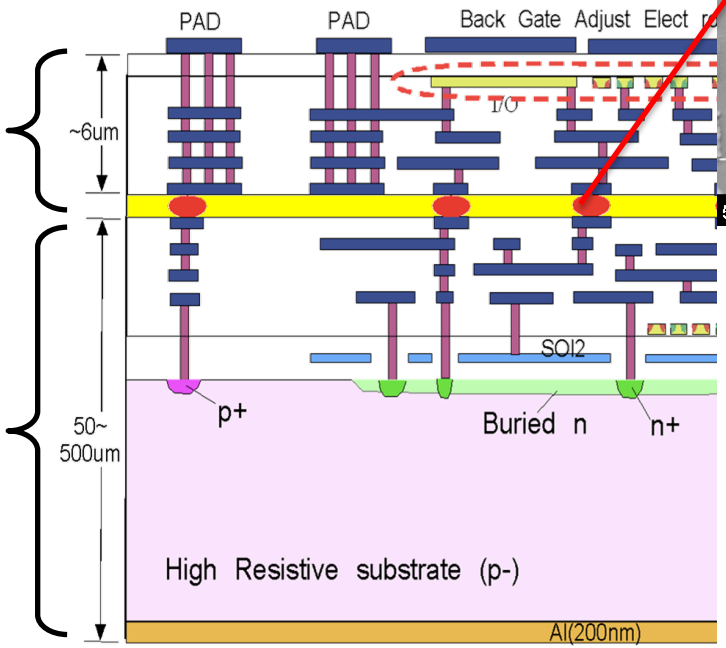
- Au cylindrical micro bump.
- The bonding efficiency is more than 99.96%
- β-ray signal seen

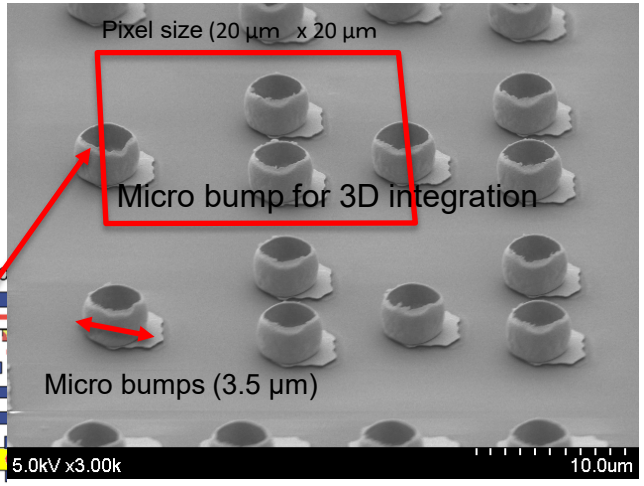
Upper chip (additional circuit) Thinned to 6 μm thick



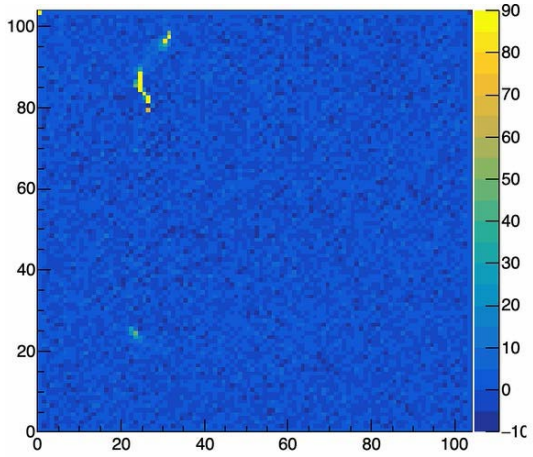
Lower chip (SOI pixel sensor)





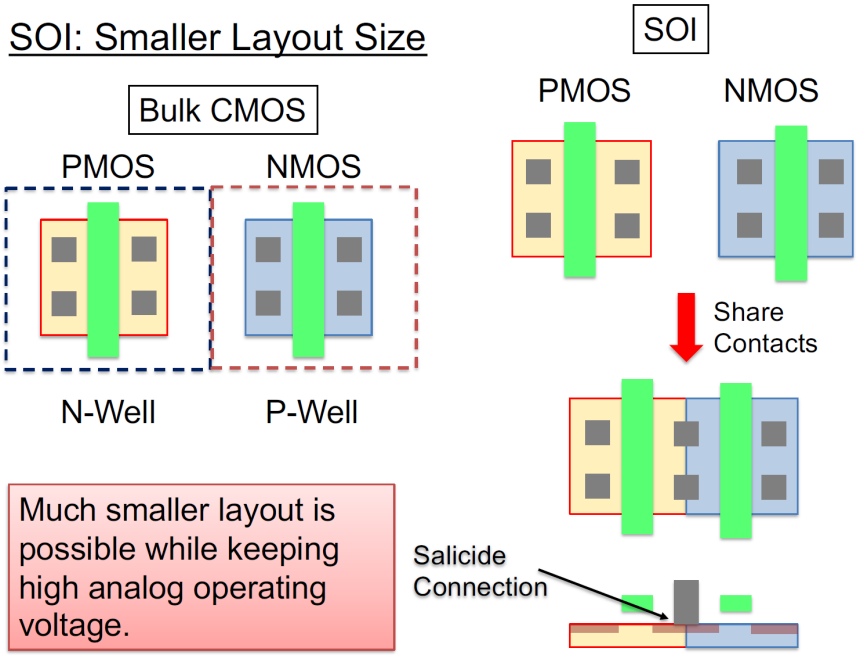

$^{90}$Sr β-ray signal seen




The president Motoyoshi-san is joining this workshop

# Active Merge Technique

- Cirucit area can be smaller than bulk CMOS with the same process rule.
  - While finer commercial process can be used for CMOS (ex. 65nm).
- Circuit area of DFF can be reduced to 16.5% with active merge
  - 84um$^2$ → 13.8um$^2$

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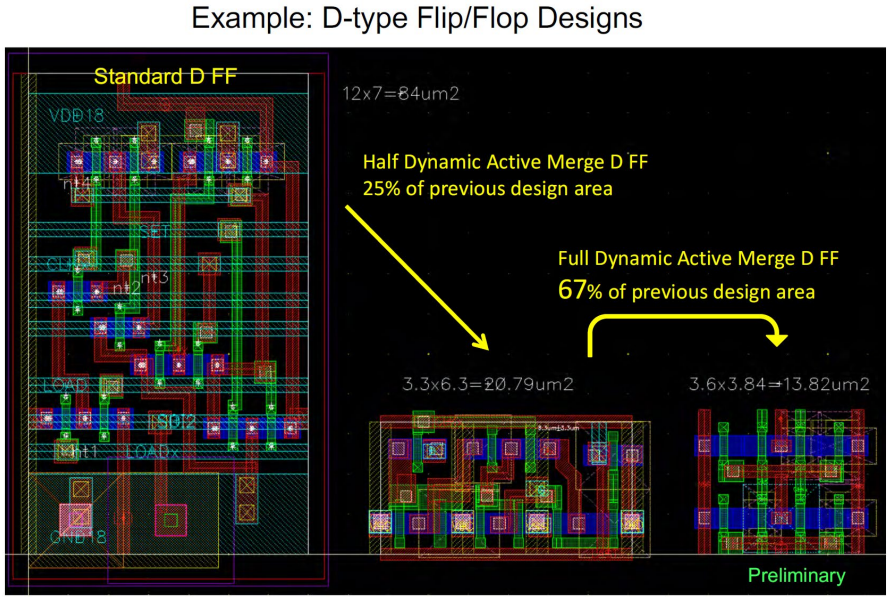


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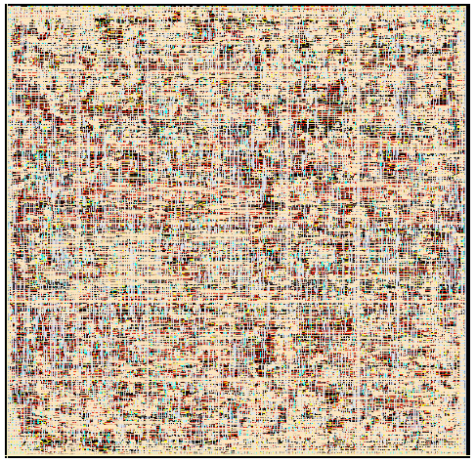
# Digital Library and Automatic Routing

- First digital library for Lapis SOI process was established by IPHC, Strasbourg group
- Prof. Cong-Kha Pham from the U of Electro-Communications developed automatic routing from Verilog source.
  - 8-bit RISC open source CPU, named Open8 SoC, was fabricated on SOI with the tools.
  - Test with real CPU will be performed.



**Open8** SoC summary

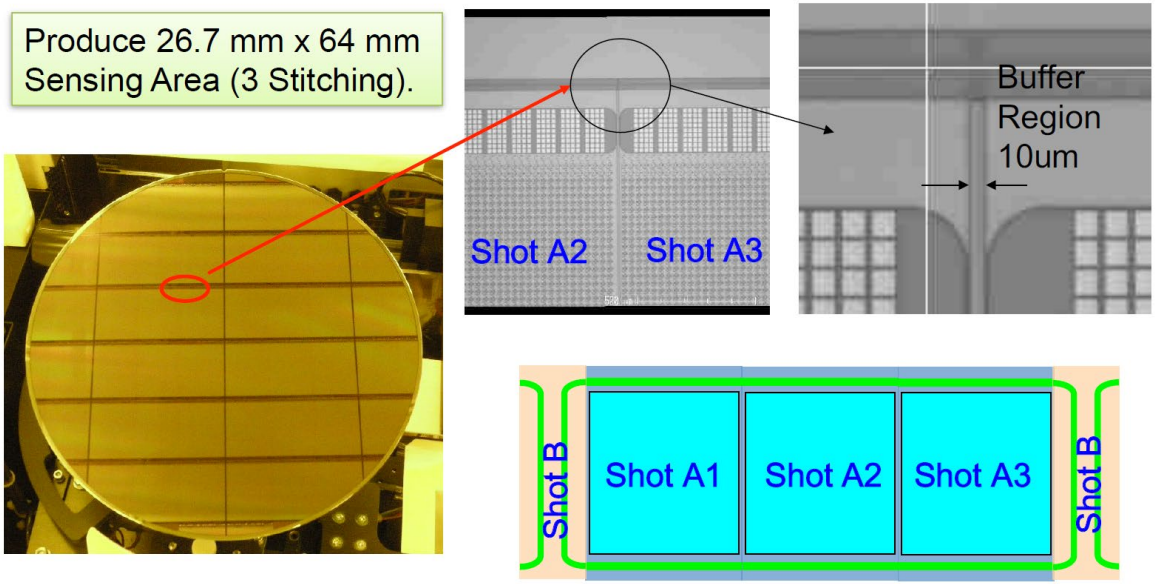
| At Synthesis | |
|---|---|
| **#Cell** | 11,109 |
| **Area** (μm²) | 486,001 |
| $F_{Max}$ (MHz) | 27 |

| At PnR | |
|---|---|
| **#Cell** | 11,691 |
| **Area** (μm²) | 798,470.7 (928.8×859.68) |
| **Density** *(%)* | 43.92 |
| $F_{Max}$ (MHz) | 52 |
| **Power** *(mW)* | 2.098 |
| **#MOSFET** | 219,454 |

# Stitching

- To make bigger chip, stitching technique was developed by RIKEN group for X-ray material science at SACLA.

Stitching for SOPHIAS (X-ray sensor
26.7mm x 64 mm single chip




- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.
- 1-direction stitching at present.

# Belle II

- Arthur Bolz – Current pixel detector : DEPFET
- Kookhyun Kang – Current strip detector : SVD

- Toru Tsuboyama – General VXD upgrade
- Zihan Wang – Thin strip detector option for the upgrade
- Ivan Dario Caicedo Sierra – DMAPS option for the upgrade

- I will talk on an SOI pixel detector option for the upgrade

# SOI for Belle II

- Originally considered for upgraded SuperKEKB with L=4x$10^{36}$
- But of course we can use it for upgrade in 2027~28 for the design luminosity of 6x$10^{35}$.

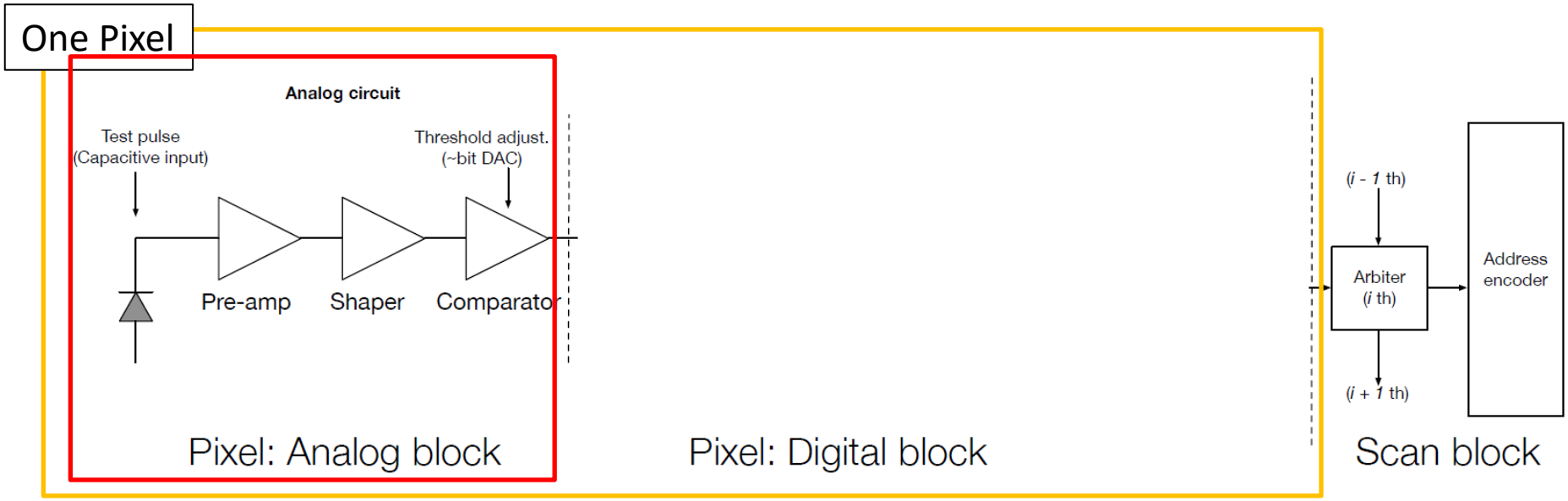
| system | layer | radius [mm] | hit rate [6] [MHz/cm$^2$] | occupancy [%] | TID [kGy/smy] | neutron [$10^{10}$n$_{eq}$/cm$^2$/smy] |
|---|---|---|---|---|---|---|
| PXD | 1 | 14 | 22.6 | 1.3 | 19.9 | 40 |
| | 2 | 22 | 11.3 | 0.5 | 4.9 | 20 |

- Concept
  - Binary detector to reduce data size and power consumption.
  - Fast clock to reduce the occupancy of O($10^{-3}$) or less at upgraded SuperKEKB L=4x$10^{36}$
  - Global shutter readout based on L1 Trigger to reduce data size.
  - Hold signals at least 4.4us trigger latency
  - Small power consumption ~0.1W/cm$^2$

- We invented the “DuTiP” concept for this purpose.

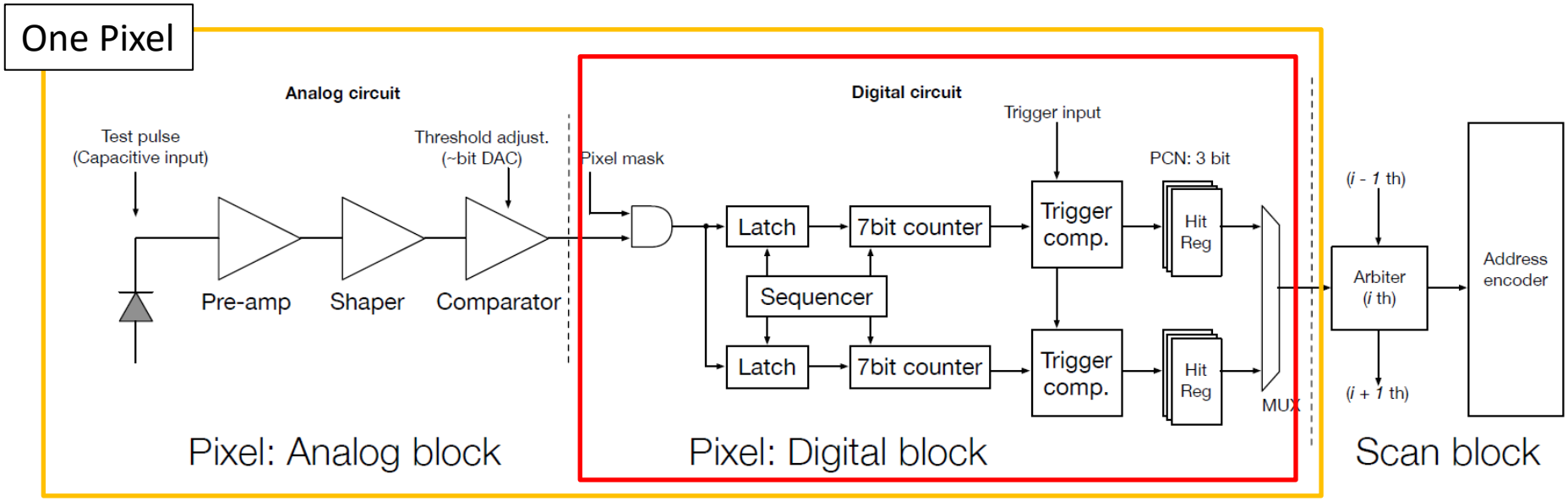
# The Concept “DuTiP”

- Dual Timer Pixel
- Analog Circuit
  - In Pixel Amplifier/Shaper/Discriminator.
  - Binary signal sent to digital circuit in the pixel.



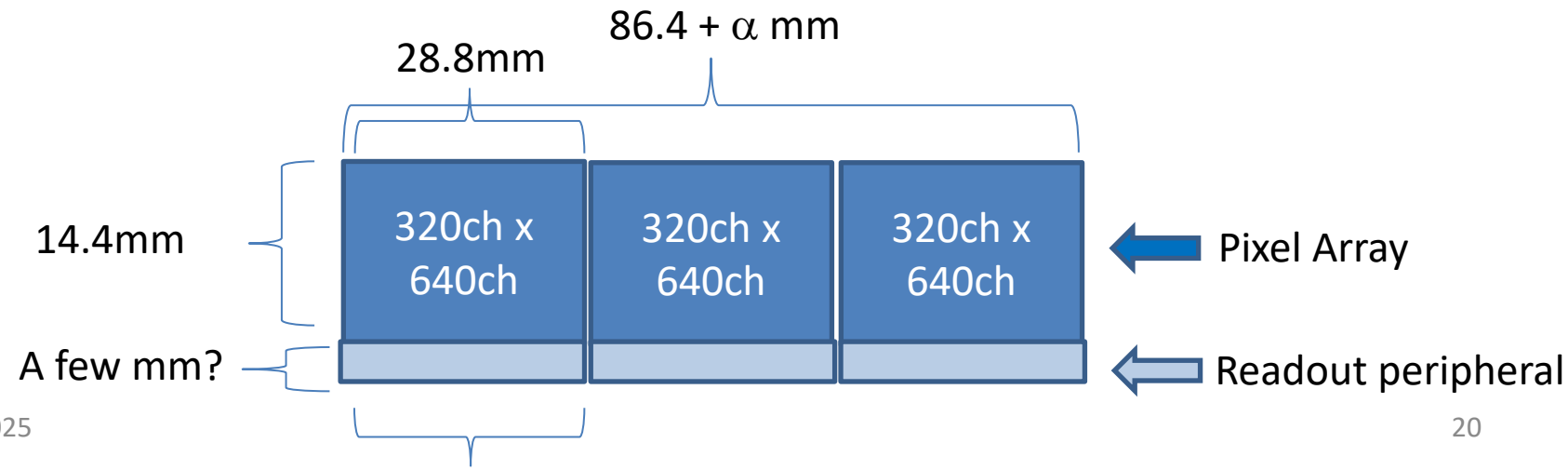
# The Concept “DuTiP”

- Dual Timer Pixel
  - Dual Timer (down time counters) in a Pixel to store signal and wait for trigger signal
  - 7bit timer can wait upto 127*CLK.
  - Two timers allow the second hit during trigger latency
  - Hit registers for three time buckets, previous, current and next for timing scan

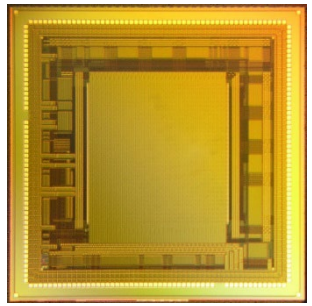


# Sensors for Layer1

- Layer1 : R=1.4cm, Z=7cm
- maximum mask size for SOI is 2.46 x 3.08 $cm^2$
- We need three chip to cover the acceptance in Z.
  - Row : 45um x 320ch = 14.4mm
  - Column : 45um x 1920ch (640ch x 3) = 86.4mm (28.8mm x 3)
  - Thickness : $50um^t$
  - (Stitching buffer width: ~10um if we adopt stitching)
- 8 ladders to cover the acceptance in phi



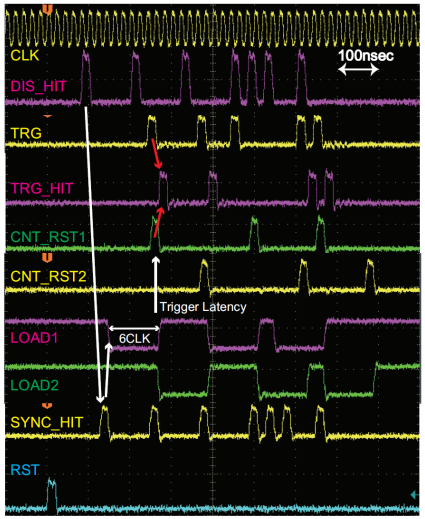
# DuTiP1 with SOI technology



- Dimension
  - 6mm$^2$ chip
  - Pixel Size 45um x 45um → 45um/√12 ~ 13um resolution
    - charge sharing improves it
  - 64x64 pixel array
- Analog circuit
  - ALPIDE analog circuit fabricated on SOI by Strasbourg and modified by KEK.
    - This is the first time to test the ALPIDE analog circuit on SOI
  - Low power amplifier
- Digital Circuit
  - 7bit x 2
  - 15.9MHz(62.9ns) CLK (SuperKEKB 509MHz/32(1.97ns*32) )
    - Trigger latency of at most 8us (4.4us requirement)
  - Only current and previous time buckets (no next bucket
  - PIXOR digital circuit, which works with 50MHz, adopted

    "Development of the Pixel OR SOI detector for high energy physics experiments",
    Y. Ono, A. Ishikawa, H. Yamamoto, Y. Arai, T. Tsuboyama, Y. Onuki, A. Iwata, T. Imamura, T. Ohmoto,
    NIM A 731, 266-269, 2013, doi:10.1016/j.nima.2013.06.044
  - No sophisticated readout circuit not fabricated

PIXOR2 digital flow



# Occupancy and Data Rate/Size

- Occupancy is enough small O($10^{-4}$) or less

| Layer | hit rate [Hz/pixel] | hit occupancy in PCN [$10^{-4}$] |
|---|---|---|
| 1 | 458 | 0.86 |
| 2 | 229 | 0.43 |

| system | layer | radius [mm] | hit rate [6] [MHz/cm$^2$] | occupancy [%] | TID [kGy/smy] | neutron [$10^{10}$n$_{eq}$/cm$^2$/smy] |
|---|---|---|---|---|---|---|
| PXD | 1 | 14 | 22.6 | 1.3 | 19.9 | 40 |
| | 2 | 22 | 11.3 | 0.5 | 4.9 | 20 |

- Data rate/size are enough small even for layer1.

| Layer | data rate per SS chip [Mbps] | data rate per ladder [Mbps] | data rate per layer [Mbps] | data size [TB/smy] |
|---|---|---|---|---|
| 1 | 11.3 | 34.0 | 272 | 340 |
| 2 | 5.65 | 22.6 | 271 | 339 |

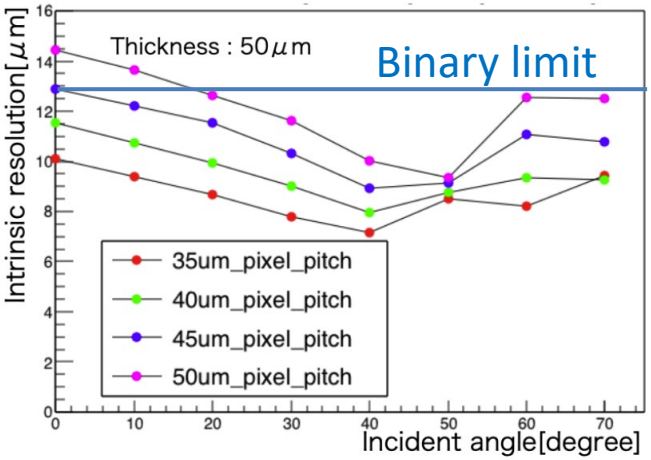
# Intrinsic and Impact parameter Resolutions with GEANT4

- Sensor intrinsic resolution and impact parameter resolution has been studied with simple geometry using GEANT4 MC.
  - Intrinsic resolution is better than binary limit thanks to charge sharing

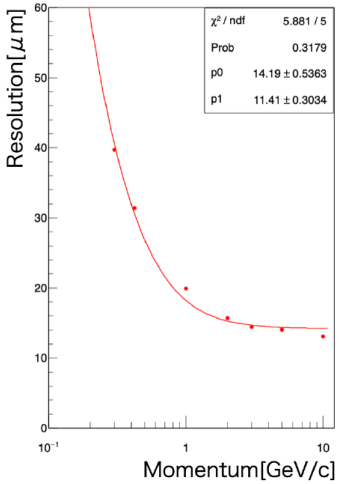
2layer DuTiP + 4Layer SVD

impact parameter resolution for theta=90deg

intrinsic resolution

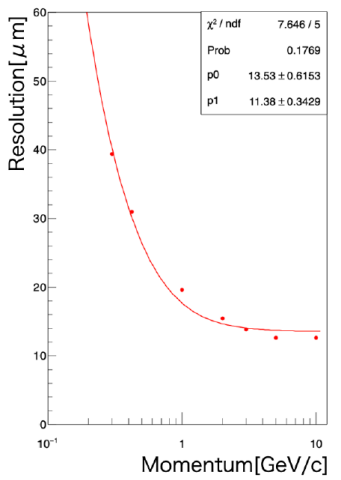



Z resolution




$$\sigma_Z(\mu m) = 14.2 \oplus \frac{11.4}{p \sin^{\frac{5}{2}}\theta}$$

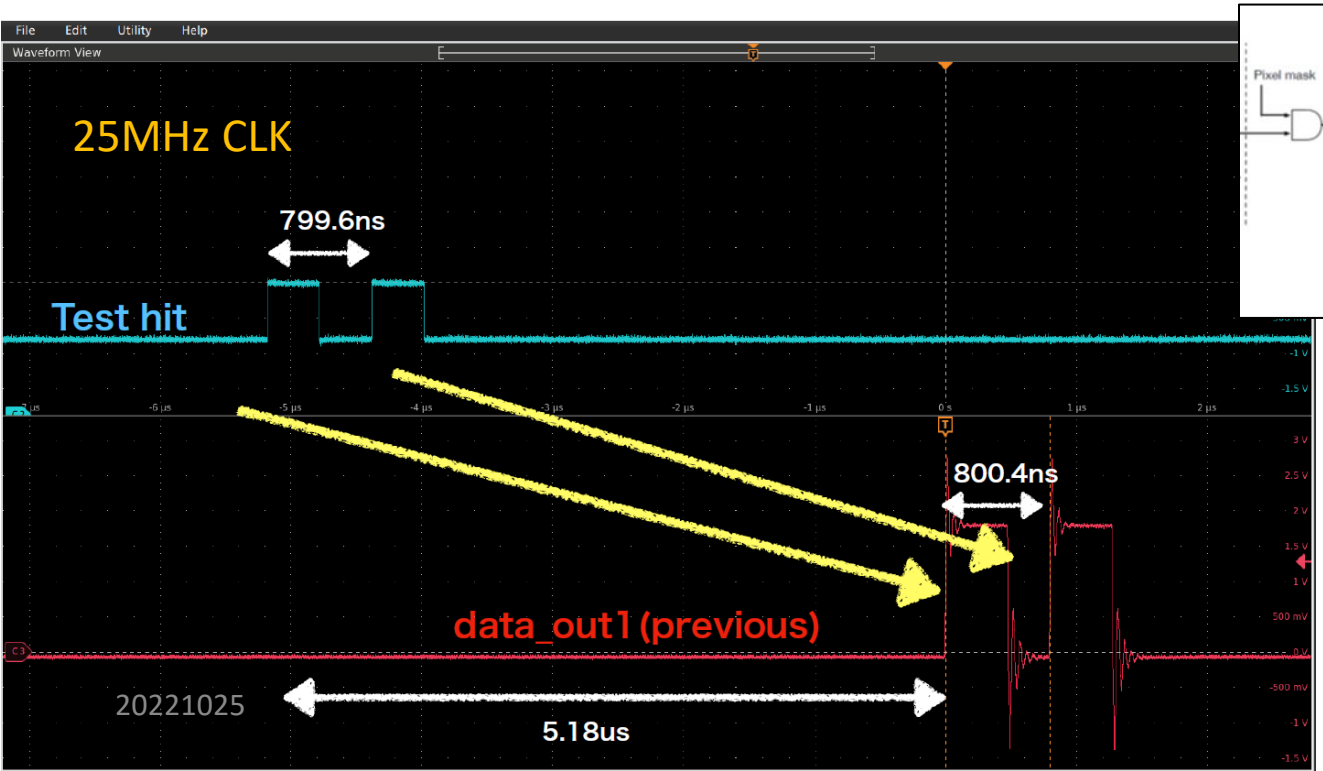
rϕ resolution

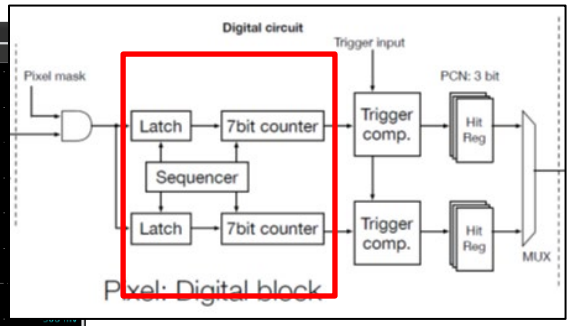



$$\sigma_{r\phi}(\mu m) = 13.5 \oplus \frac{11.4}{p \sin^{\frac{3}{2}}\theta}$$

# Characterization Sequencer/Dual Timer

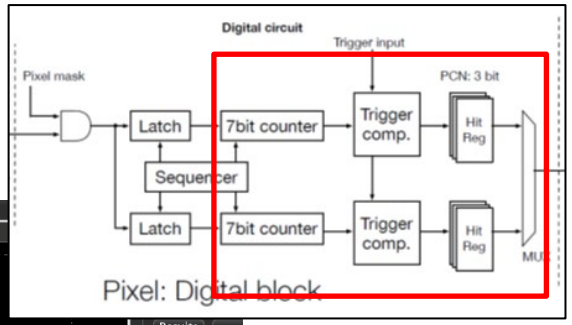
- Two test hit signals with 800ns interval which is less than trigger latency are injected.
- Triggers are also injected to previous timing
  - Two output signal can be correctly seen in previous buckets

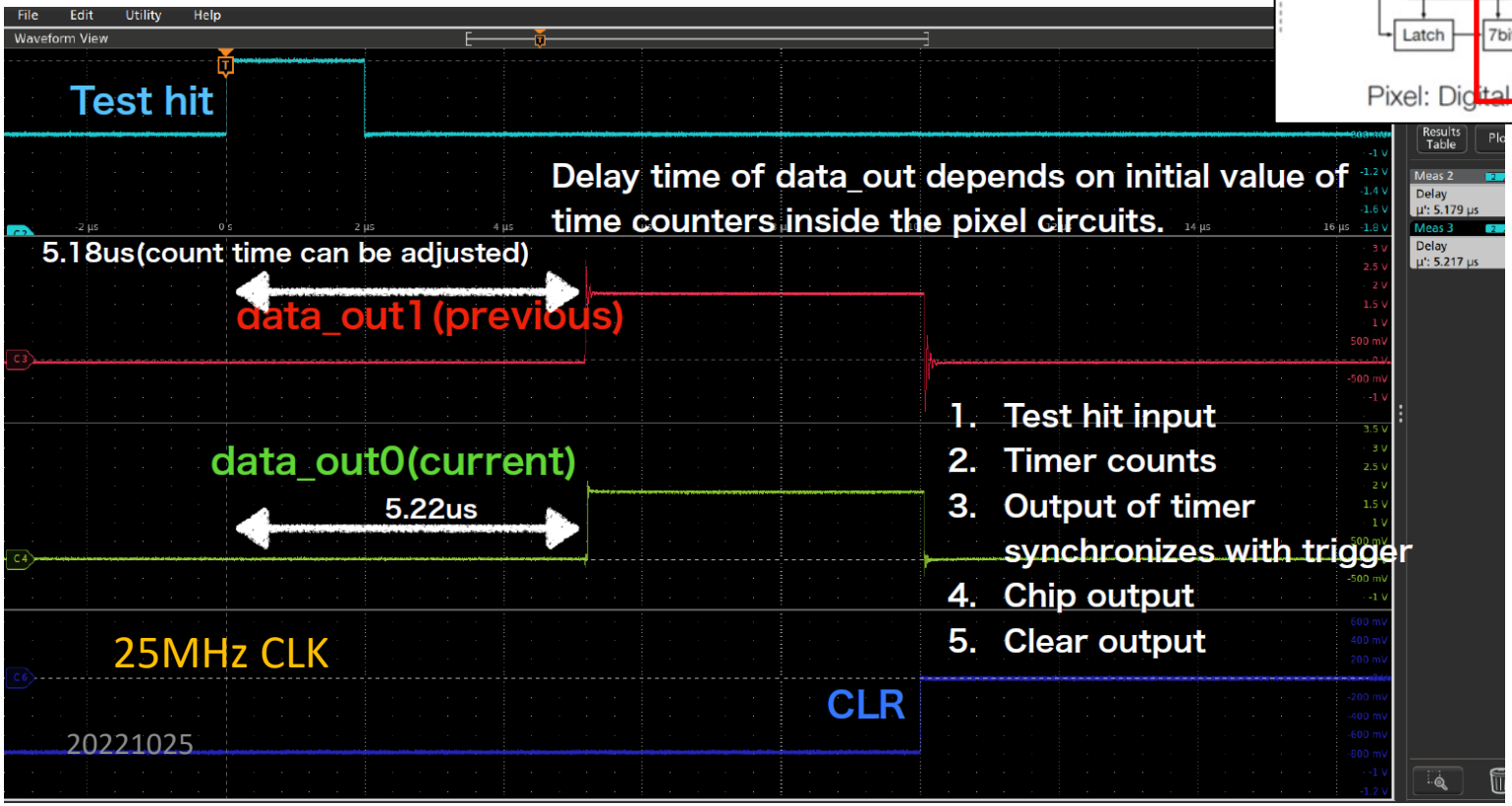


# Characterization
# Timers and Time Buckets

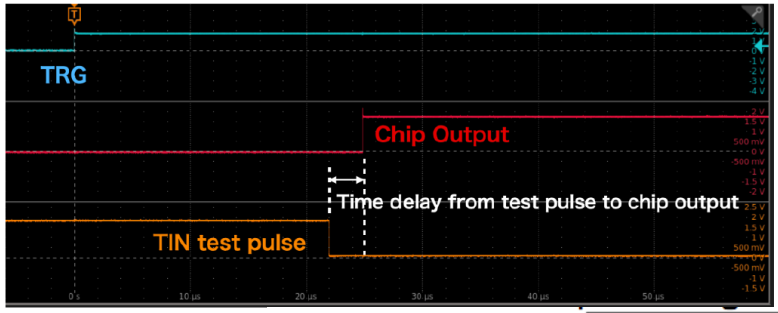
- test hit signal
  - 7bit counters (127*40ns=5080ns) are working fine
  - Correctly assigned to previous and current time bucket
- Digital Circuit is working perfectly.

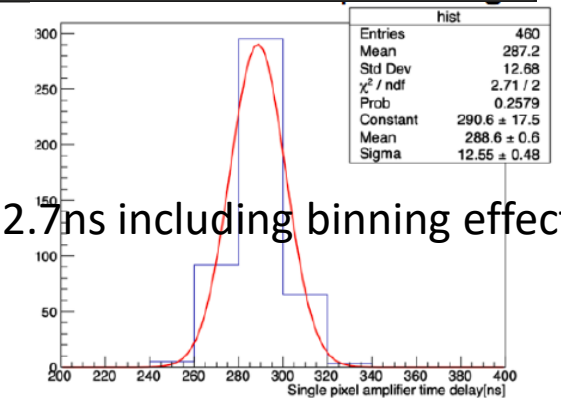


# Timing Resolution for single pixel

- DuTiP + Scintillation counter
- Tested with $^{90}$Sr and 50MHz CLK (20ns)
  - 11.7ns
    - With test pulse ~10ns
  - Enough smaller than time bucket of 63ns




12.7ns including binning effect

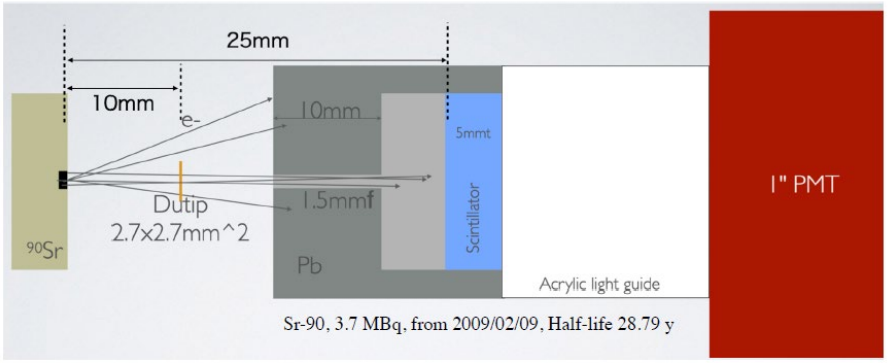



fig. Setup of the Beta ray measurement triggered by the scintillator

$^{90}$Sr irradiation

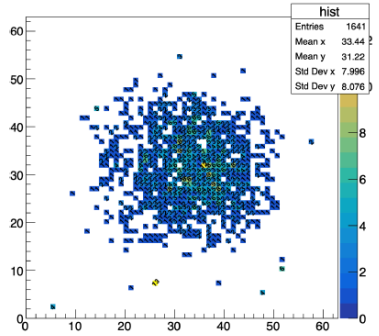



fig. The histogram image of the beta ray. Triggered by the electrons restricted by the collimator.

# Efficiency

- Tested with $^{90}Sr$
  - DuTiP + Scintillation counter
  - Efficiency
    - Using $^{90}Sr$ : ~98+-2%
    - Cosmic or accidental noise hit are subtracted with dry run data.
  - We will use KEK new electron beam line, upto 5GeV

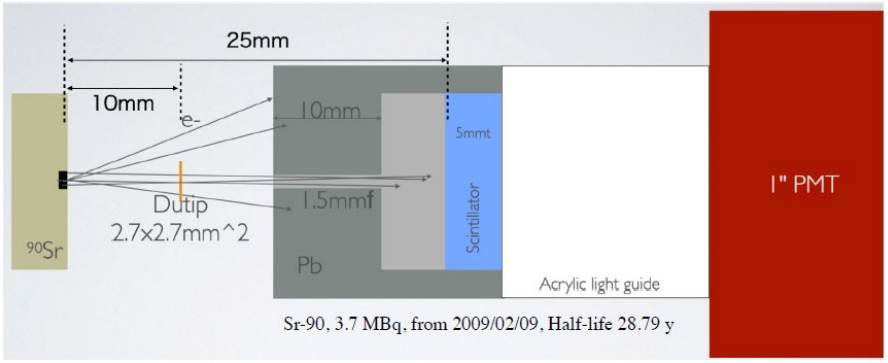



**fig. Setup of the Beta ray measurement triggered by the scintillator**

$^{90}Sr$ irradiation

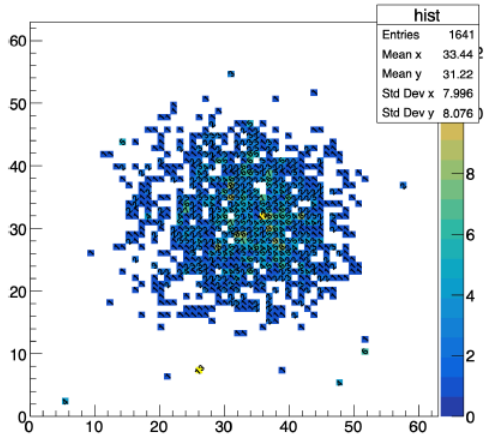
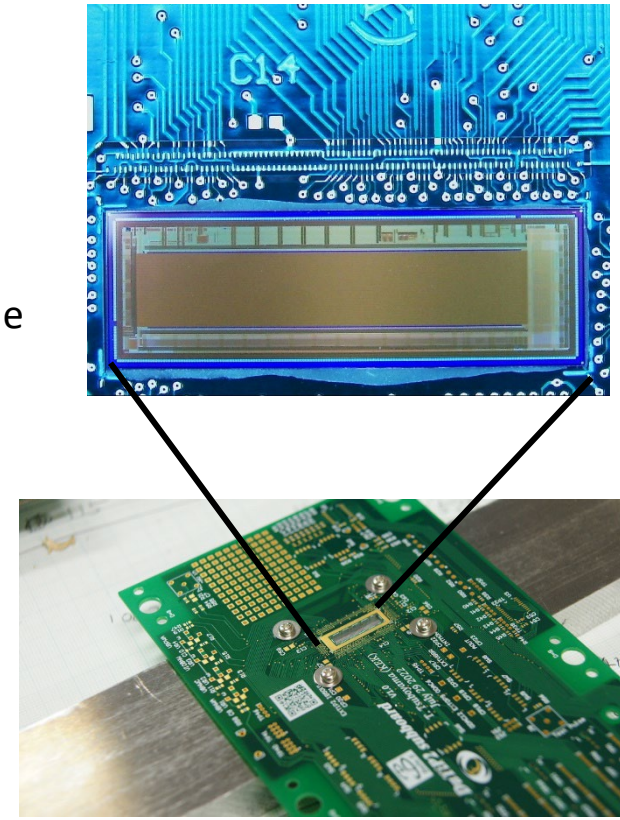



**fig. The histogram image of the beta ray. Triggered by the electrons restricted by the collimator.**

# DuTiP2

- Almost Full functionality
  - Circuit NOT fabricated for DuTiP1 should be in
    - Fast data transfer circuit from the periphery to outside
      - 300MHz 1.8V LVDS
    - Except for PLL and pixel array scan system
  - Full size chip just for row direction (r-phi)
    - Chip size : 17.2mm x 6.0mm
    - Pixel array : 14.4mm (row) x 2.88mm (column)
    - Full size chip 14.4mm (row) x 28.8mm (column)
    - Increasing the size to z direction is trivial
- Delivered the chip in 2022 June.
- Characterization to be started.




| pitch [$\mu$m] | row $\times$ column [pixels] | array $r$-$\phi$ $\times$ $z$ [mm$^2$] | array area [cm$^2$] | chip $r$-$\phi$ $\times$ $z$ [mm$^2$] |
|---|---|---|---|---|
| 45 | 320 $\times$ 640 | 14.4 $\times$ 28.8 | 4.15 | 17.2 $\times$ 29.6 |

# Summary

- SOI is suitable for high energy hysics
- Since 2005, Japanese group is developing the SOI pixel detector with Lapis semiconductor
  - Several technology were developed

- DuTiP concept for Belle II and ILC were invented.
- First prototype DuTiP1 was tested
- Second one was delivered and will be tested soon.

# Acknowledgement


- This talk is supported by the Grant-in-Aid for Scientific Research (A), “Search for physics beyond the Standard Model by studying lepton universality in B meson decays”, 22H00144

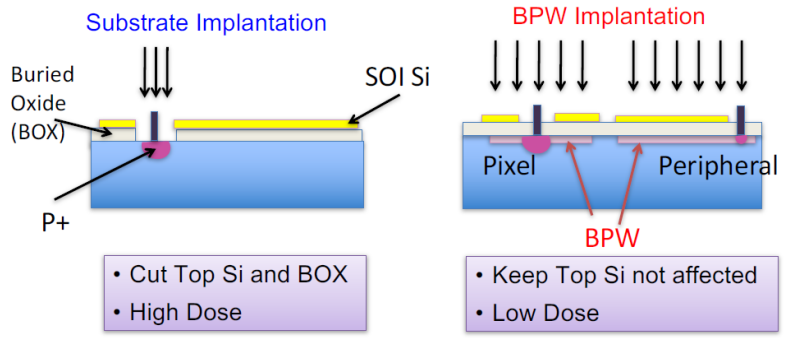
- B中間子崩壊でのレプトン普遍性の研究による素粒子標準理論を超える物理の探索

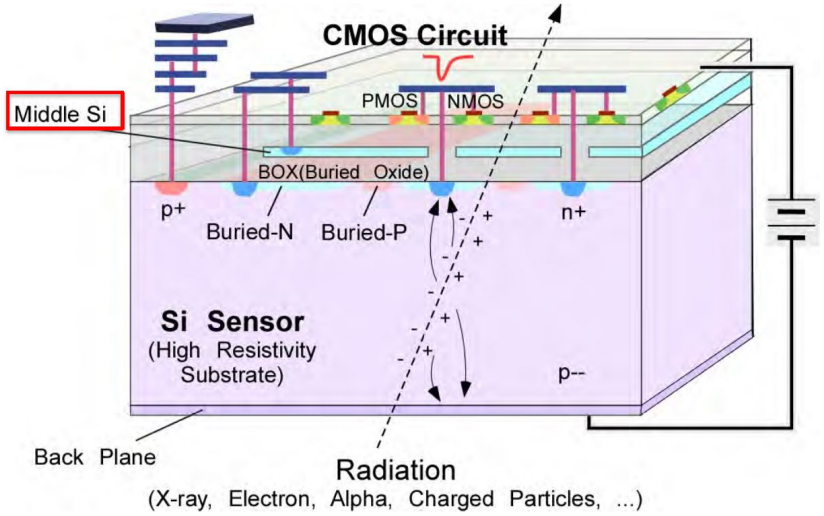

# Backup

“New pixel detector concept DuTiP for Belle II upgrade and the ILC with an SOI technology”

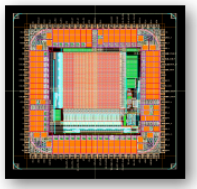
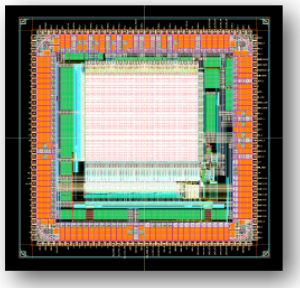
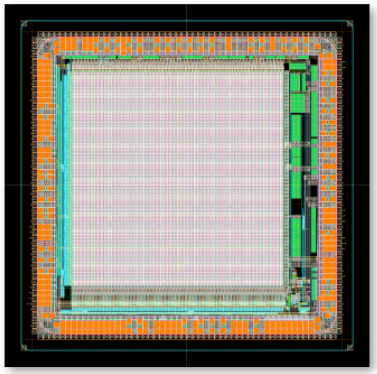
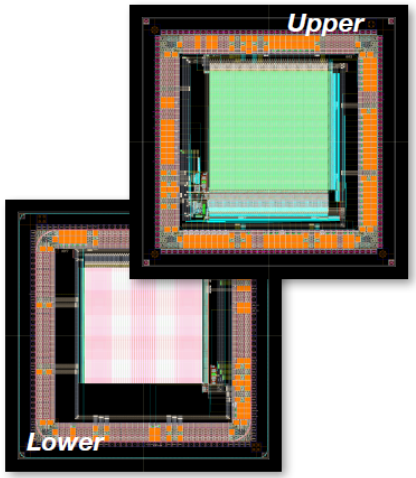
# Two difficulties for SOI Solved

- Back-gate effect
  - Applied E-field affects the circuit
  - Suppressed by buried P well (BPW)
    - Additional well below the circuit.
- Radiation tolerance (hole trapped by BOX)
  - E-field by holes affects the circuit
  - compensated by Double SOI
    - Additional silicon layer in BOX layer applied LV.
  - Upto 20Mrad was tested with transistor TEG.

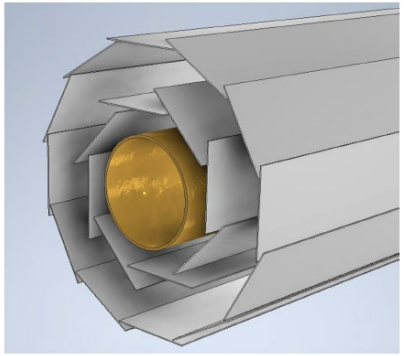


# SOFIST

| SOFIST | ver.1 | ver.2 | ver.3 | ver.4 (3D) |
|---|---|---|---|---|
| | Beam test at FNAL in Jan. 2017 Analog signal | Beam test at FNAL in Feb. 2018 Analog signal or Timestamp | Beam test at FNAL in Feb. 2019 Analog signal and Timestamp | Beam test at FNAL in Feb. 2020 |
| |  |  |  |   |
| Chip Size ($mm^2$) | 2.9 × 2.9 | 4.45 × 4.45 | 6 × 6 | 4.45 × 4.45 |
| Pixel Size ($\mu m^2$) | 20 × 20 | 25 × 25 | 30 × 30 | 20 × 20 |
| Pixel Array | 50 × 50 (Analog Signal) | 64 × 64 (Time Stamp)<br>16 × 64 (Analog Signal) | 128 × 128<br>(Analog signal and Time stamp) | 104 × 104<br>(Analog signal and Time stamp) |
| Functions (Pixel) | Pre. Amplifier (CSA)<br>Analog signal memory (2 hits) | Pre. Amplifier (CSA)<br>Comparator (Chopper inverter)<br>Shift register (DFF × 2)<br>Analog signal memory (2 hits)<br>or<br>Time stamp memory (2 hits) | Pre. Amplifier (CSA)<br>Comparator (Chopper inverter)<br>Shift register (DFF × 3)<br>Analog signal memory (3 hits)<br>Time stamp memory (3 hits) | Pre. Amplifier (CSA)<br>Comparator (Chopper inverter)<br>Shift register (DFF × 3)<br>Analog signal memory (3 hits)<br>Time stamp memory (3 hits) |
| Functions (On Chip) | Column ADC (8 bit) | Column ADC (8 bit)<br>Zero-suppression logic | Column ADC (8 bit) | Column ADC (8 bit) |
| Wafer | FZ *n*-type (Single SOI) | Cz *p*-type (Double SOI) | FZ *p*-type (Double SOI) | FZ *p*-type (Double SOI) |
| Wafer Resistivity (kΩ·cm) | 2 ≤ | 1 ≤ | 3 - 10 | 3 - 10 |
| Status | Delivered (Dec. 2015)<br>Position resolution ~1.4 μm | Delivered (Jan. 2017)<br>Time resolution ~1.55 μs | Delivered (May. 2018)<br>Time resolution ~1.92 μs | Delivered (Jan. 2019 ~)<br>Under evaluation |

Beam pipe and Layer 1-2



# Possible Configuration

- 7-layer VXD
  - Layer 1-3 : S type chip
  - Layer 4-7 : L type chip with issuing input signal to track trigger
    - Binary detector can easily issue the signal by taking digital OR of hit information
    - Trigger cell is 1.44x1.44mm$^2$ → displaced track trigger for LLP possible?

TABLE IV. Possible pixel detector c

| Layer | Radius [mm] | $z$ Length [mm] | Number of Ladders |
|---|---|---|---|
| 1 | 14 | 70 | 8 |
| 2 | 21 | 105 | 12 |
| 3 | 35 | 175 | 20 |
| 4 | 55 | 275 | 20 |
| 5 | 80 | 400 | 28 |
| 6 | 105 | 525 | 38 |
| 7 | 135 | 675 | 48 |

TABLE II. The size of Small (S) and Large (L) DuTiP chips.

| sensor type | pitch [$\mu$m] | row × column [pixels] | array $r$-$\phi$ × $z$ [mm$^2$] | array area [cm$^2$] | chip $r$-$\phi$ × $z$ [mm$^2$] |
|---|---|---|---|---|---|
| S | 45 | 320 × 640 | 14.4 × 28.8 | 4.15 | 17.2 × 29.6 |
| L | 45 | 480 × 640 | 21.6 × 28.8 | 6.22 | 24.4 × 29.6 |

TABLE III. The trigger cell configuration.

| sensor type | input signal for trigger | trigger cell [pixels] | row × column [cells] | cell size [mm$^2$] |
|---|---|---|---|---|
| S | no | – | – | – |
| L | yes | 32 × 32 | 15 × 20 | 1.44 × 1.44 |

# Characterization of DuTiP1 Digital Circuit

- Digital Circuit
  - Test hit を入れて trigger 信号と同期した hit が正しい timing (previous/current) で出てくるか
  - Input clock 25MHz (40ns)
    - faster than 15.9MHz for real operation
    - 7bit -1 →127CLK → 5.08us latency