Business from technology

Recent Results of VTT's Edgeless Detector Prototypes

6th "Trento" Workshop on Advanced Silicon Radiation Detectors, 2011

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Content

- **VTT's nanofabrication facilities**
- **Edgeless Si Detectors**
  - Structure and fabrication
  - Preliminary results of latest p-on-n edgeless detectors
  - Detector assembly
  - Latest Imaging results (n-on-n edgeless detectors)
- **Summary and outlook**

MICRONOVA CLEANROOMS

Main Cleanroom Characteristics

Total Area	2 600 m^2
(Largest cleanroom in Scandinavia)	
Cleanroom Classification	ISO 4…ISO 6
(in clean bays)	(10…1000)
Temperature	21 °C ± 0,5 °C
Relative humidity	45 % ± 5%

Clean bay - Service chase type
Ventilation based on filter fan units
Raised perforated floor
Subfab with technical support areas

Labs with built-in Cleanrooms

Micropackaging lab - dicing saws, wire bonding

SubTech lab - Ion implantation, CMP, backgrinder, spin etcher

Process equipment is mainly for 150 mm wafer size, but some processes can be performed also on 200 mm wafers

Equipments

Furnace:

- oxidation, LTO, TEOS, Nitride, doped and undoped polysilicon
- 2 Centrotherm furnace stacks

Lithography:

- Contact aligners – MA150 and MA6 (bottom side alignment), MA200
- E-beam writing – Zeiss LEO 1560
- Step and Stamp Imprint Lithography – Suss MicroTec NPS 300
- i-line stepper, Canon FPA 2500i3
- Resist/development tracks, Suss ACS 200 and AIO Duna 700

Dry etching

- Etchers for silicon oxide, nitride, metals - LAM 4520/4420/9600
- Deep silicon etching - Aviza Omega i2L and STS ASE
- Silicon oxide ICP etching – STS AOE
- RIE – Oxford 80Plus
- Plasma strippers (PRS 800/801), microwave asher (Aura 1000), wet ozone stripping

Ion Implantation

- Medium current, 200 keV, P, As, B – Eaton NV8200-P

Equipments

Sputtering: AlSi, Mo, TiW, Si - Provac LLS 801

PECVD: Silicon oxide and nitride, incl. TEOS-process

Electroplating:

- Ni, Cu, SnAg, SnPb, SnBi and InSn – RENA and home-built plating systems

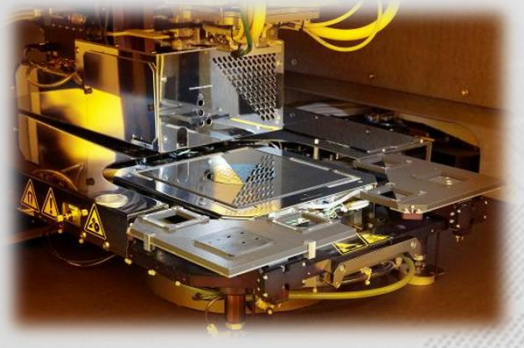
Flip-chip bonding: 2 Suss MicroTec FC150 bonders

Dicing: Disco DFD 651 and Loadpoint uAce-352

Fusion wafer bonding: EVG 5201S and EV 801 (non-IC materials)

Backgrinding (wafer thinning): Strasbaugh 7AF

Polishing and planarization: Strasbaugh 6DS-SP



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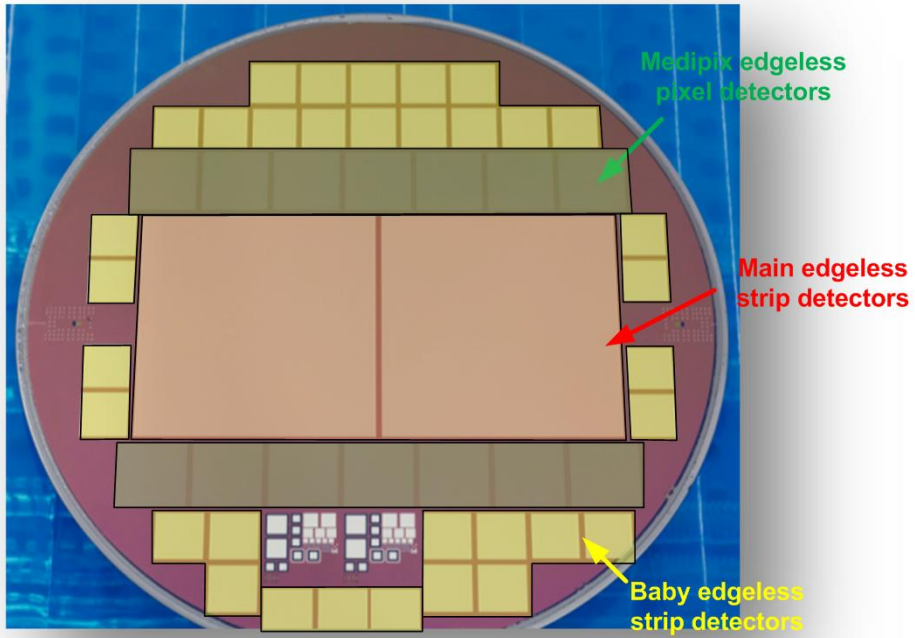
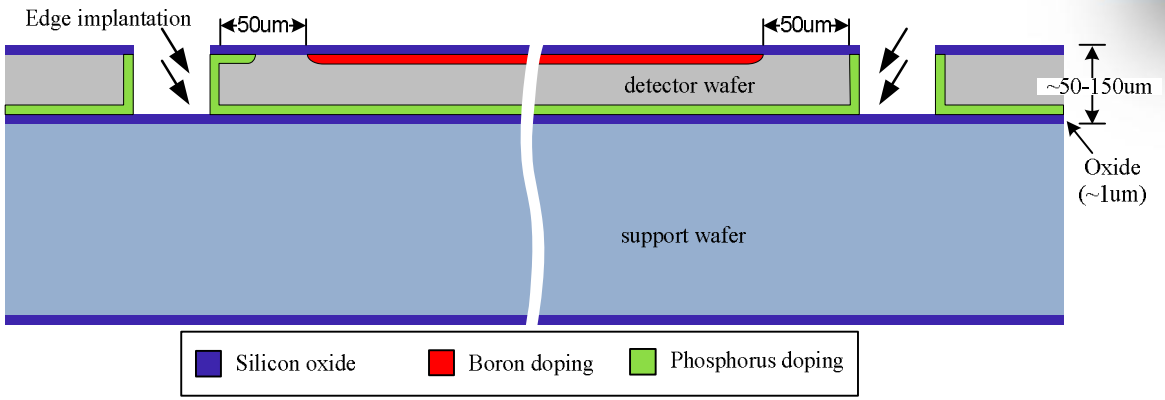
Wafer Layout and Detector Structure

- Various detector designs on 6 inch wafer
  - Main edgeless strip detectors
    - *5 x 5 cm²*
    - *50 µm edge distance*
  - Baby edgeless strip detectors
    - *1 x 1 cm²*
    - *20µm, 50µm, 100µm edge distance*
  - Medipix edgeless pixel detectors:
    - *1.4 x 1.4 cm²*
    - *20 µm & 50 µm edge distance*

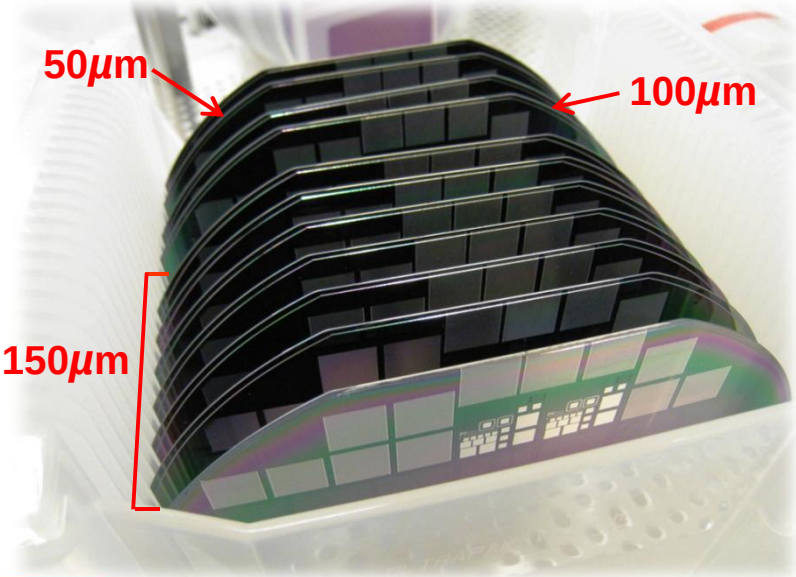


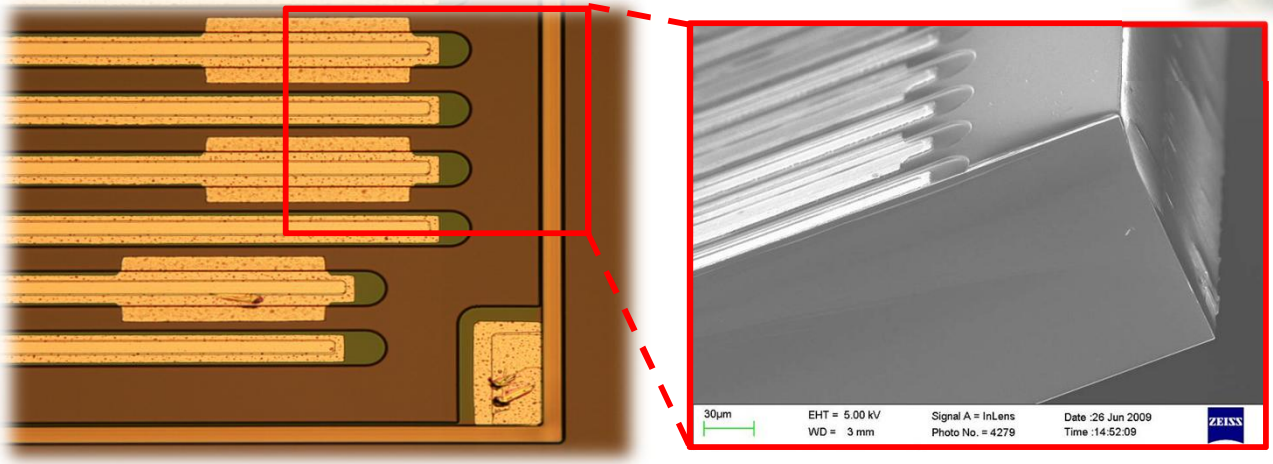


- Processing wafers with three thicknesses
  - *50µm, 100µm and 150µm*
- Edge implantation

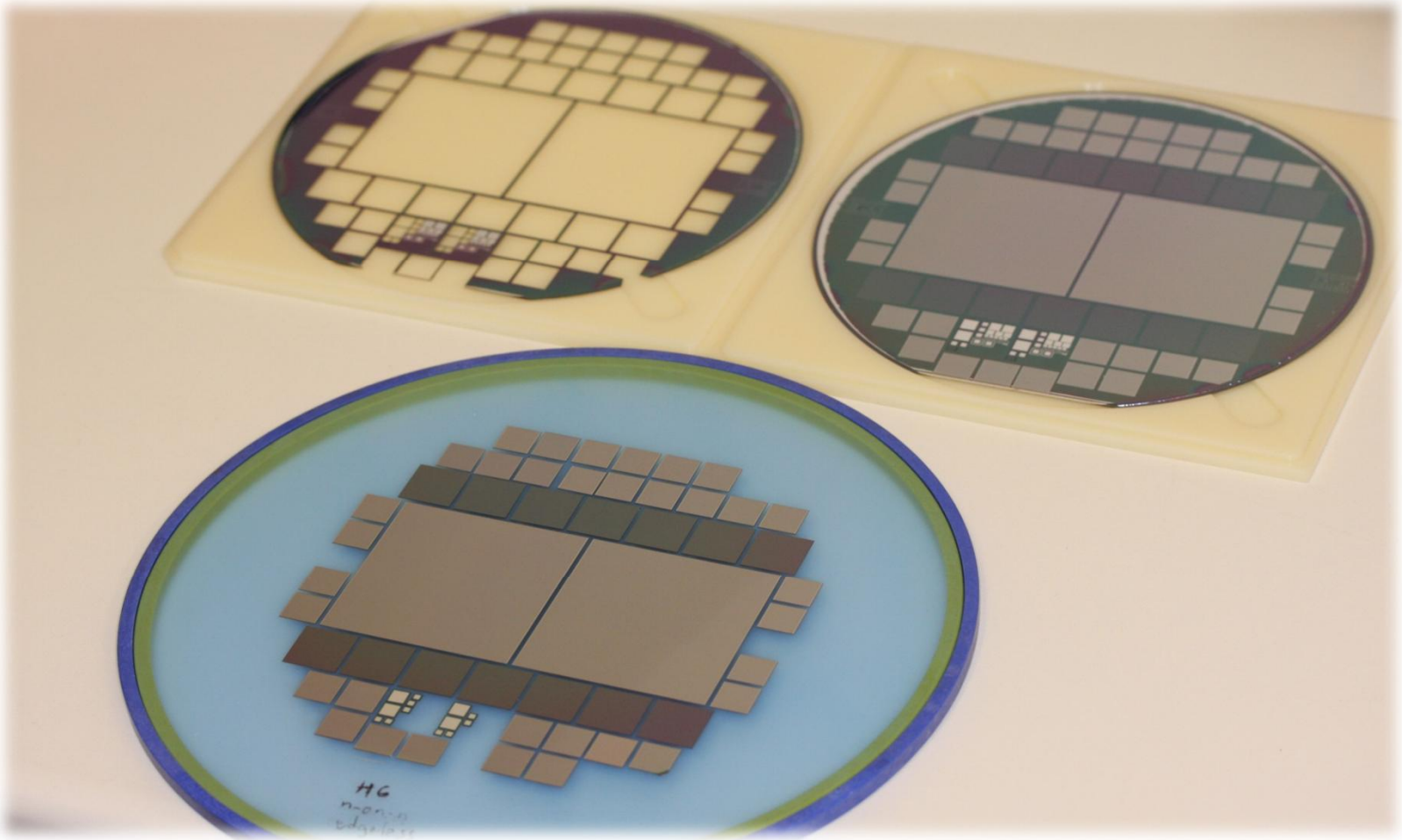
Edgeless Detector Fabrication at VTT

- 11 pcs edgeless wafers were fabricated
  - *2 pcs with 50 µm thickness*
  - *2 pcs with 100 µm thickness*
  - *7 pcs with 150 µm thickness*
- Inactive region at the edge less than 1μm
- Smooth chip edges obtained without dicing





Handle Wafer Removal



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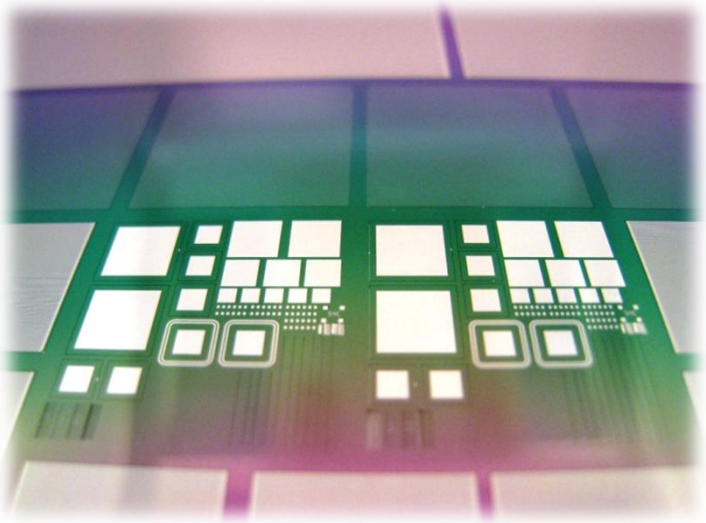
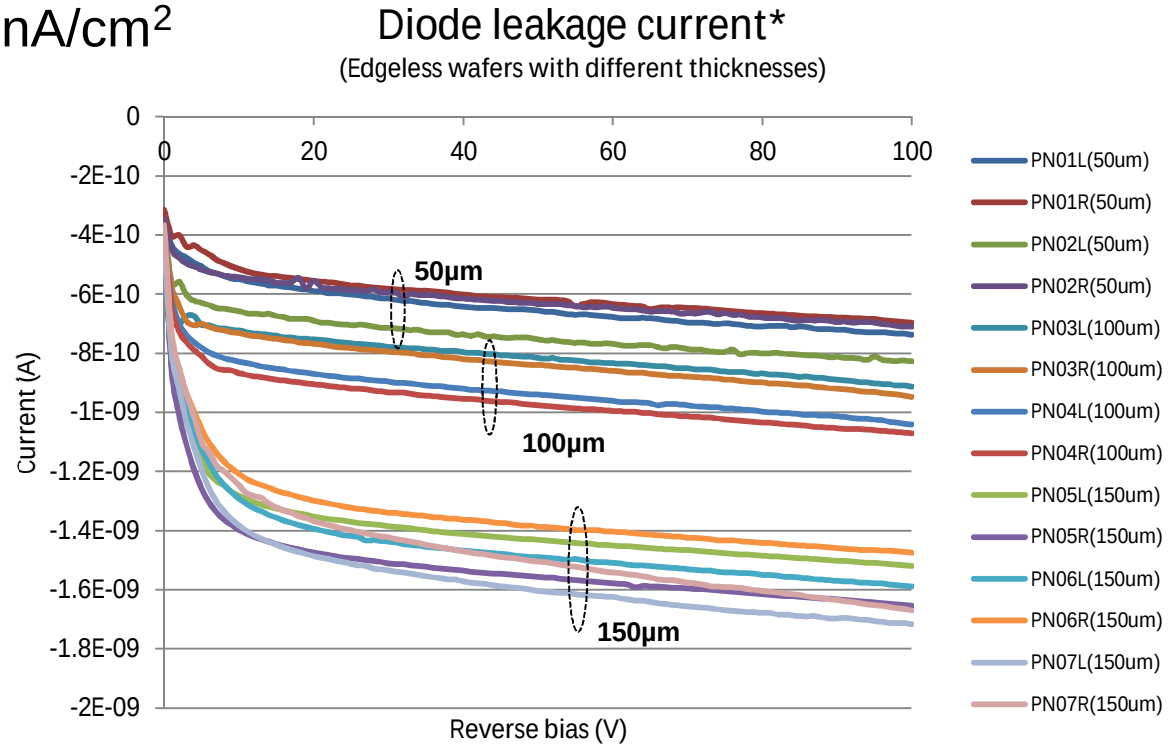
Diode Leakage Current

- Thin wafers with different thickness 50*μm*, 100*μm* and 150*μm*
- Distance from edge to diffusion: 50*μm*
- Low leakage current of 3 - 8 nA/cm^2

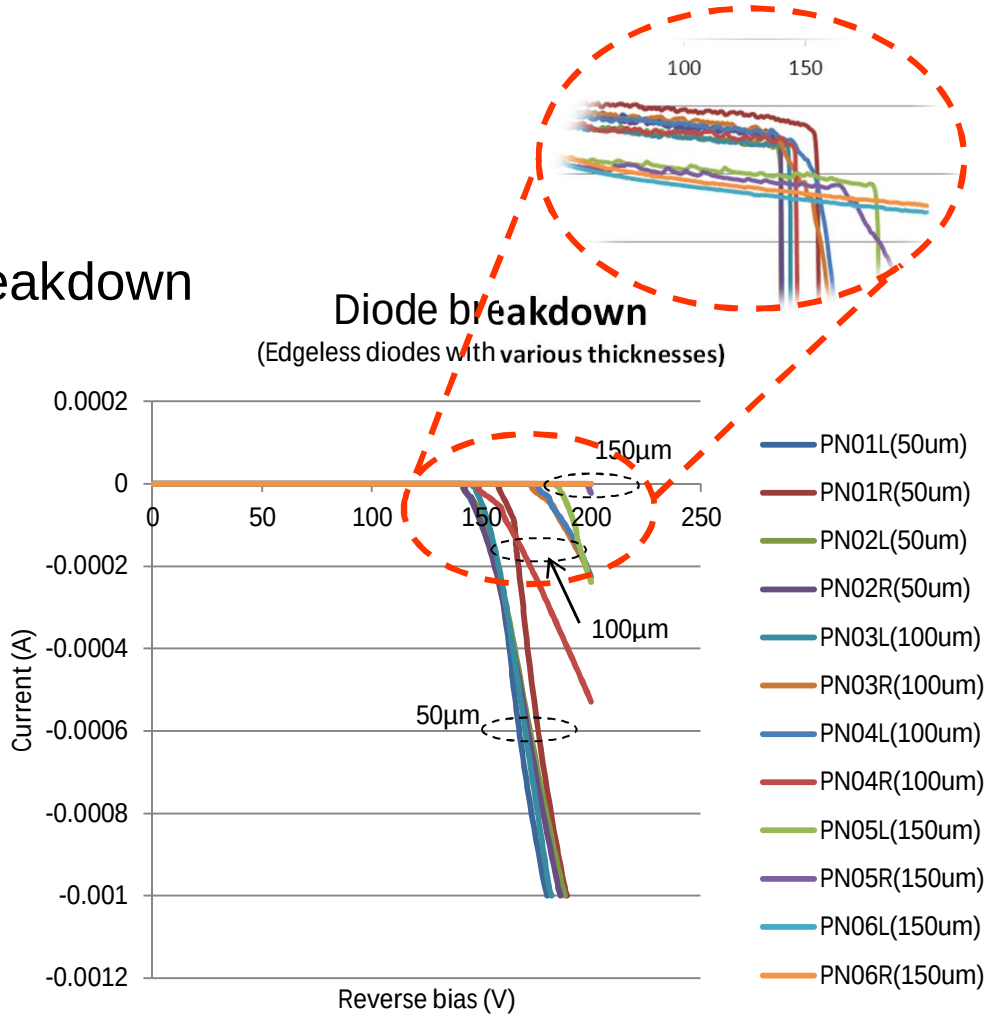




* Diode area: 5 mm x 5 mm

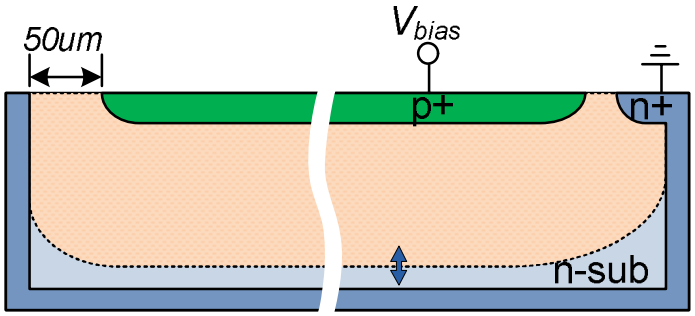
Breakdown

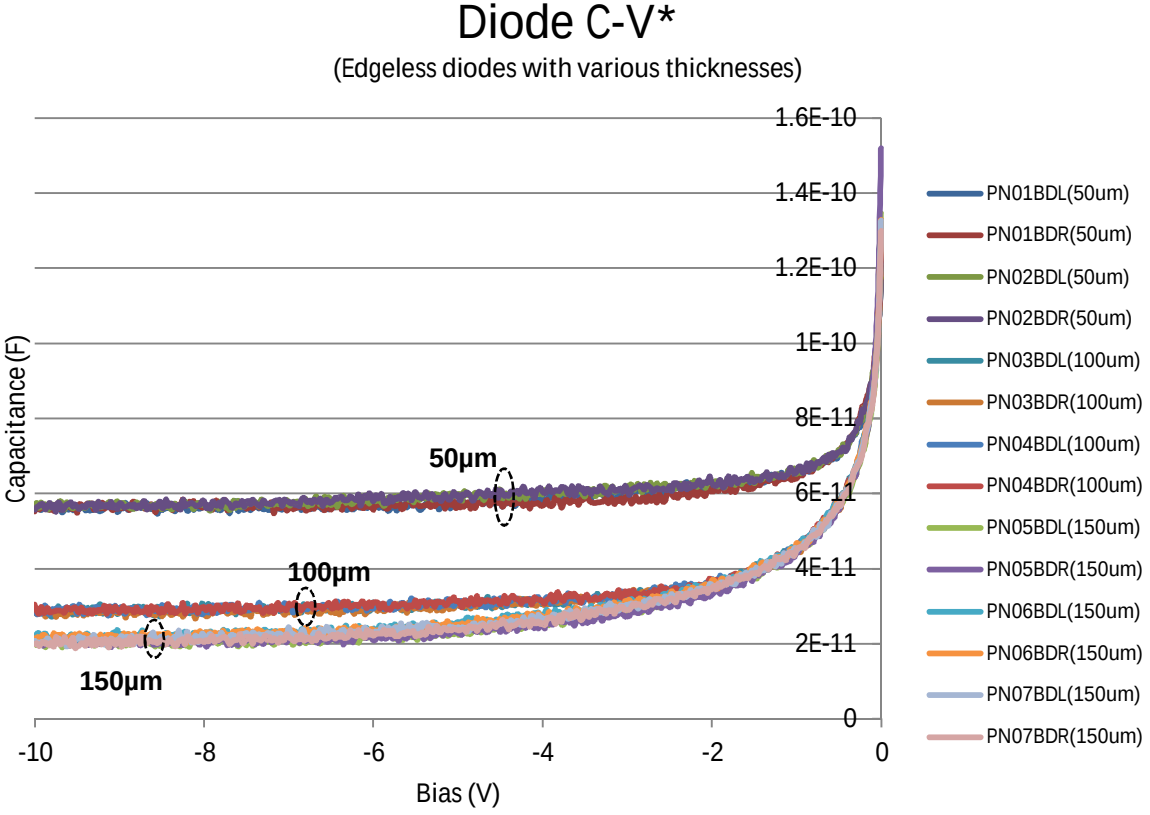
- Sharp breakdown features
- No breakdown below 130 V
- Thicker wafers have more robust breakdown performance
  - 50 µm: 135 ~ 150 V
  - 100 µm: 140 ~ 170 V
  - 150 µm: 170 ~ more than 200 V



Diode C-V

- Full depletion voltage of edgeless detectors with different thicknesses
  - 50 µm detector: ~ 4.5 V
  - 100 µm detector: ~ 7 V
  - 150 µm detector: ~ 8.5 V
- Edge distance dependence of capacitance
  - Only slight shift when thickness increases from 100µm to 150µm





* 10kHz, diode area: 5 mm x 5 mm

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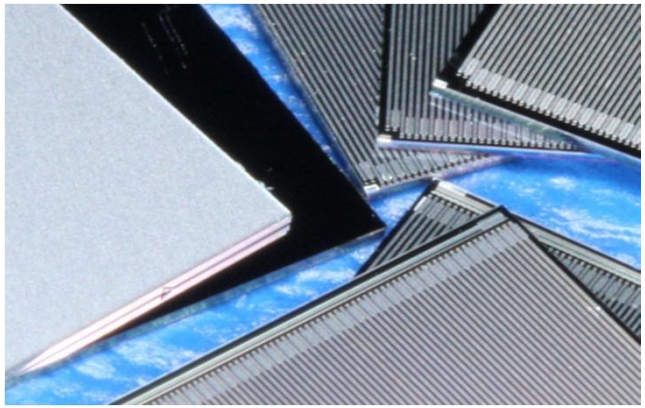
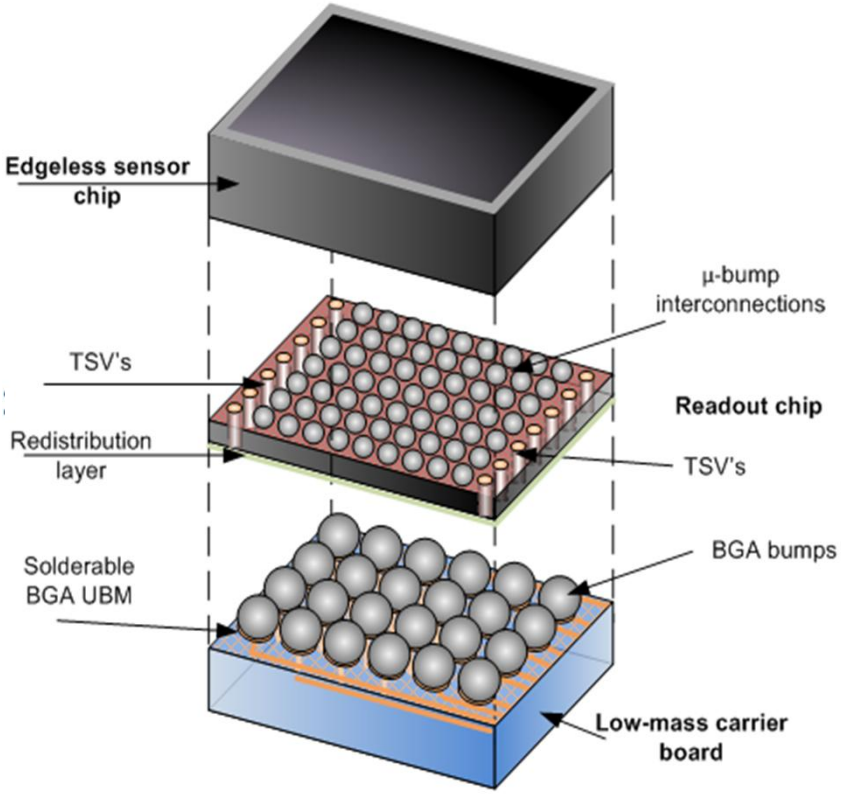
4-side Buttable Detector Module

- Detection area defined by detector geometry
- Low temperature (145 ºC) solder (InSn) technology available
- Cu Through Silicon Via (TSV) technology under development
- ENIG UBM technology available for ROCs





S. Vähänen et al., VIPS 2010

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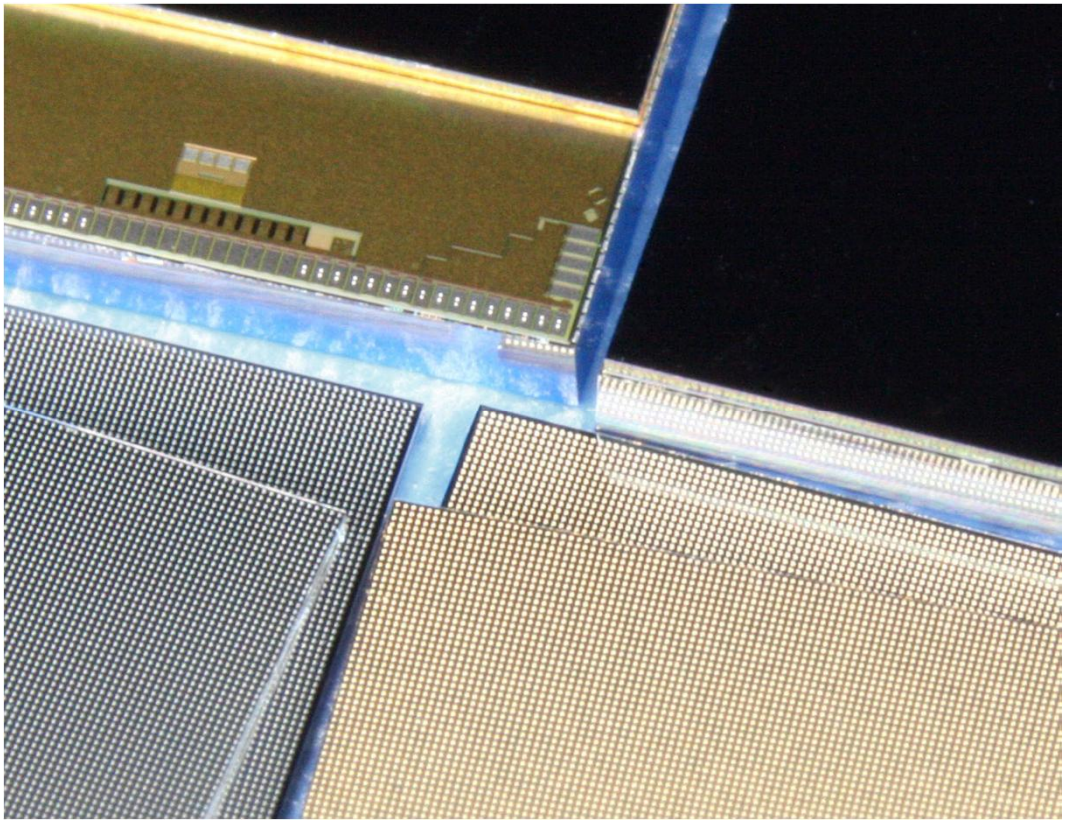
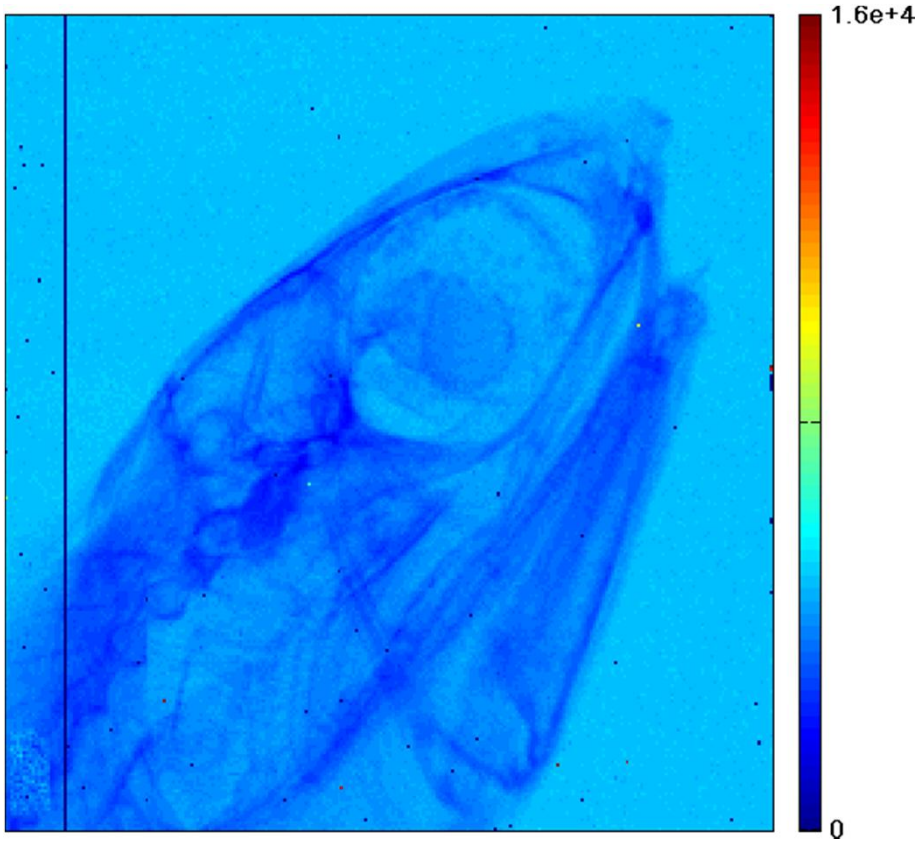


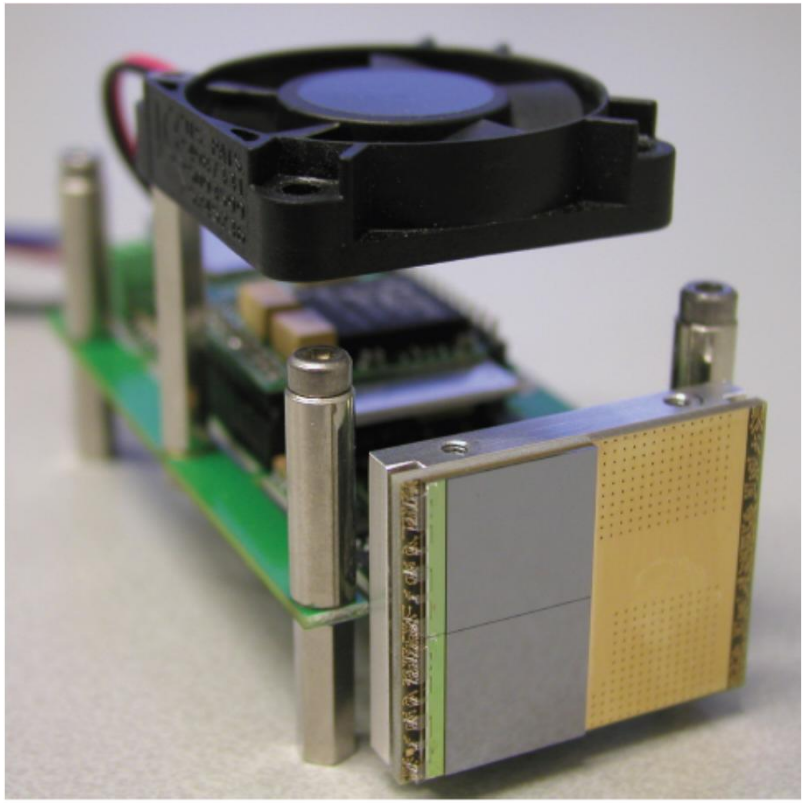
Side buttable (active edge) imaging detector modules for medical and pharmaceutical use

These imaging detectors (1.4 x 1.4 cm^2) can be tiled seamlessly to obtain large area images with high spatial resolution of ~10 µm. *Top:* packaged (flip-chip bonded) imaging detector modules, where the detector is on top (face down) and the readout chip on bottom. The readout chips here are Medipix2. *Bottom left:* active edge pixel detectors. *Bottom right:* active edge pixel detectors with under bump metallization to allow contact to the Medipix2 readout chips.

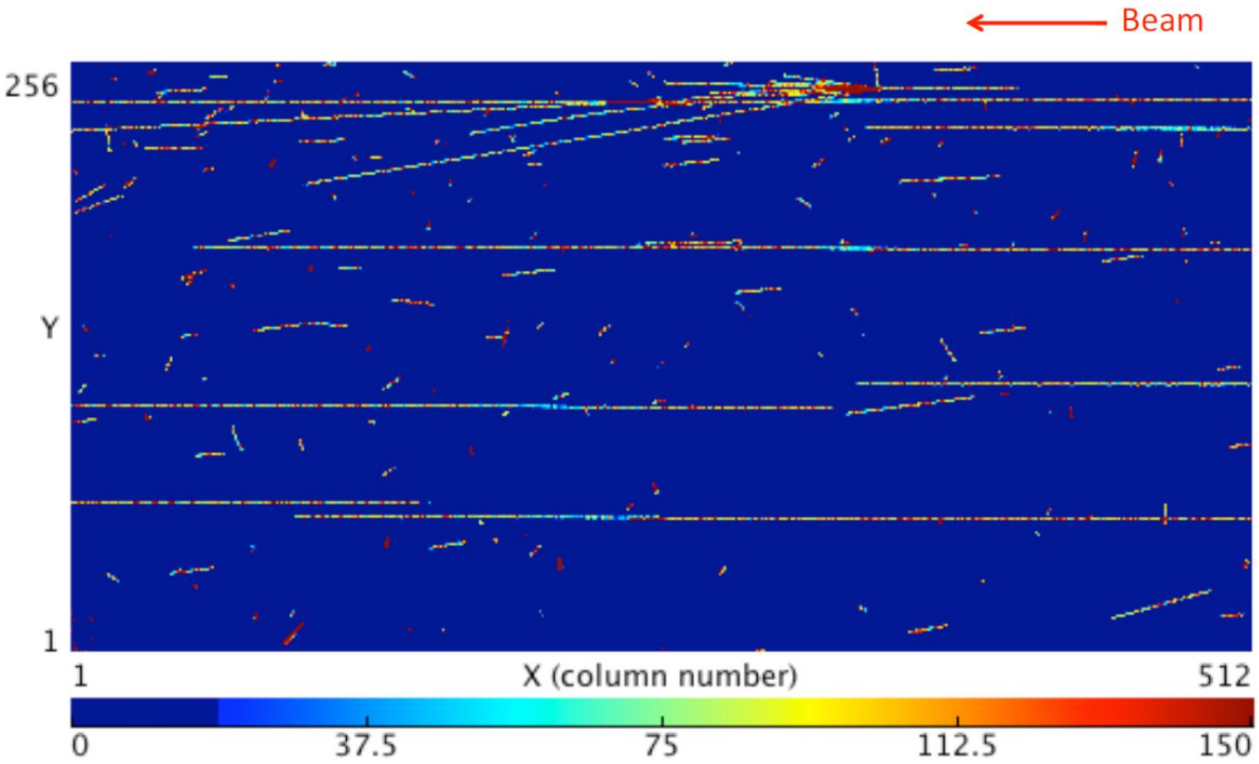


X-ray image of a small fish with active edge imaging module

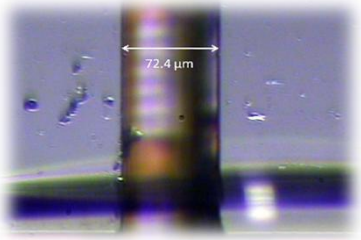
Image was taken with 20 keV X-ray tube with acquisition time of 36 s. Seamless large area images can be obtained by tiling the detectors in to matrices. [Courtesy of L. Tlustos, CERN]



Two edgeless silicon detector on a Timepix ROCs mounted and wire connected to the RELAXD readout board. Physical gap between the detector elements is about 80 µm. It is caused because the Timepix ROC has larger area than the edgeless silicon detector that is bonded to it. [Courtesy of M.Bosma]



Minimum ionizing particle tracks measured with two edgeless pixel detectors on a Timepix ROCs from 120 GeV/c^2 muons and pions at the SPS accelerator at CERN. [Courtesy of M.Bosma]



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Summary and Outlook

Summary

- VTT is a globally networked multitechnological contract research organization, with a high class cleanroom facilities and looking for partners
- Edgeless detector development at VTT
  - Edgeless detector fabrication technology is available (n-on-n, n-on-p and p-on-n)
  - Development of assembly technology for seamless detector is ongoing
  - Promising results obtained from latest processing run

Outlook

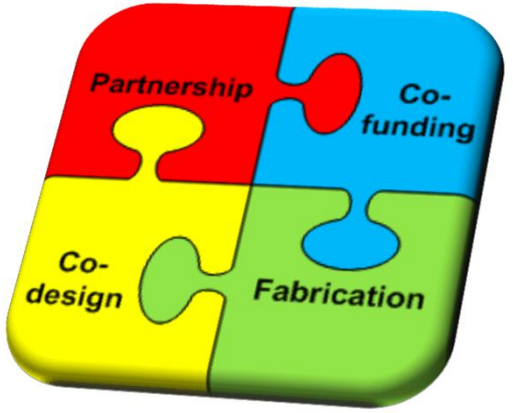
- Characterize latest p-on-n edgeless detectors
- Future processing with improved fabrication technology

Joint Pixel Detector R&D Process Run

- Motivation for an edgeless detector process run
- Batch size: 25 wafers
- Detectors can be fabricated in different thicknesses
  - 50 µm – 500 µm
- n-type & p-type wafers available
  - n-on-n (or p-on-n) configuration
  - n-on-p configuration
- Varied layout – guard structures, active edge distance from pixels optimized with the ROC cutline, etc.
- Under bump metallization and flip chip assembly in-house
- Work will be done on best effort basis

Invitation for partnership

- Individual partner could join the edgeless R&D run with 15-20 k€ contribution
- Partners can contribute to
  - Wafer layout (6” wafer)
  - Wafer type selection
  - Thickness of detectors



- Partner provides
  - Bumped readout chips according to their preference
  - Delivers readout wafer or chips and organizes a bumping run at VTT
- Deliverables: 15-20 edgeless assemblies per partner
- Possibility for additional assemblies on demand
- Interested? Contact Juha.kalliopuska@vtt.fi & Sami.vahanen@vtt.fi

Thanks for your attention!

Q&A