Laser-Scribing and Al_2O_3 Sidewall Passivation of P-Type Sensors

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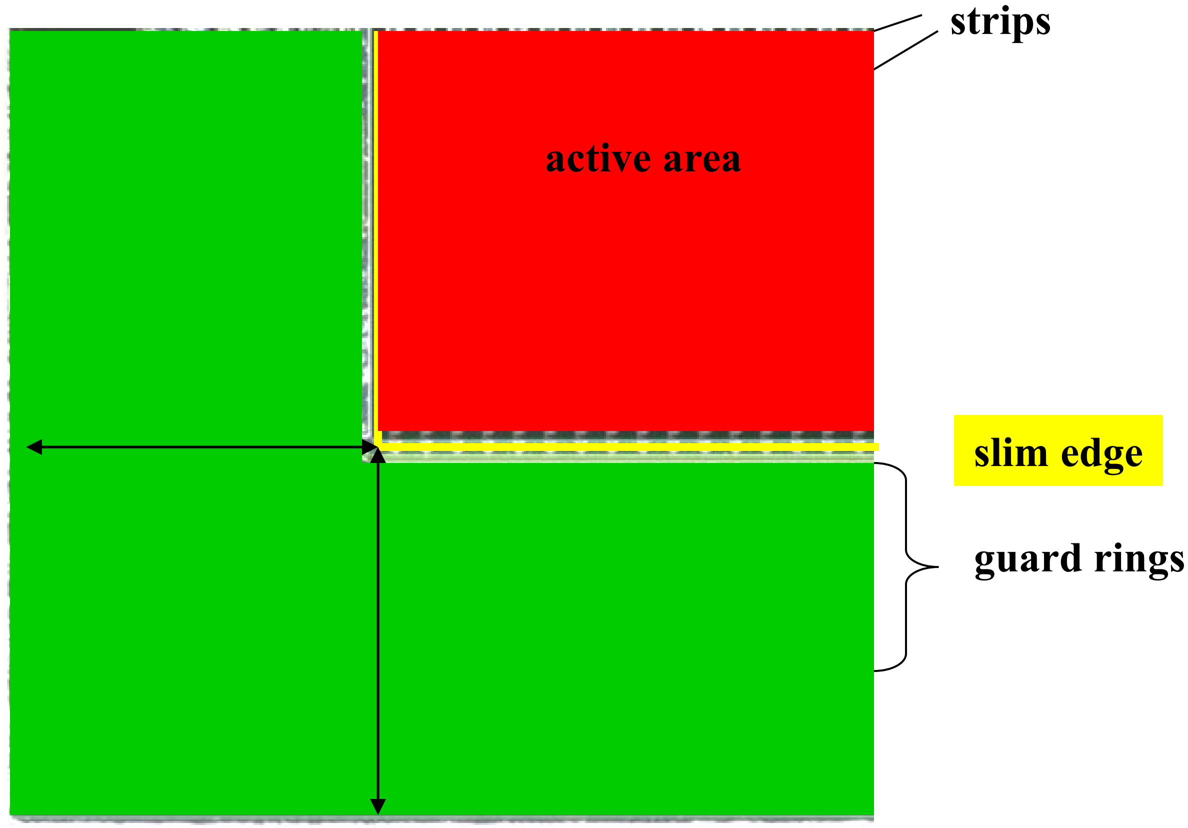
Outline

- Slim Edges – Motivation and Approaches
- Laser-Scribing and Cleaving
- Results for N-Type Sensors
  - Laser Parameters
  - IV Curves for N-Type Sensors
- Results for P-Type Sensors
  - Alumina for P-Type Silicon Passivation
  - Introduction into Atomic Layer Deposition (ALD)
  - Silvaco Simulations for P-Type sensors
  - IV Curves for P-Type Diodes with Alumina Passivation
- Conclusions and Outlook

Motivation – Slim Edges

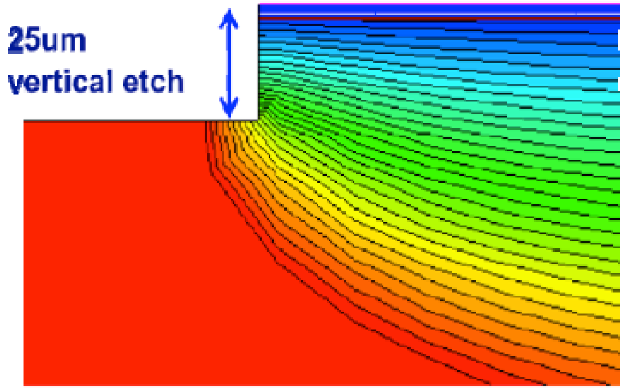


Optical micrograph

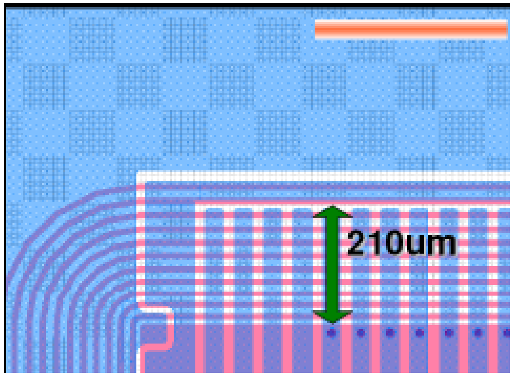
Slim edges offer:

- better tiling of sensors (especially for imaging applications)
- reduced inactive area

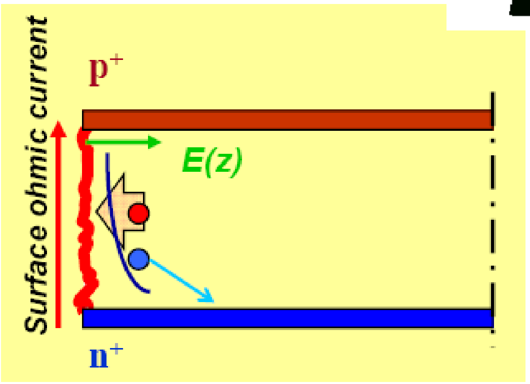
Slim Edges - Approaches



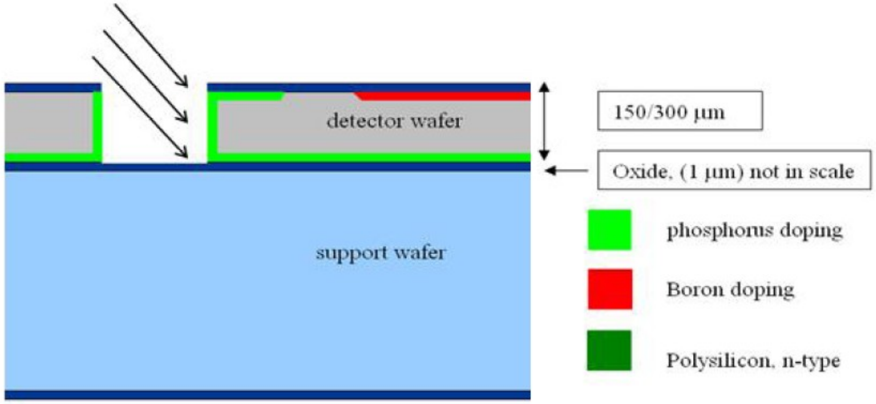
J. D. Segal, et al., NSS 2010



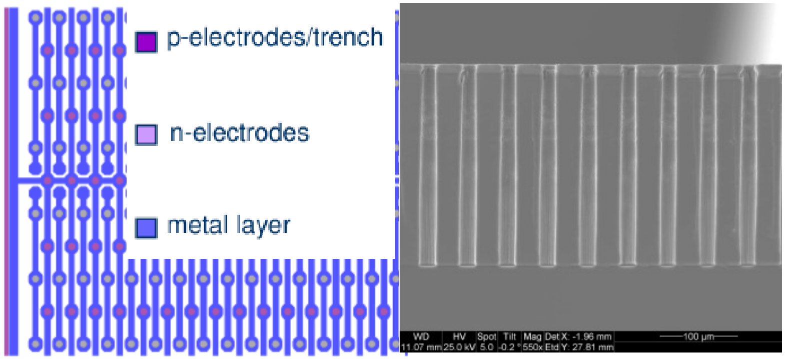
A. Rummler et al., 2010



E. Verbitskaya et al., 13 RD 50 workshop, 2008



J. Kalliopuska, NSS 2010



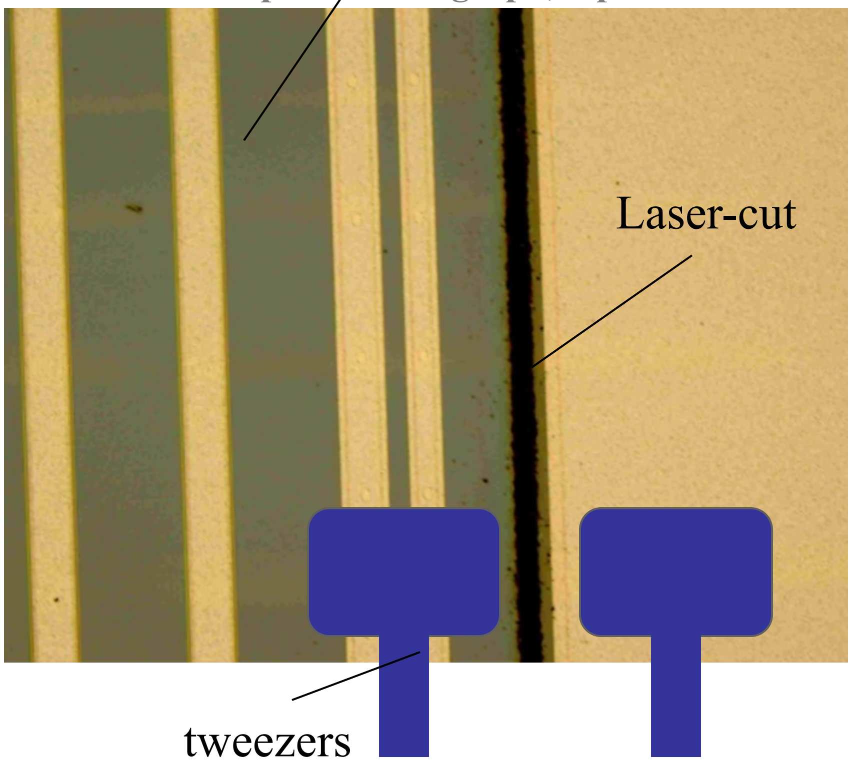
T.-E. Hansen et al., 2009

Goal of our research:
- **slim edges with finished devices on die level**
- **slim edges on p- and n-type devices**

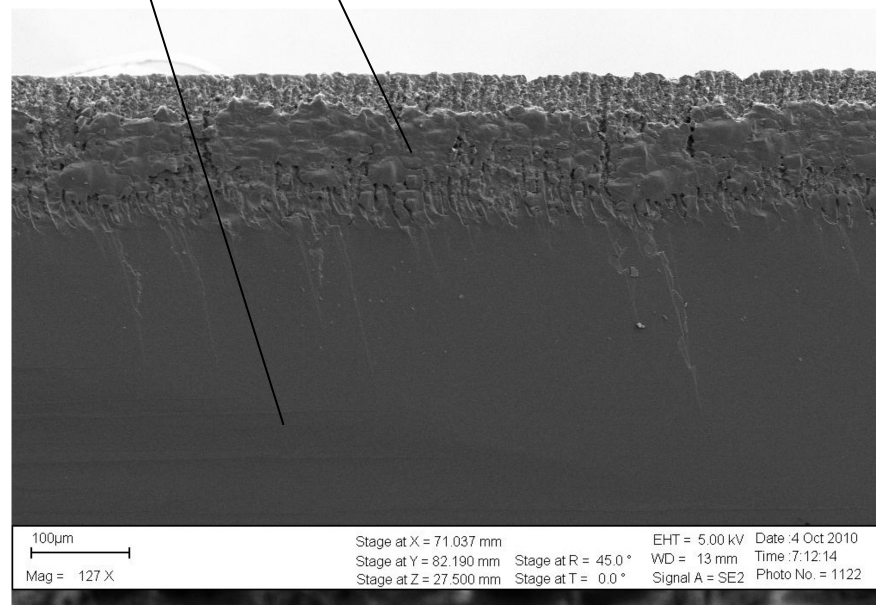
Laser-Scribing and Cleaving

- used finished dies (post-processing)
- laser scribing → laser-damage
- cleaving → no damage

Optical micrograph, top-view



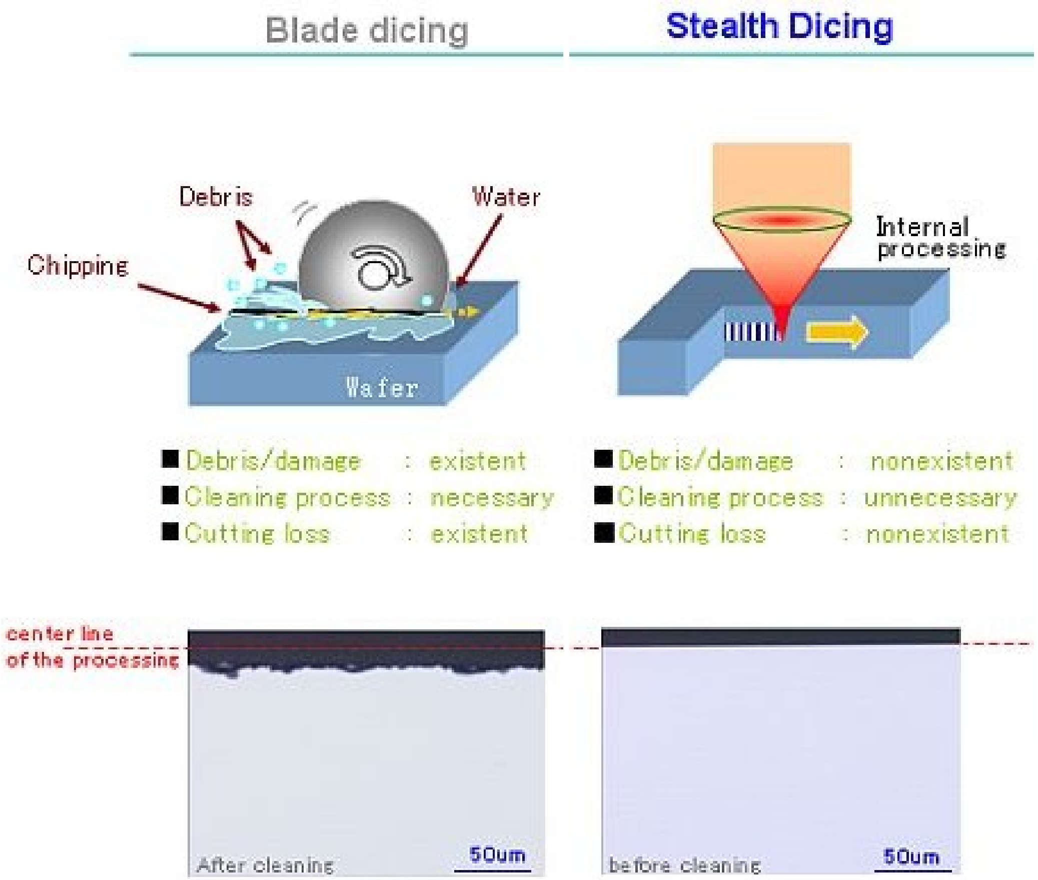
SEM micrograph, cross-section



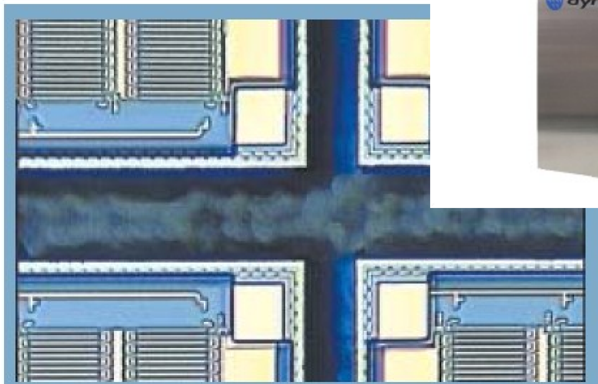
Laser-scribing done at U.S. Naval Research Laboratory using an Oxford Laser Instruments E-Series tool. Breaking done by hand using tweezers, but can be done fully automatic, see next slide.

Industrial Applications of Laser-Scribing & Cleaving

Dynatex International DTX-200-AB
AUTOMATED BREAKER PRODUCTION SYSTEM



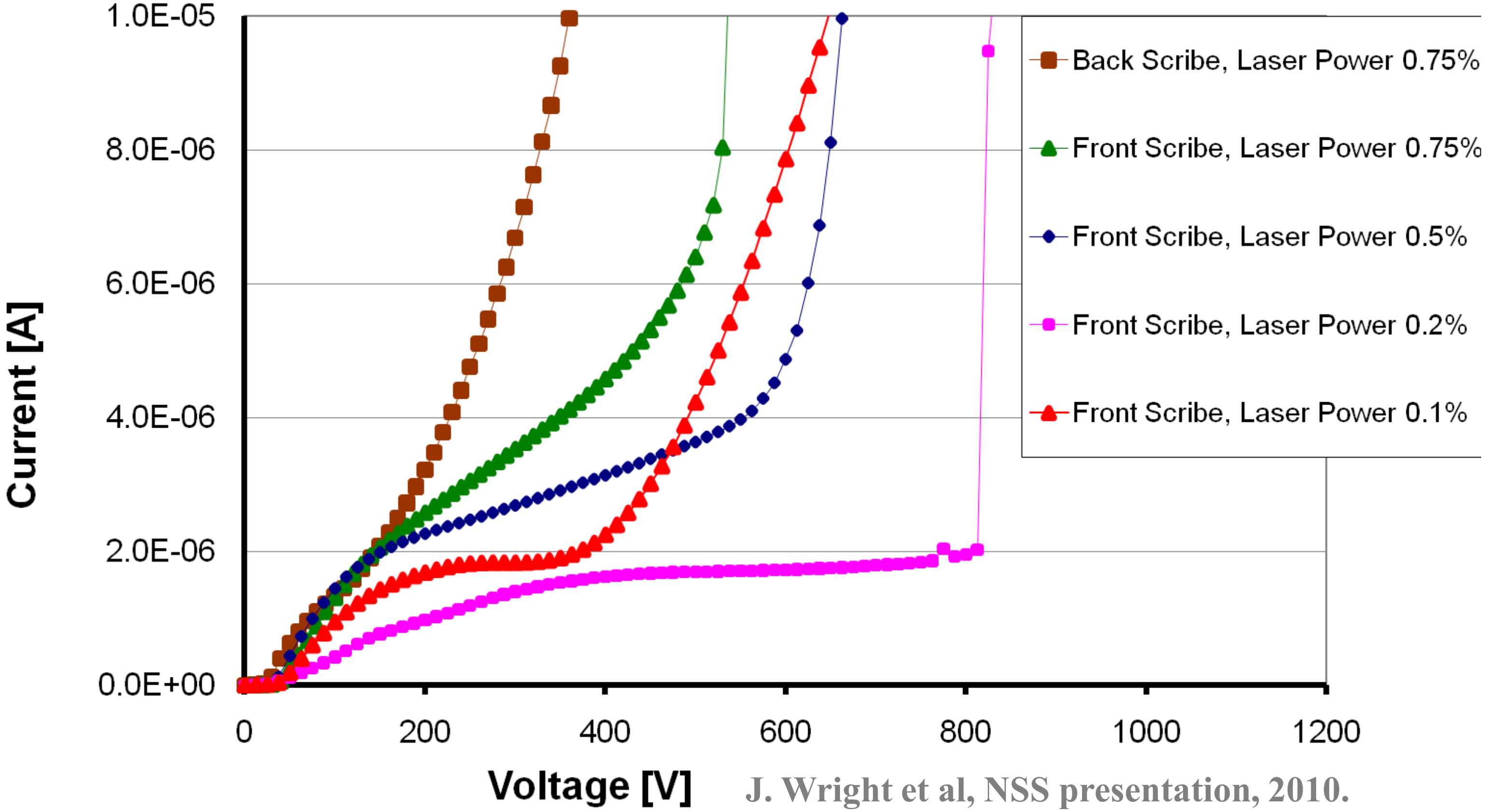
HAMAMATSU



GaAs wafer, diced and expanded. Wafer dicing is well-suited for UV DPSS lasers with their highly focusable, pinpoint-bright beams

- laser-scribing and cleaving common in LED industry
- automated tools for scribing and breaking of devices on wafer-scale

N-Type Sensor Results – NSS 2010

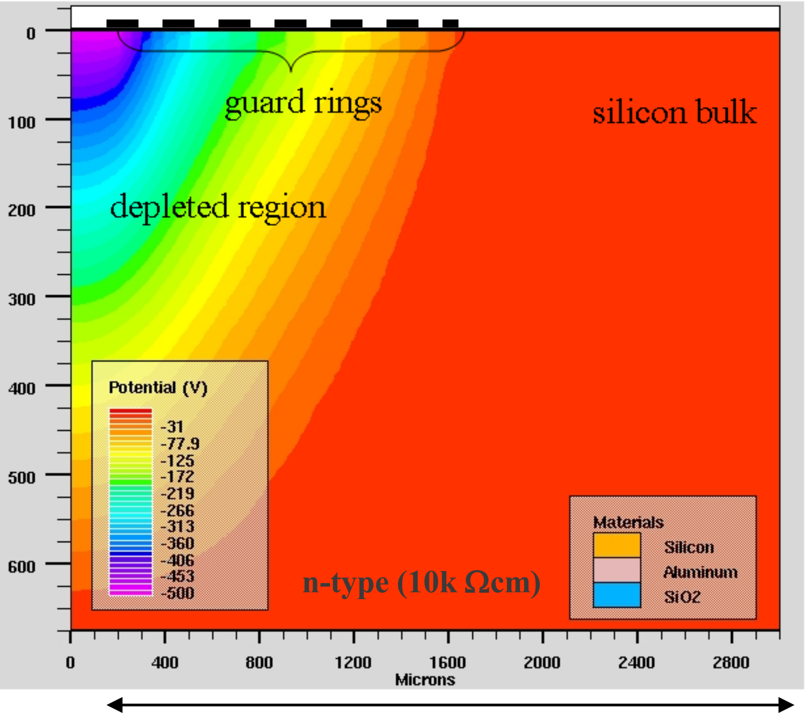


J. Wright et al, NSS presentation, 2010.

- scribe at 100 um from the guard ring.
- front-side scribe seems to be preferential to back-side one.
- lower laser power is preferential.

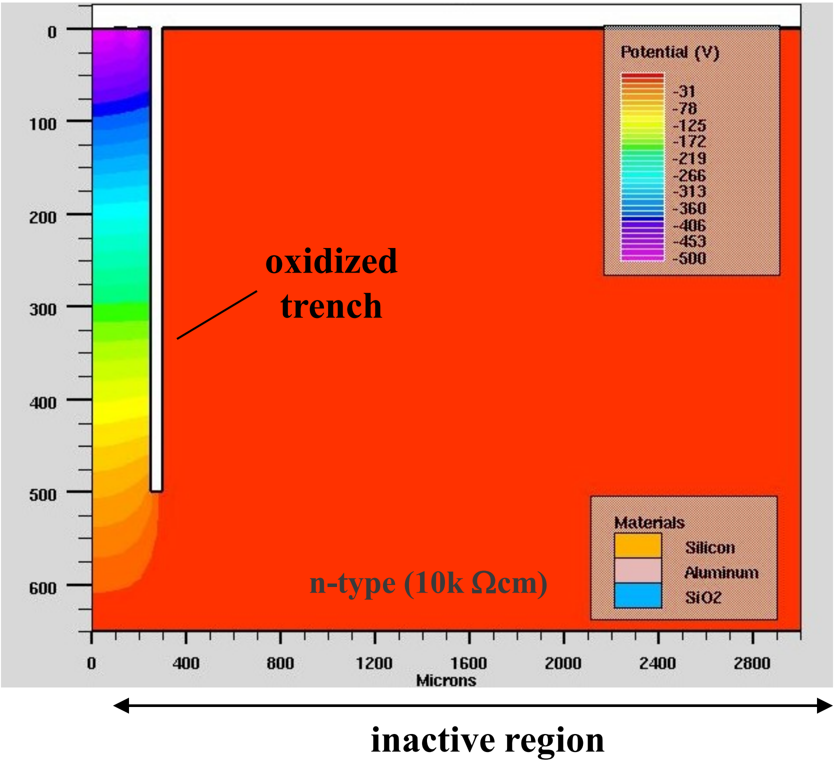
How Do We Establish Controlled Potential Drop?

Silvaco simulations



Guard rings used to ..
• reduce effects of dicing, ☑
• control potential drop toward the cut edge. ☑

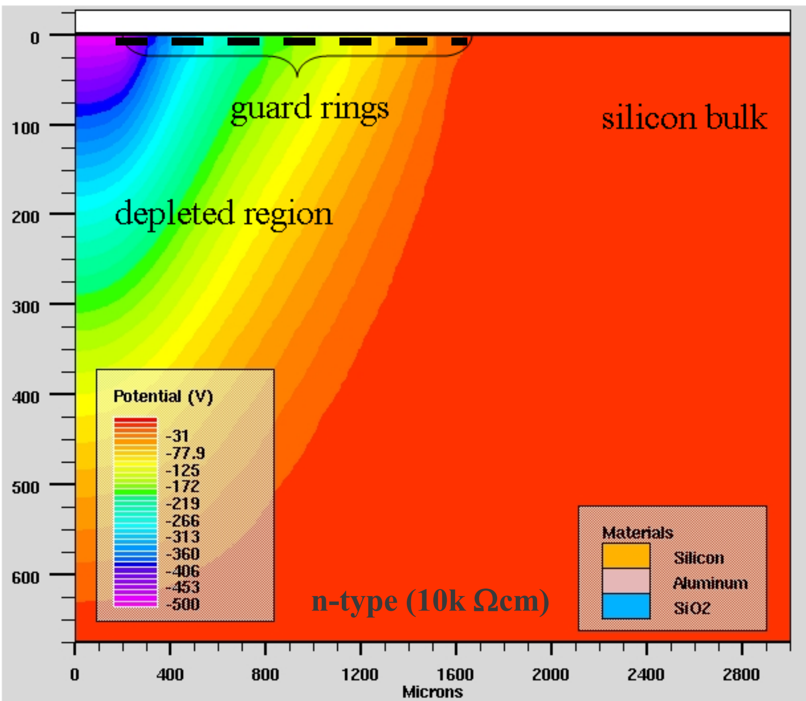
How Do We Establish Controlled Potential Drop? N-Typ Si



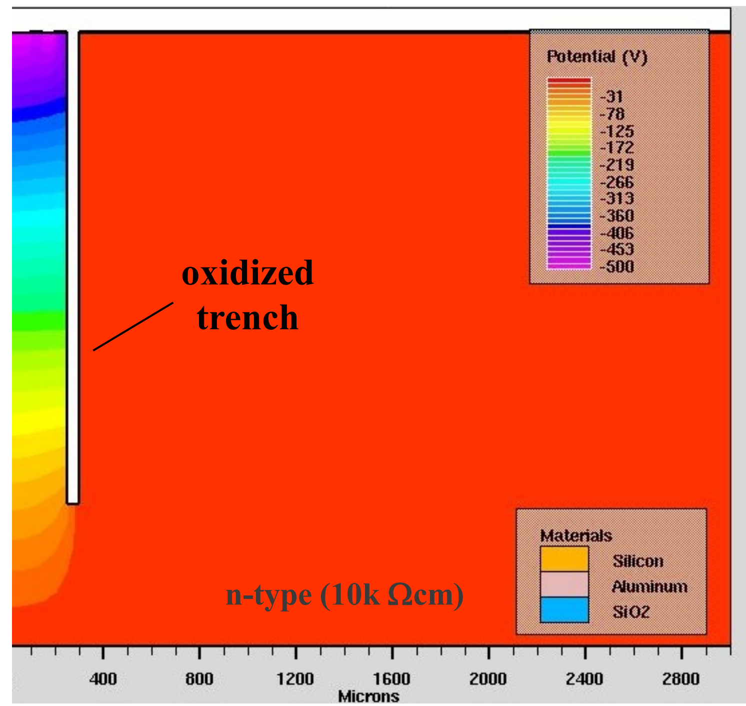
A passivated trench with a thermally grown oxide (**positive** charge density 10^{11} cm^{-2}) trench will lead to:

- control potential drop toward the cut edge, ☺
- protection from saw cut edge. ☺

How Do We Establish Controlled Potential Drop? N-Typ Si

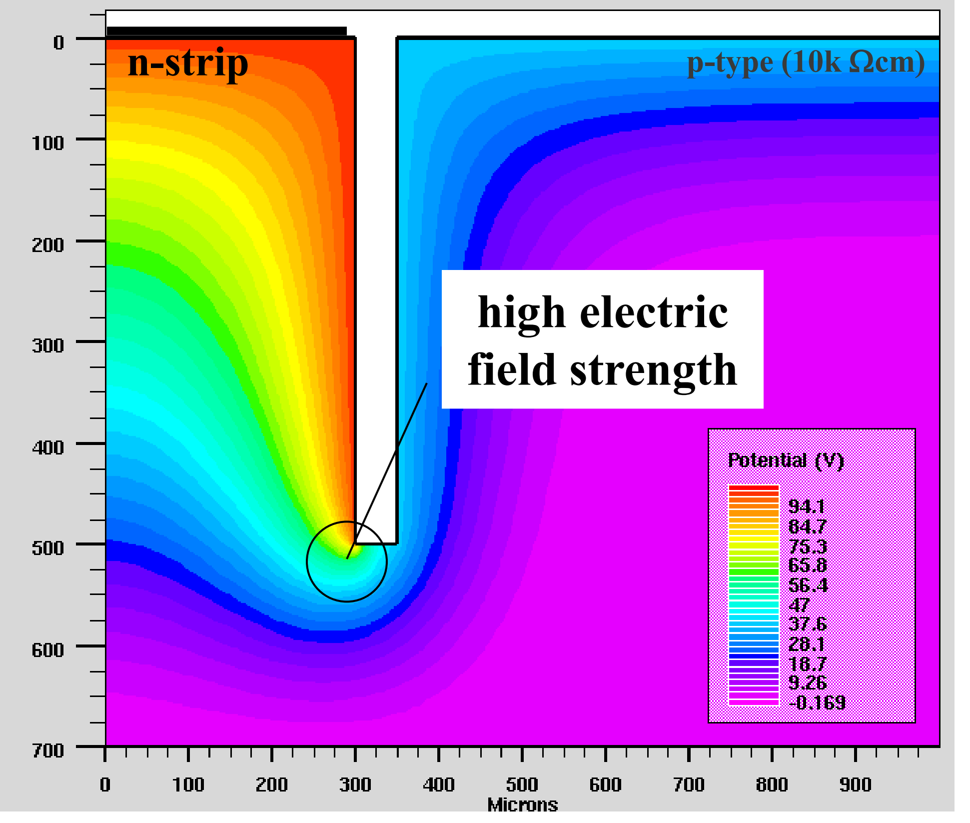


inactive region



inactive region

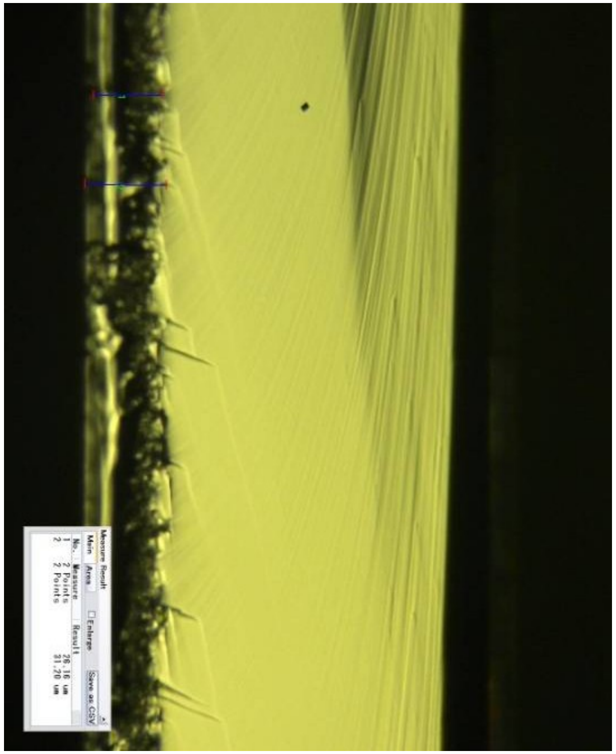
Oxidized Trench for P-Type Si



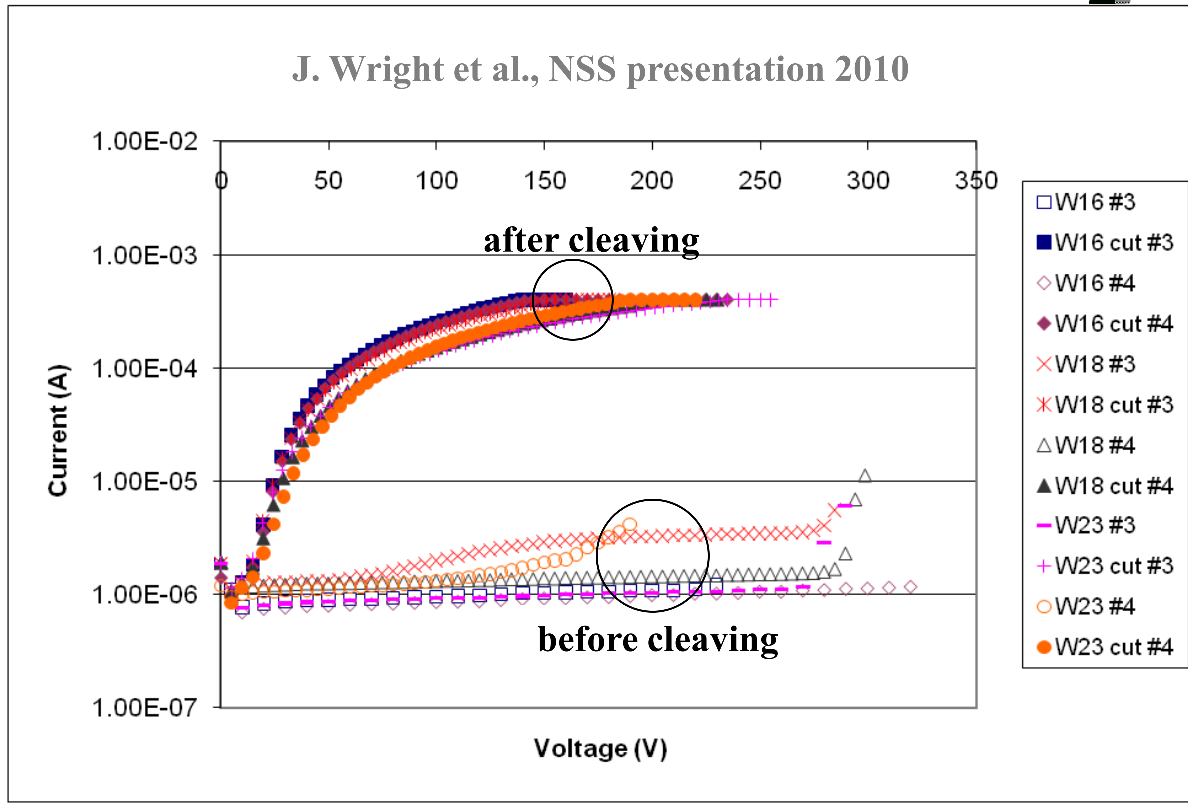
An oxidized trench leads to:

- high electric field at trench edge,
- no control potential drop toward the cut edge,
- no protection from saw cut edge.

P-Type Sensor – NSS 2010 Presentation

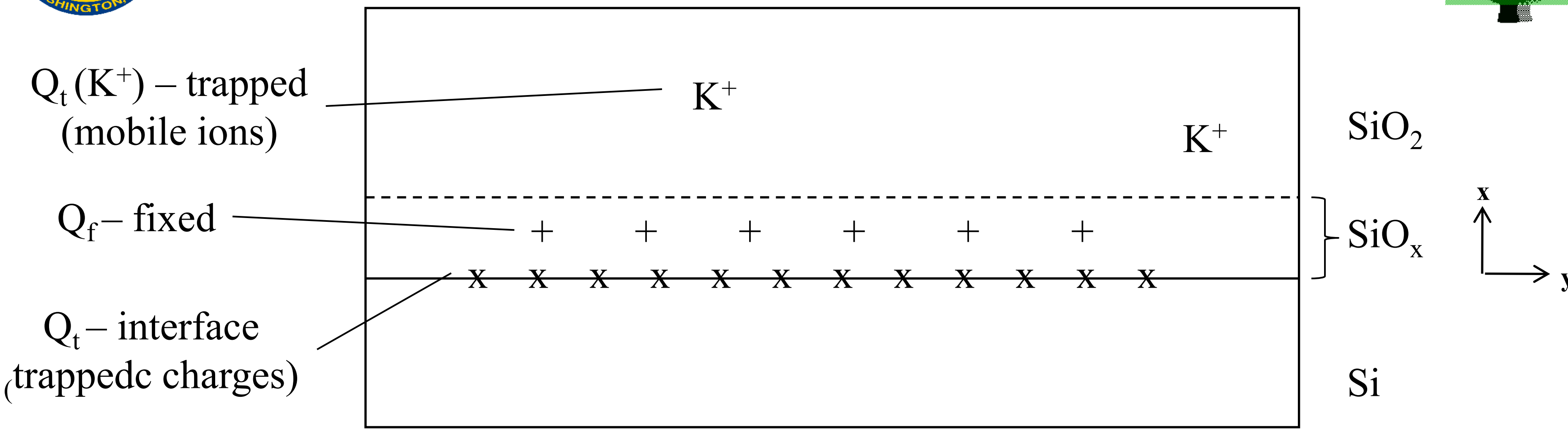


Optical micrograph, cross-section



- Some of the sensors showed a relatively early breakdown voltages of 200/300 V before the procedure.
- Processed sensors show a uniform early breakdown at ~20 V.
- We also tested Micron and HPK p-type sensors.

SiO_2 – Si Interface Charges



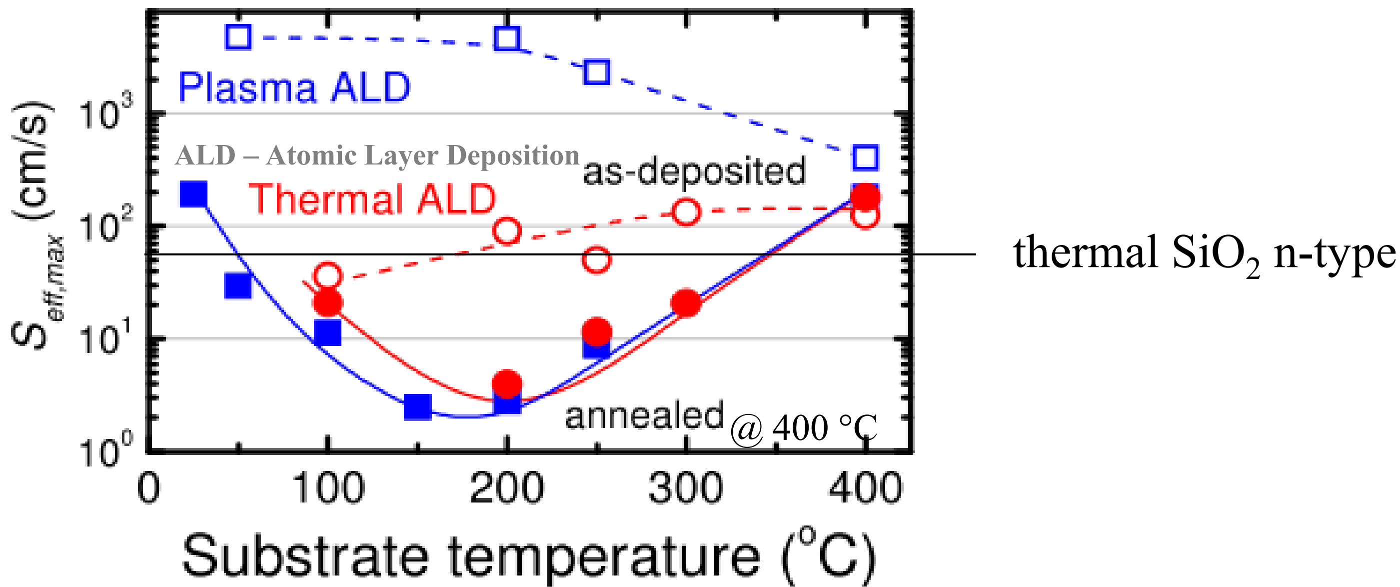
"*Origin*" of excellent passivation for **n-type Si:**

-Thermally grown oxides typically have from ~ 10^{10} to 1-2x10^{11} **positive** charges per cm^2, localized within about 35 Å of the Si/SiO_2 interface [Silicon Processing for the VLSI Era (Vol I), S. Wolf and R. Tauber, Lattice Press 1986, p. 223].

- surface recombination rate: FZ n-type Si (10 Ωcm): ~ 60 cm/s

Negative Surface Charge for P-Type Passivation

Surface recombination rate for FZ p-type Si (2 Ωcm), Al_2O_3 passivation



Data from G. Dingemans, et al., 35th IEEE PVSC 2010.

- low recombination rate after Al_2O_3 passivation → high carrier life time
- detector material kΩcm → higher life times
- fixed ***negative*** interface charge
- low temperature process (< 400 °C)
- standard process in solar cell industry

Negative interface charge enables effective surface passivation for p-type Si.

Values for surface recombination rate and charge density for Al_2O_3 /p-type Si are comparable to SiO_2/n-type Si.

Introduction - ALD

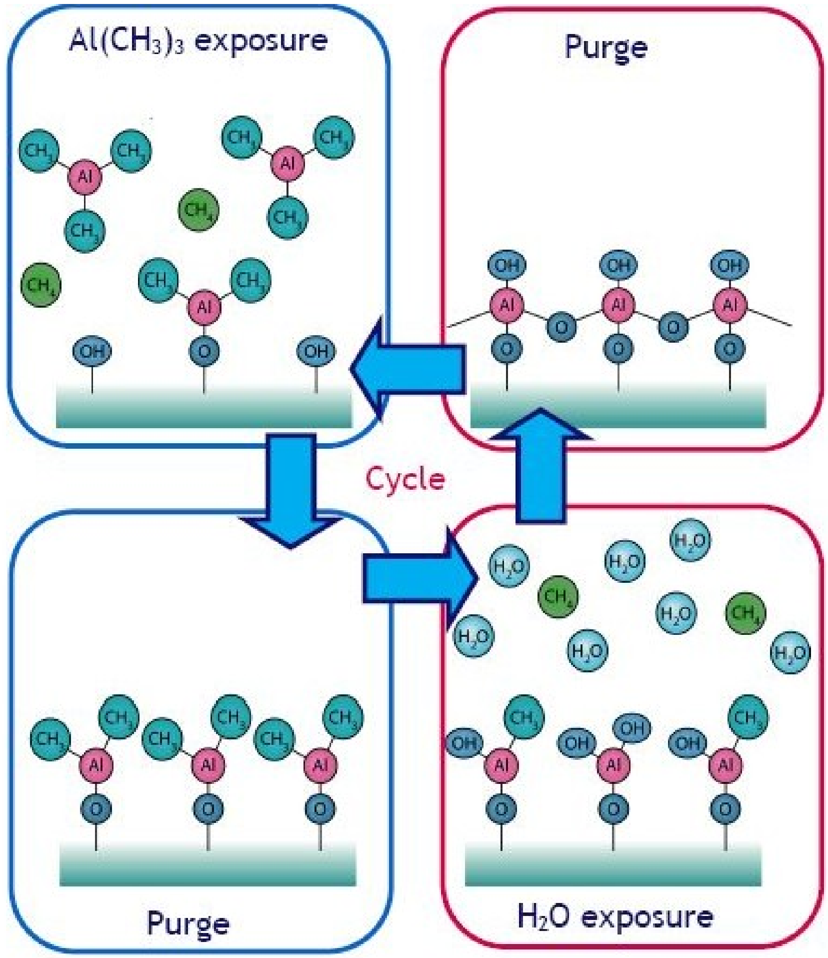
- Similar in chemistry to CVD (chemical vapor deposition), except that the ALD (**atomic layer deposition**) reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction.
- ALD film growth is **self-limited and based on surface reactions**, which makes achieving atomic scale deposition control possible.
- Perfect 3-D conformality, 100% step coverage: uniform coatings on flat, inside porous and around particle samples.

- **Origin of negative interface charge**: Functional surface groups on the silicon wafer are not optimal for an adsorption of the TMA (trimethylaluminium) precursor molecules, which leads to an incomplete reaction of the TMA and, consequently, an increased relative oxygen concentration at the interface (F. Werner et al., 25th European Photovoltaic Solar Energy Conference, Valencia, Spain, 6-10 September 2010).

U.S. Naval Research Laboratory's FlexAL®

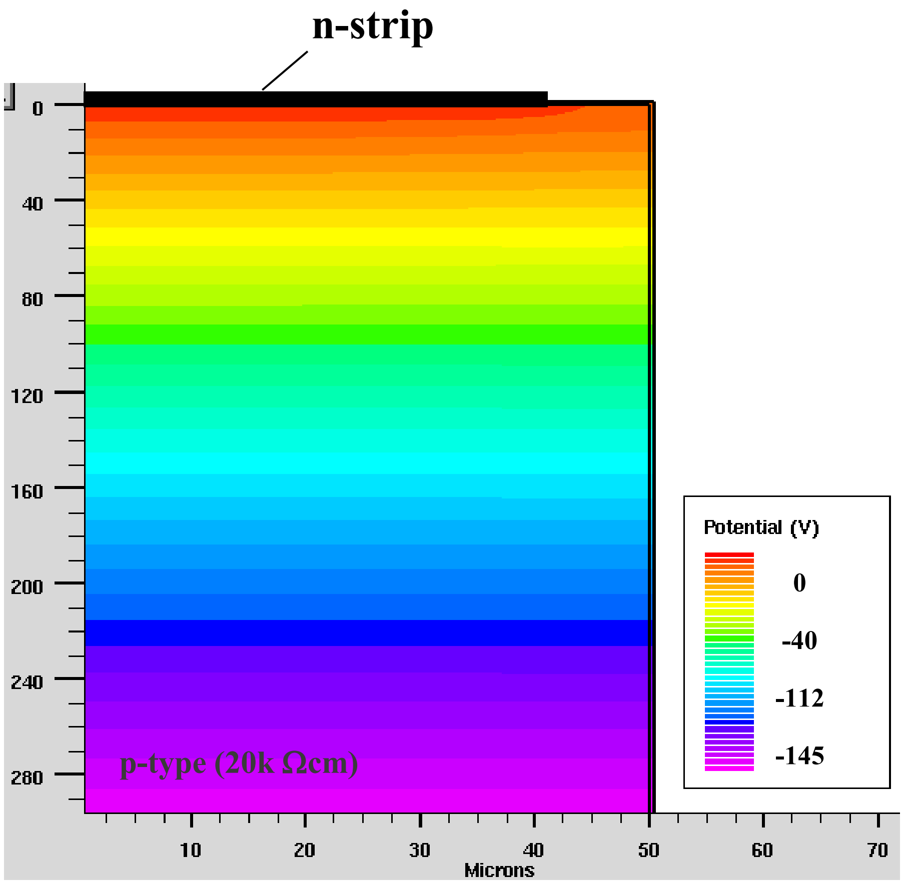
- FlexAL® from Oxford Instruments.
- plasma & thermal ALD in one flexible tool.
- stage temperature: 100 – 400 ºC.
- installed at NRL's Nanoscience Institute.

Alumina ALD Deposition Cycle



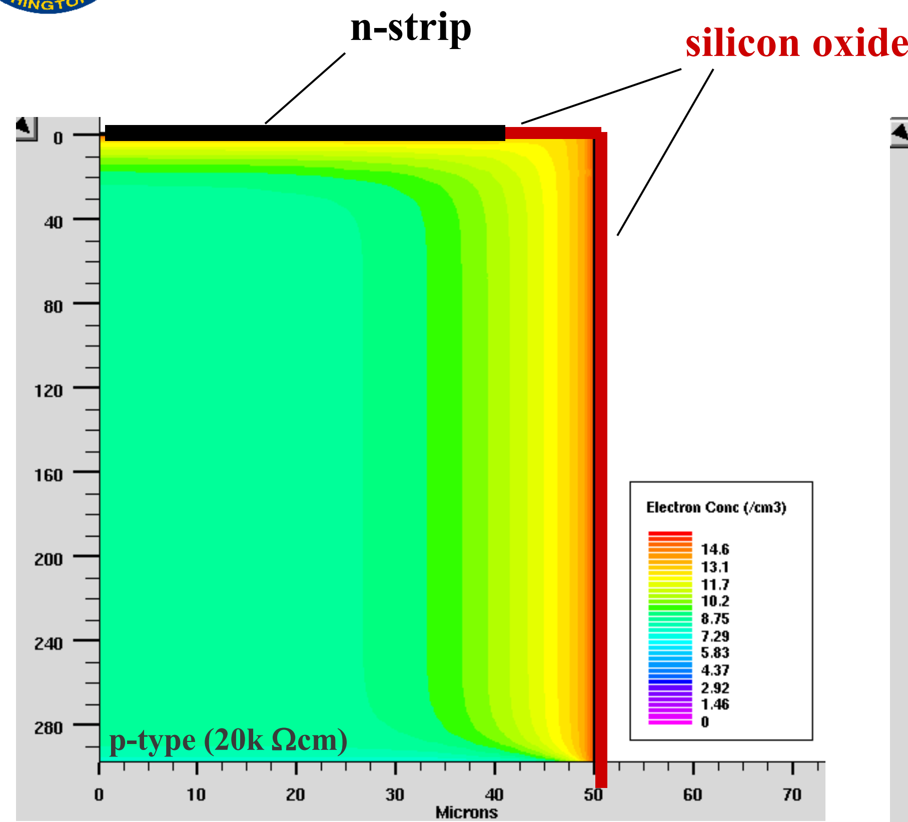
ALD Growth of Al_2O_3 from $Al(CH_3)_3$ and H_2O

Potential Distribution Without Surface Charge

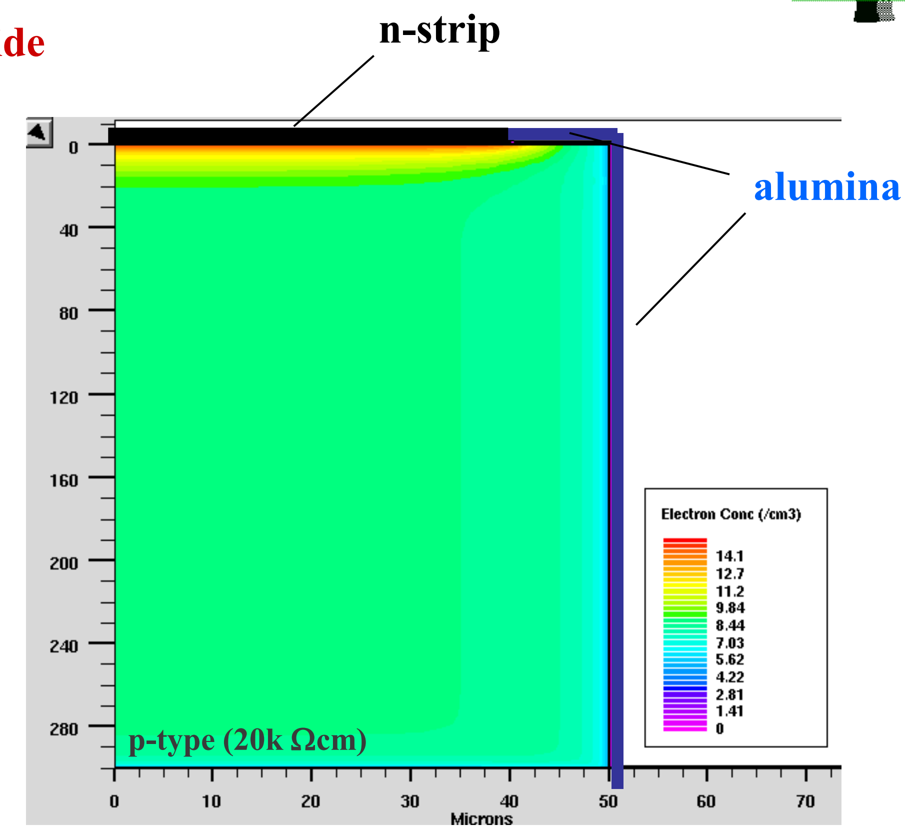


Not considering surface charges leads to *wrong* potential distribution at sidewall.

Equilibrium Electron-Concentrations for SiO_2 and Al_2O_3



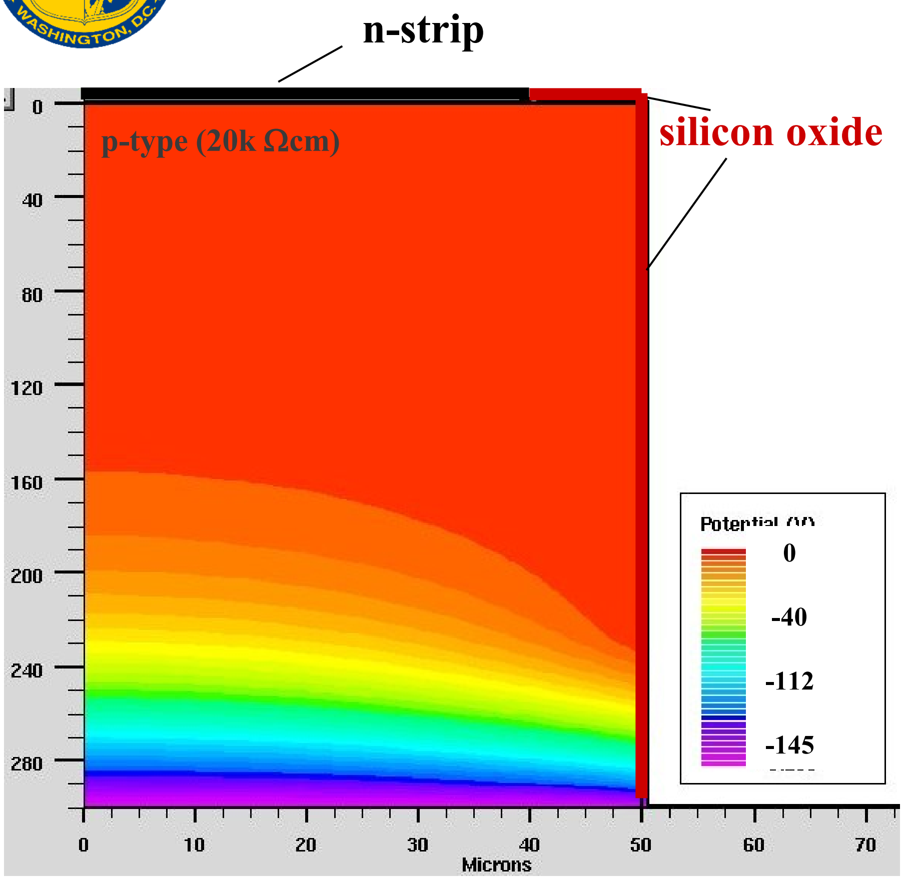
Positive charge (+1E11 cm^{-2}), no bias (V=0)



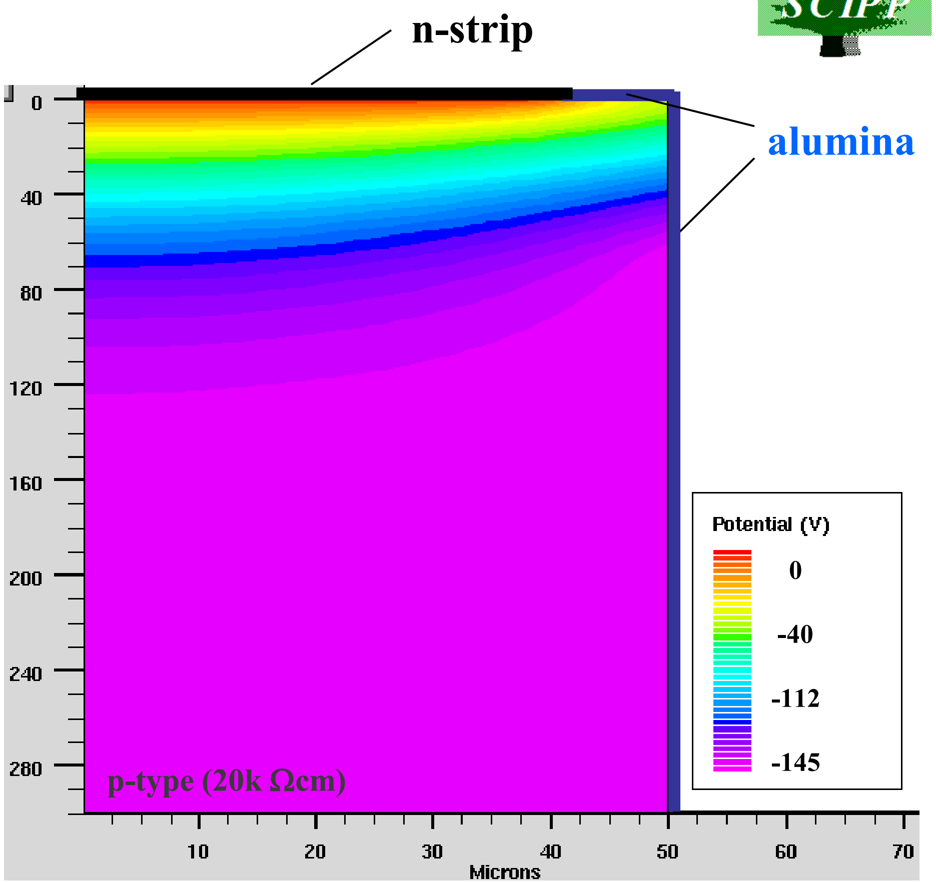
Negative charge (-1E11 cm^{-2}), no bias (V=0)

- silicon oxide ➡ electrons path from n-strip to sidewall ☹
- alumina ➡ electrons “pushed away” from sidewall 😮

Potential Distributions for SiO_2 and Al_2O_3 Passivation



Positive charge (+1E11 cm^{-2})

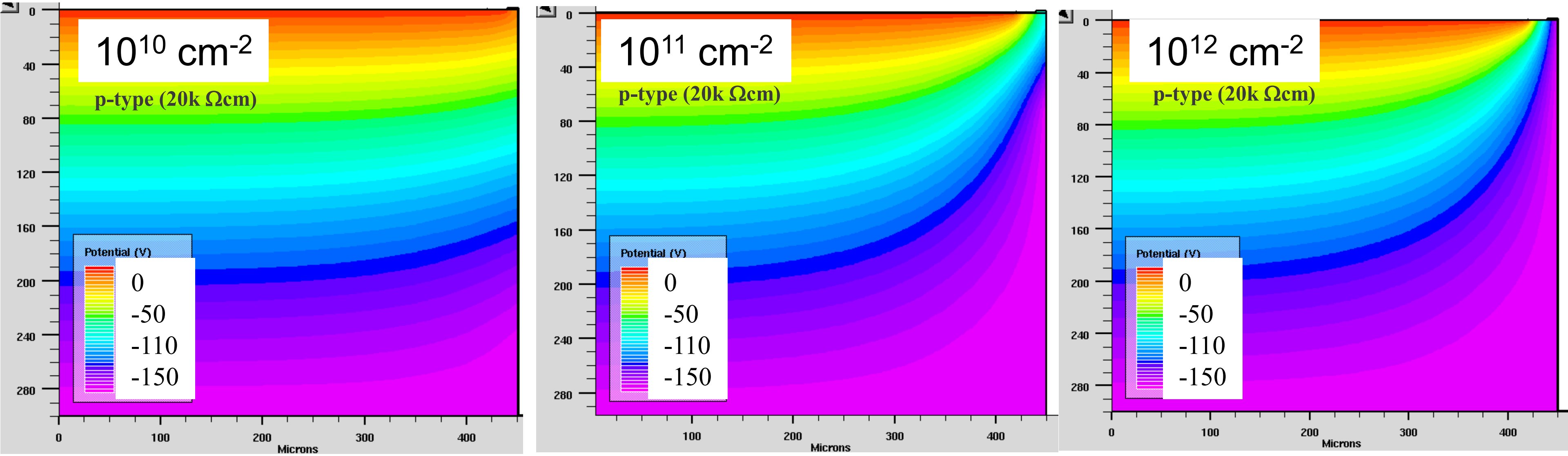


Negative charge (-1E11 cm^{-2})

Oxide passivation leads to:
- high electric field at trench edge,
- no control potential drop towards the cut edge

Alumina passivation leads to:
- high electric field strip edge,
- partially controlled potential drop towards the cut edge.

Influence of Surface Charge Concentration: P-Si/Al_2O_3

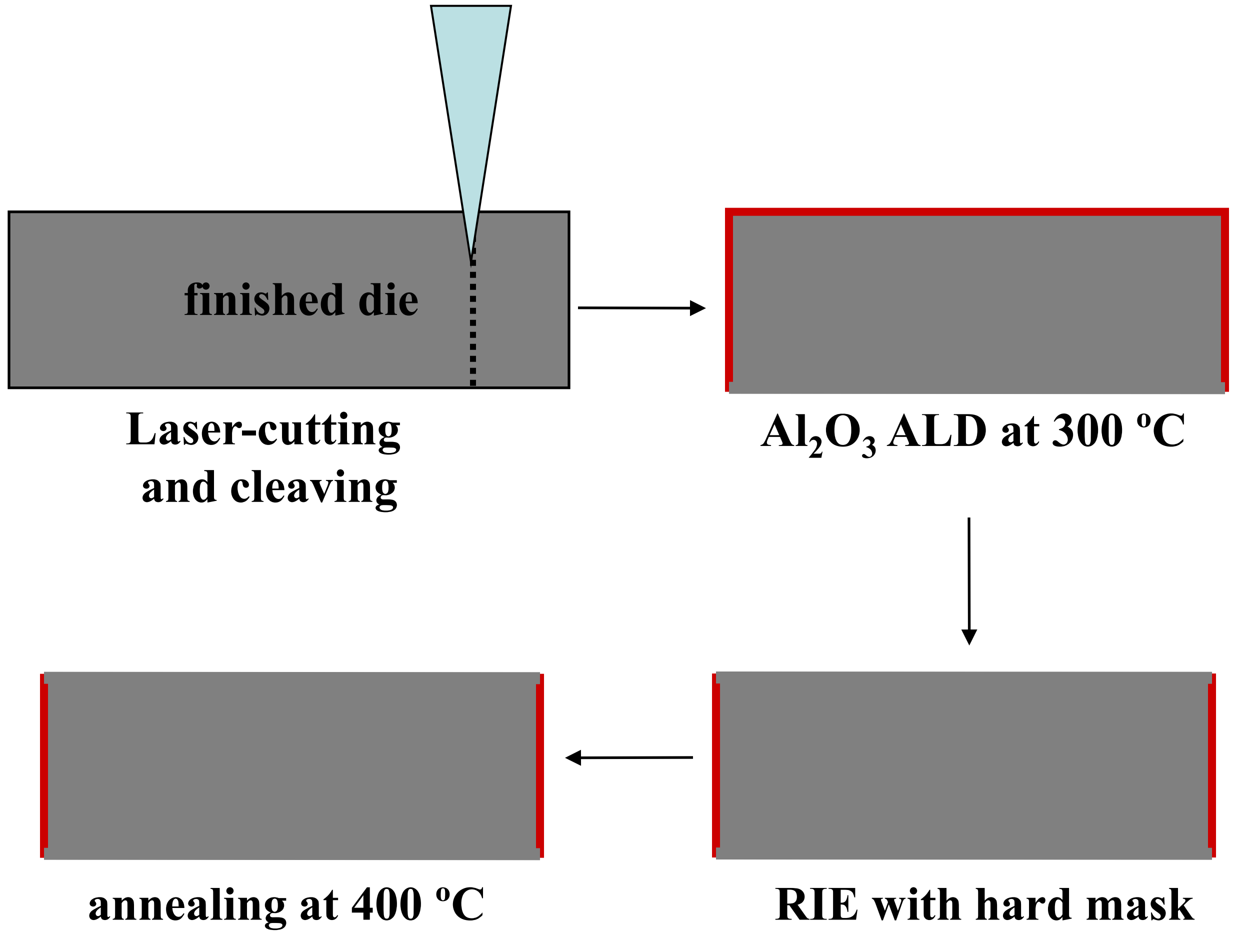


increasing negative surface charge

Typical literature values for alumina are ~ $10^{11} – 10^{13}$ cm^{-2} depending on deposition conditions. BUT most research is focused on increasing (*not decreasing)* surface charge.

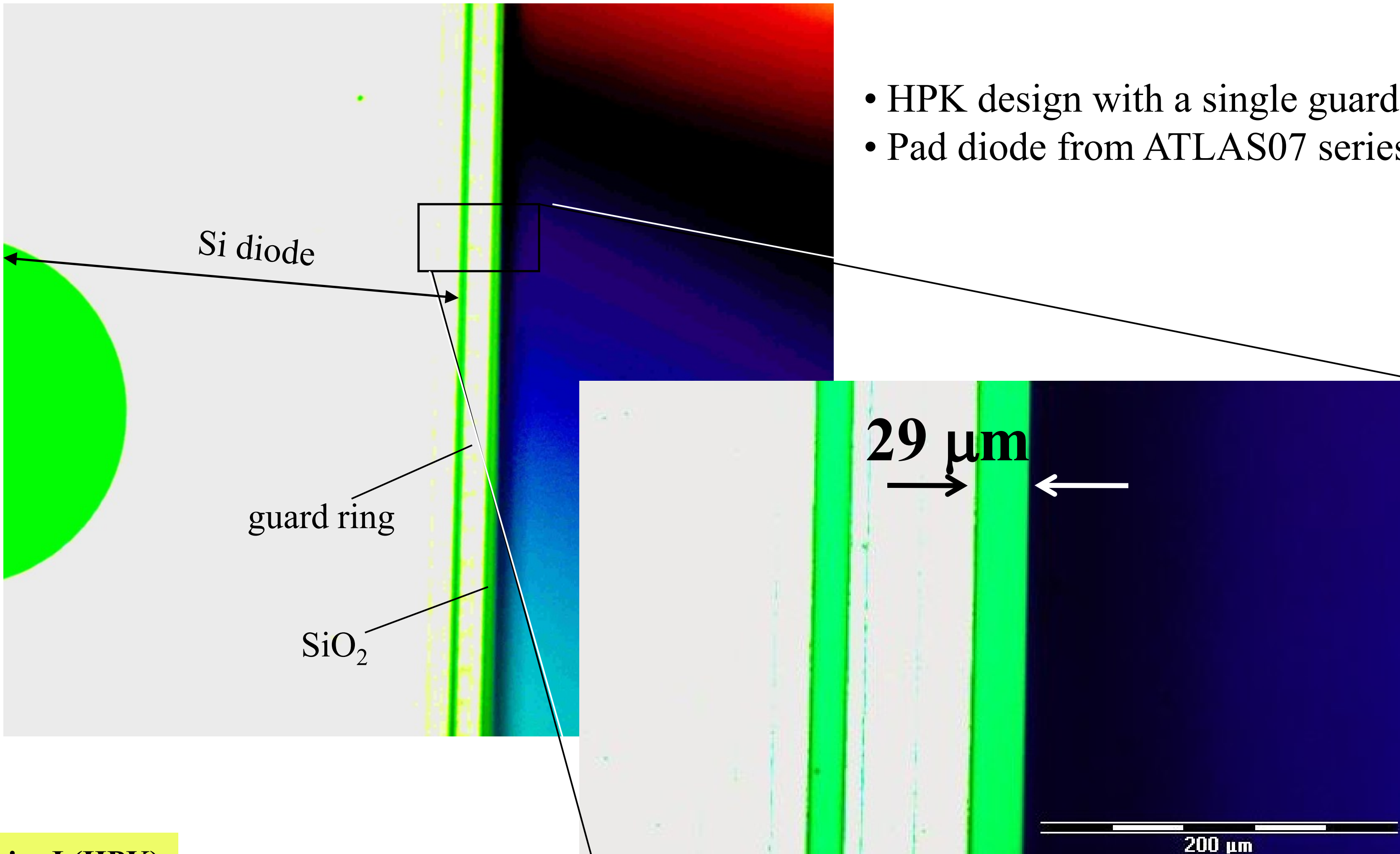
The potential drop at edge depends strongly on surface charge density.

Fabrication Sequence



ALD Passivation for P-Type Silicon

Optical micrograph, top-view

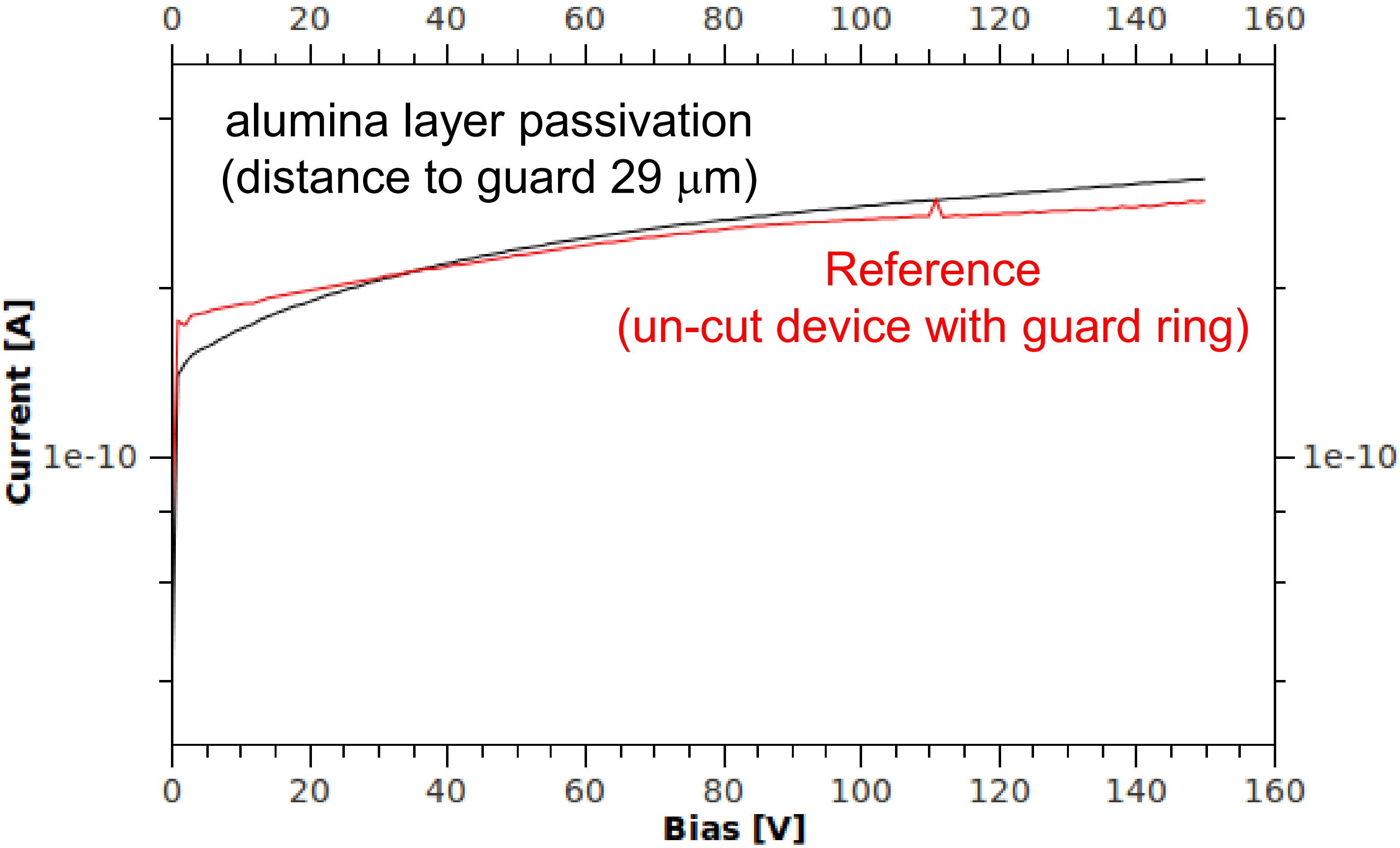


Optical micrograph, top-view

- HPK design with a single guard ring.
- Pad diode from ATLAS07 series.

Device I (HPK)

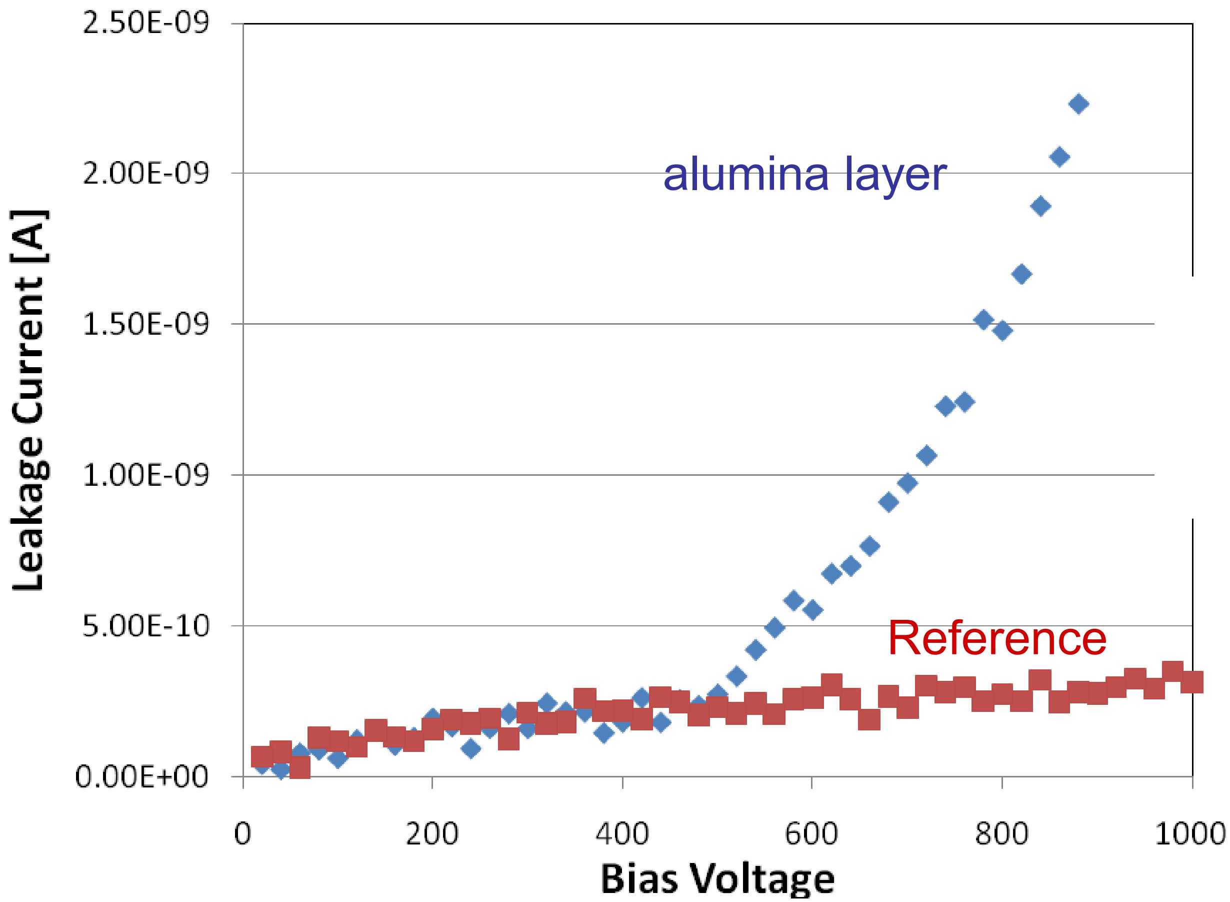
ALD Alumina Passivation for P-Type Silicon



Leakage for sample with Al_2O_3 passivation comparable to un-cut device with full guard ring structure.

Device I (HPK)

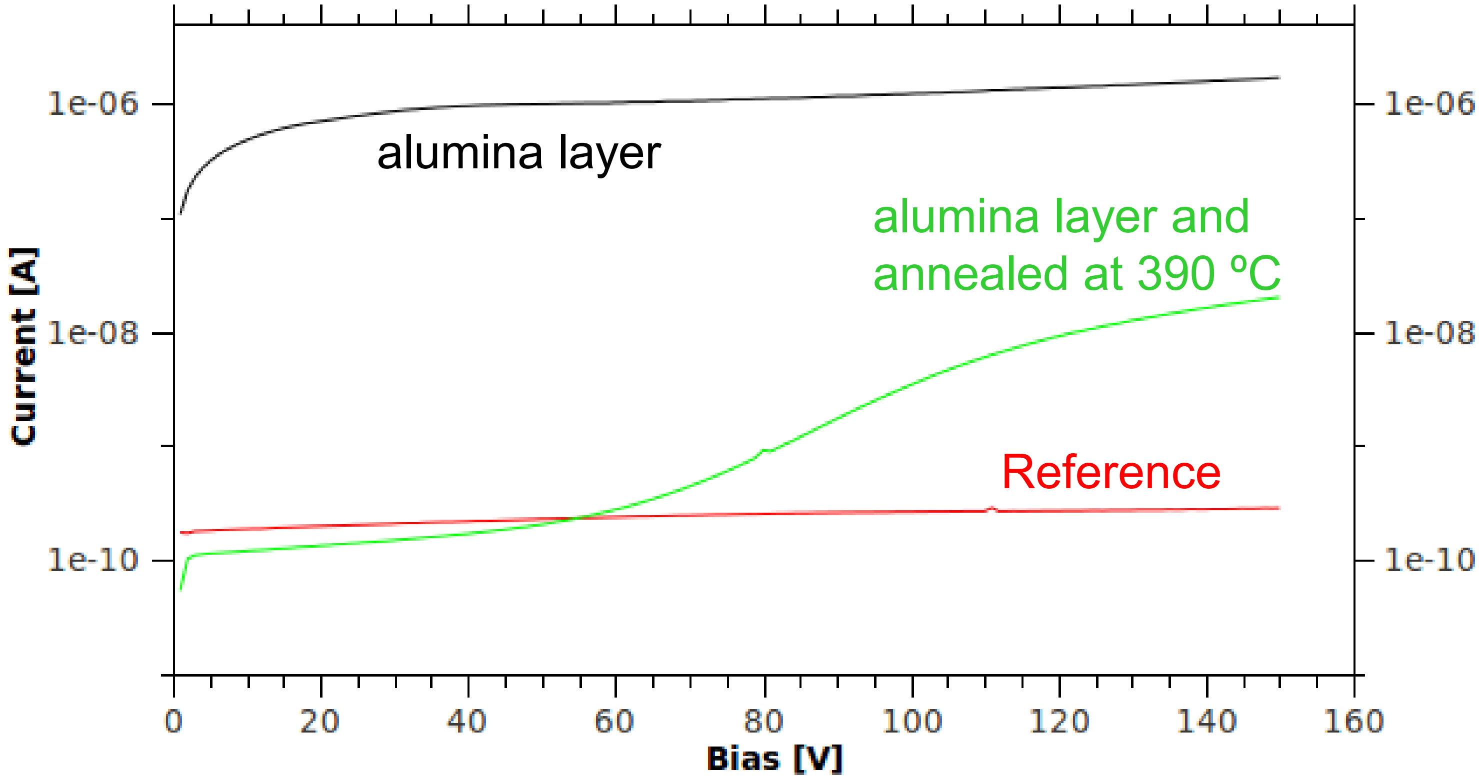
Low Leakage Currents up to 1,000 V



Leakage is low for voltages up to 1,000 V.

Device II (HPK)

Effect of Annealing and Native Oxide

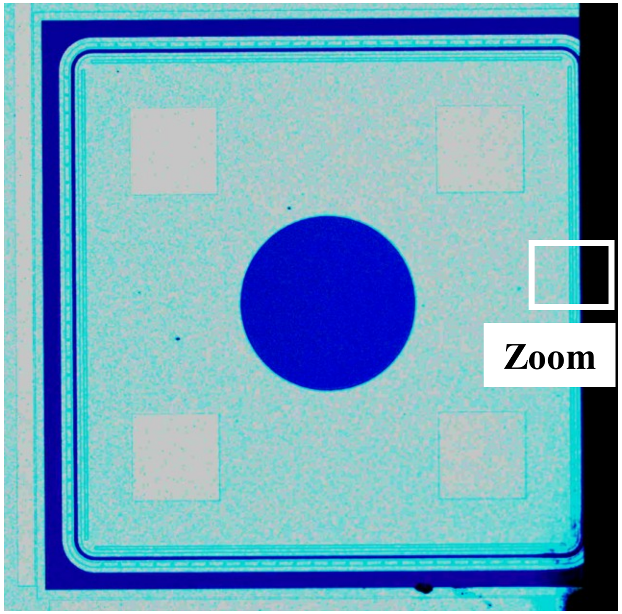


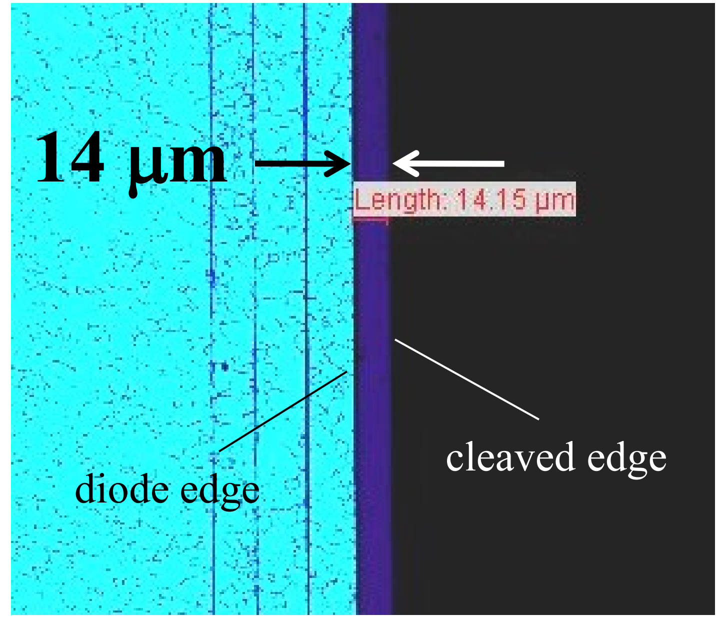
- annealing of alumina layer reduces leakage current (same effect as seen for solar cells, see slide #14).
- formation of native oxide (wrong surface charge) ↑ leakage current.
- native oxide forms rapidly (within seconds/minutes) in air.
- native oxide: ~ 2 nm thick, high charge trap density.

Device III (HPK)

Device Without Guard Ring

Optical micrographs, top-views

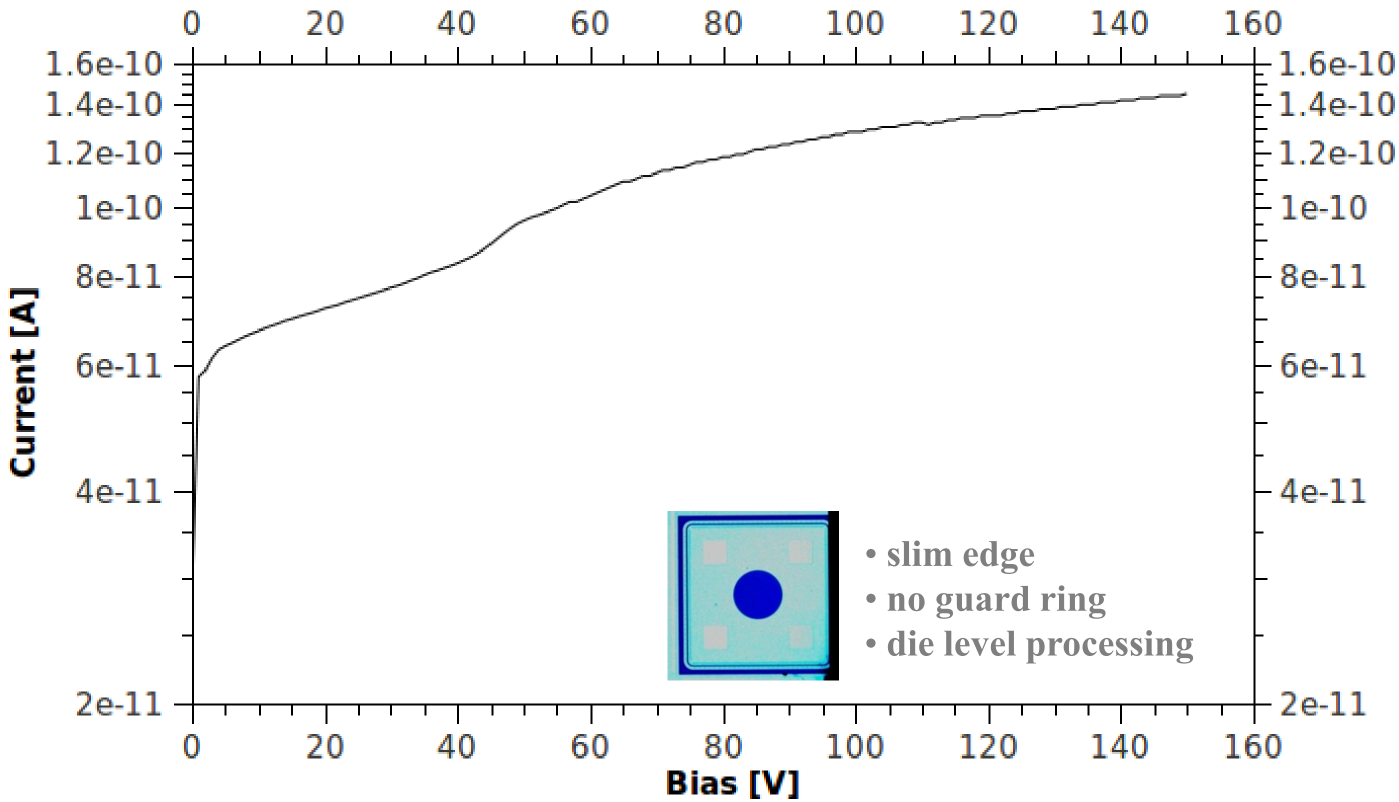




- No guard ring left.
- Slim edge (14 µm distance to active area).
- Leakage current 0.1 nA (see next slide).
- Pure cleaving of sample (no laser damage).
- Alumina sidewall passivation (thermal Al_2O_3 ALD at 300 °C).
- Done on finished die.

Device IV (HPK)

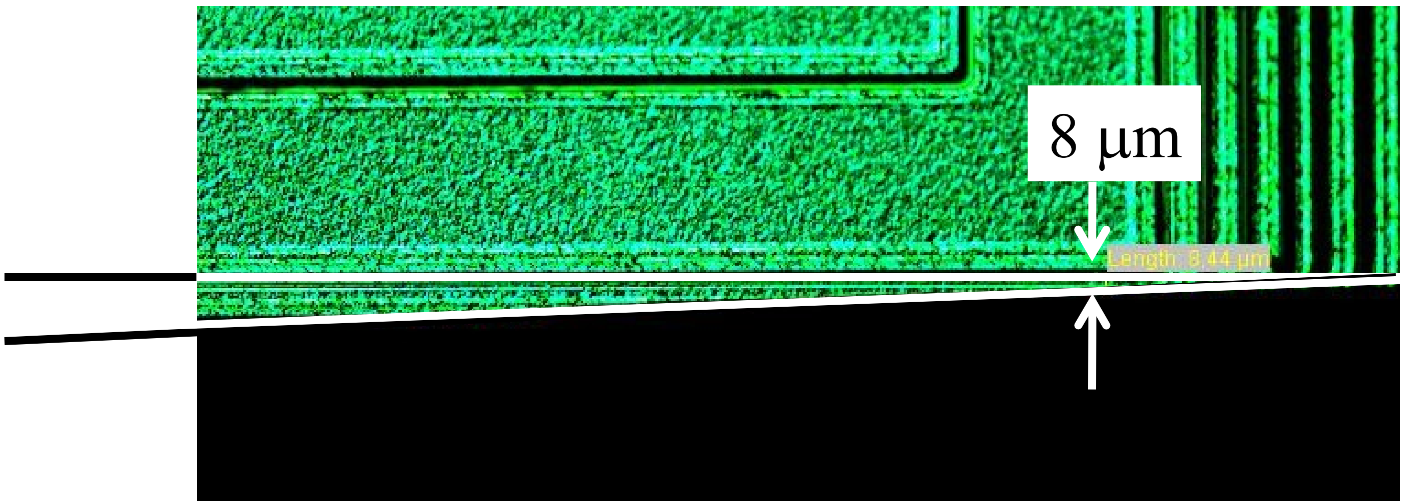
Device Without Guard Ring



If you obtain
1. minimal damage at edge and
2. "right" sidewall surface charge
you don't need guard ring(s)!

Device IV (HPK)

Cleaving – Crystal Alignment



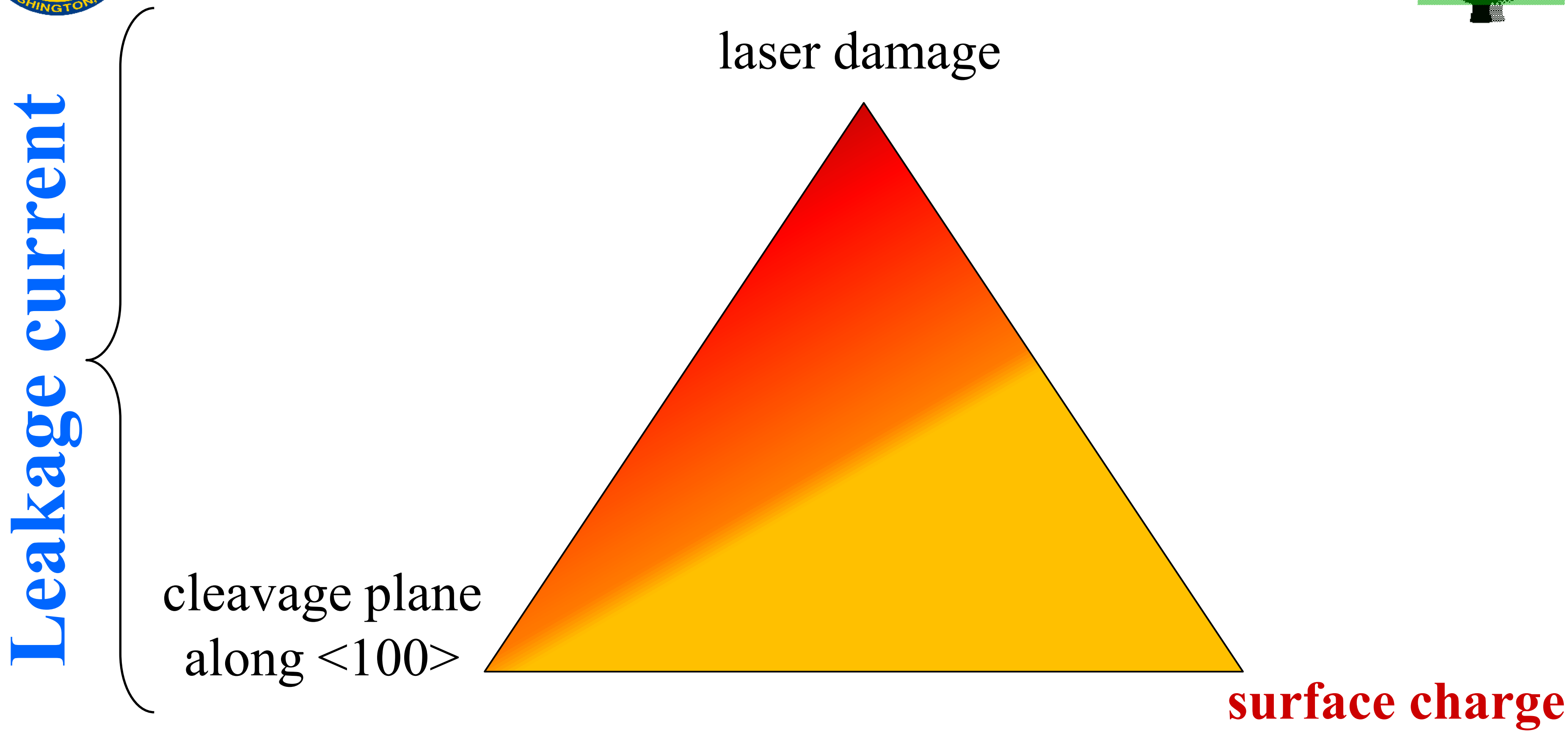
- CIS strip sensor from PPS submission.
- 8-guard ring design originally from Liverpool.

Cleaving is easier if
- device aligned with <100> direction,
- no mechanical stress from thin films.

SEMI standard for flat/crystal alignment: +/- 0.9 degrees
typical values for FZ material: +/- 0.1 degrees

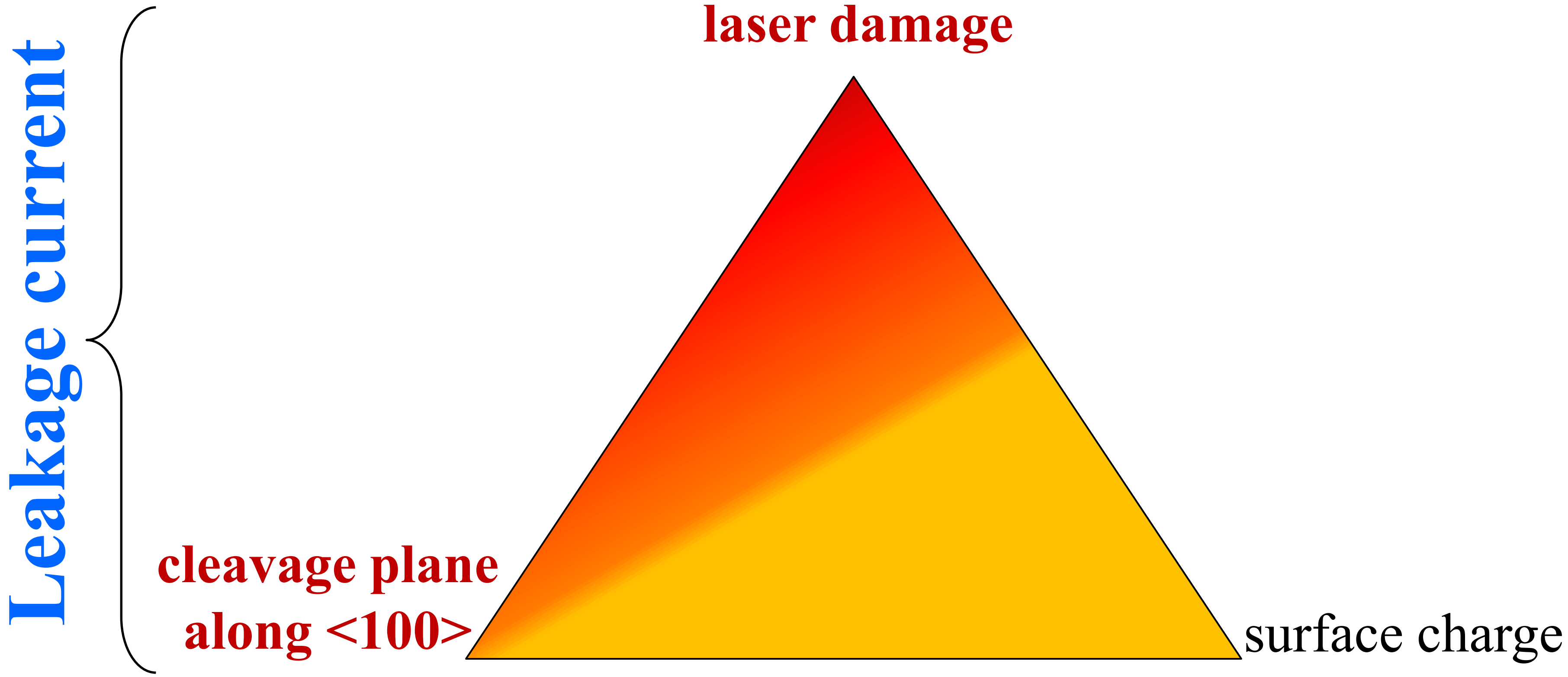
Device V CIS

Conclusions – Importance of Surface Charge



Leakage current is determined by
- controlled potential drop towards edge.

Conclusions – Importance of Sidewall Damage



Leakage current is determined by
- controlled potential drop towards edge.
- "quality" of silicon edge (cleaving leads to *no* silicon damage).

Conclusions and Future Work

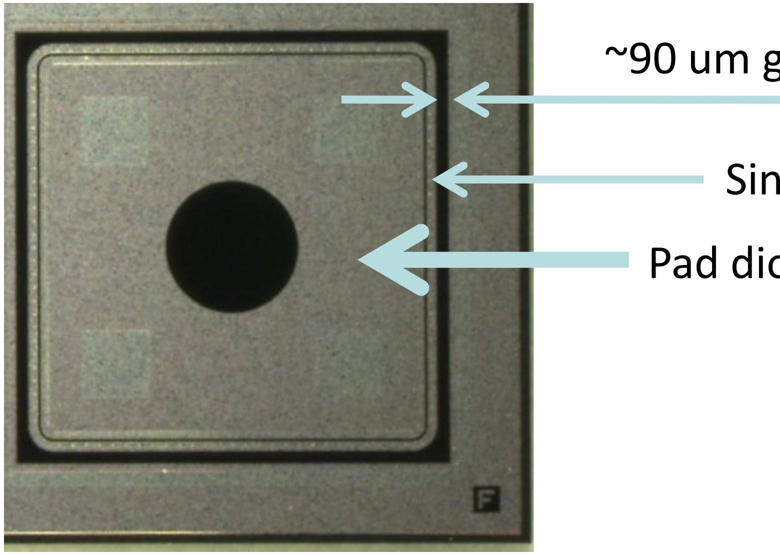
- Laser damage ↔ distance to active area.
- Laser damage can be minimized by laser power and defocusing.
- Cleavage plane depends on alignment and breaking process.
- **Cleaved sidewall has no silicon damage.**
- **N-type** silicon requires **positive** side wall passivation.
- **P-type** silicon requires **negative** side wall passivation.
- **Alumina/silicon interface has negative charge**.
- Alumina ALD passivation - **conformal, low-temperature process, low leakage currents, and can be used on finished die**.
- **We made a slim-edge p-type diode without guard ring and extremely low leakage currents (comparable to an active edge).**
- **If you obtain (i) minimal damage at edge and (ii) "right" sidewall surface charge you don't need guard ring(s)!**

- We currently perform charge collection measurements.
- Adjustable surface charge by ALD deposition.
- Determine exact alumina/silicon interface charge (CV plots).
- Alumina surface charge region sensitive to radiation/dose?

Back-Up Slides

Devices I-IV: HPK Samples

- Using a pad diode from HPK test structure meant to provide control over key sensor parameters for ATLAS07 sensors (*).
- It features a classic HPK single-guard ring design.
- Simple DC-coupled n-on-p pad. Vdepl ~ 180 V. Thickness 320 um.



(*) ATLAS07 strip sensors have been developed for ATLAS tracker upgrade for higher luminosity. They served as test vehicle for inter-strip isolation, punch-through protection, and other studies.

References:

Y. Unno et al., "Development of n-on-p silicon sensors for very high radiation environments", NIM A, doi:10.1016/j.nima.2010.04.080 .

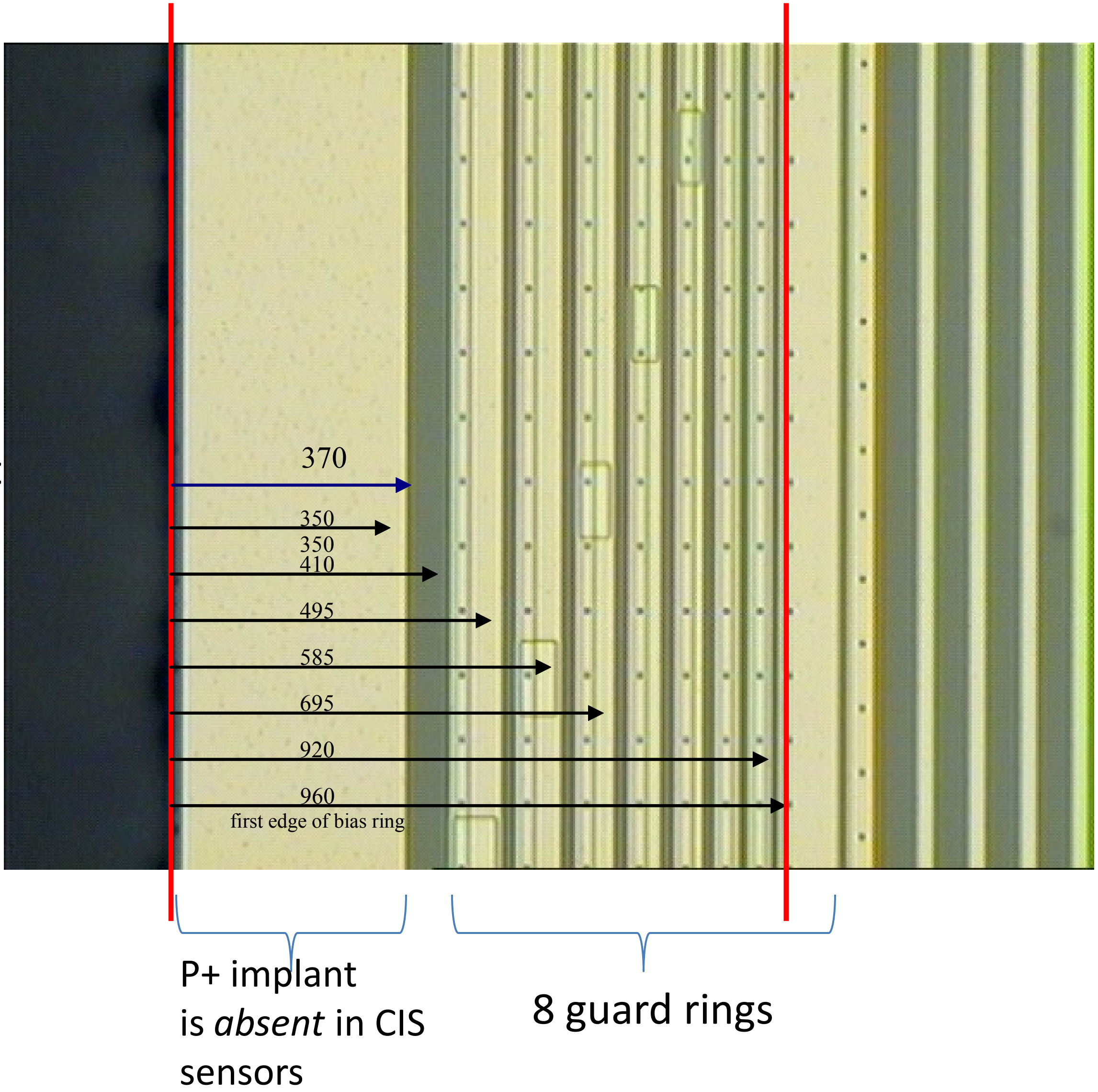
S. Lindgren et al., "Testing of surface properties pre-rad and post-rad of n-in-p silicon sensors for very high radiation environment", NIM A, doi:10.1016/j.nima.2010.04.094 .

J. Bohm et al., "Evaluation of the bulk and strip characteristics of large area *n*-in-*p* silicon sensors intended for a very high radiation environment ", NIM A, doi:10.1016/j.nima.2010.04.093 .

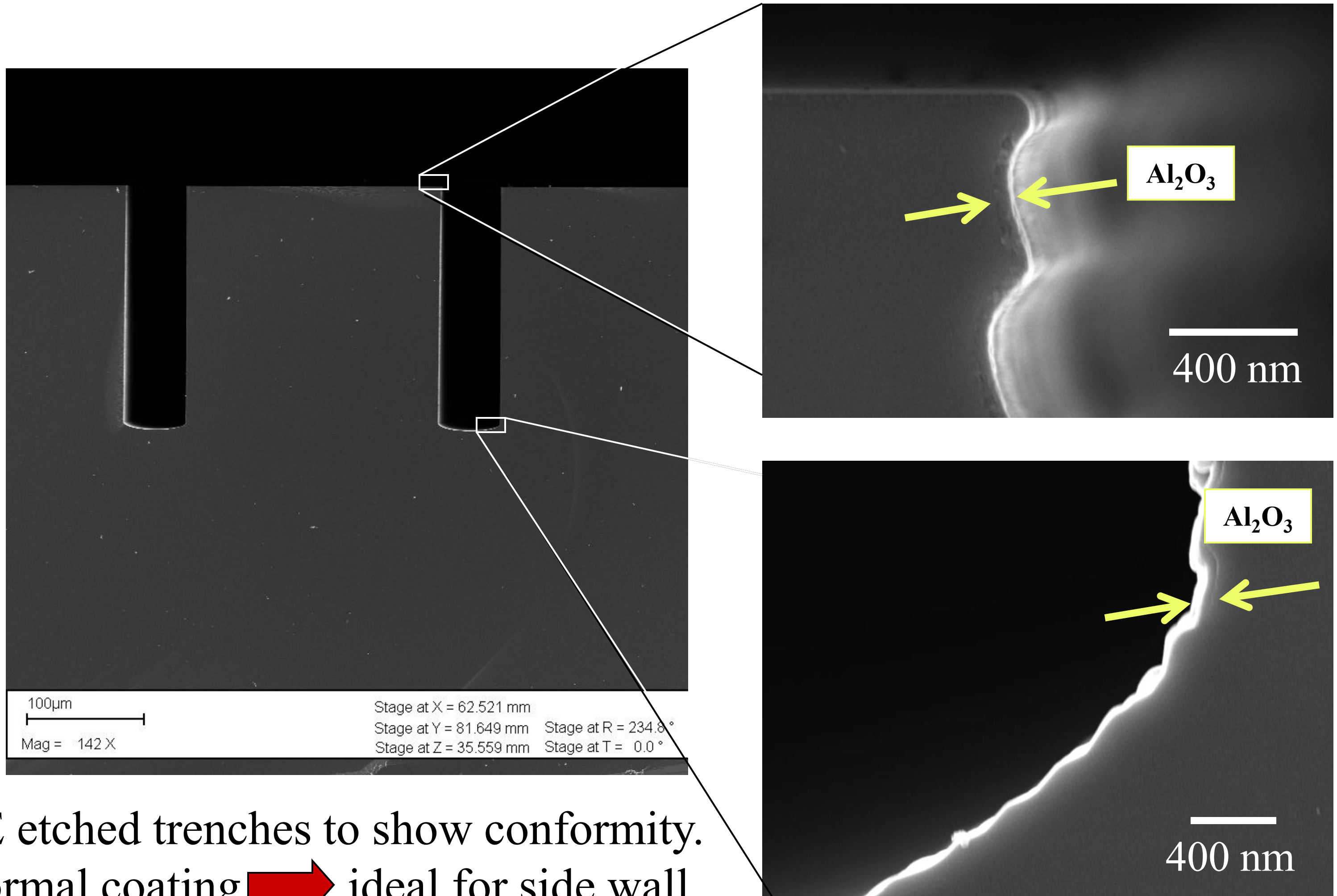
Device IV: CIS Sensor

- These strip test structures were part of ATLAS Planar Pixel submission to CIS foundry.
- The basic design is the same that Liverpool group used in Micron submissions (*).
- 8 guard ring structures. N-on-p sensor type. Vdepl ~50 V.
- The usual p+ implant structure at the periphery was specifically removed to facilitate the edge studies.

(*) G. Casse, P.P. Allport, A. Greenall, “Response to minimum ionising particles of p-type substrate silicon microstrip detectors irradiated with neutrons to LHC upgrade doses”, NIM A 581 (2007) p. 318.



ALD – Step Coverage



- DRIE etched trenches to show conformity.
- conformal coating → ideal for side wall passivation.

Alumina ALD Reactions

- Releases sequential precursor gas pulses to deposit a film one layer at a time.

  Two fundamental mechanisms:
  - *Chemisorption saturation process*
  - *Sequential surface chemical reaction process*

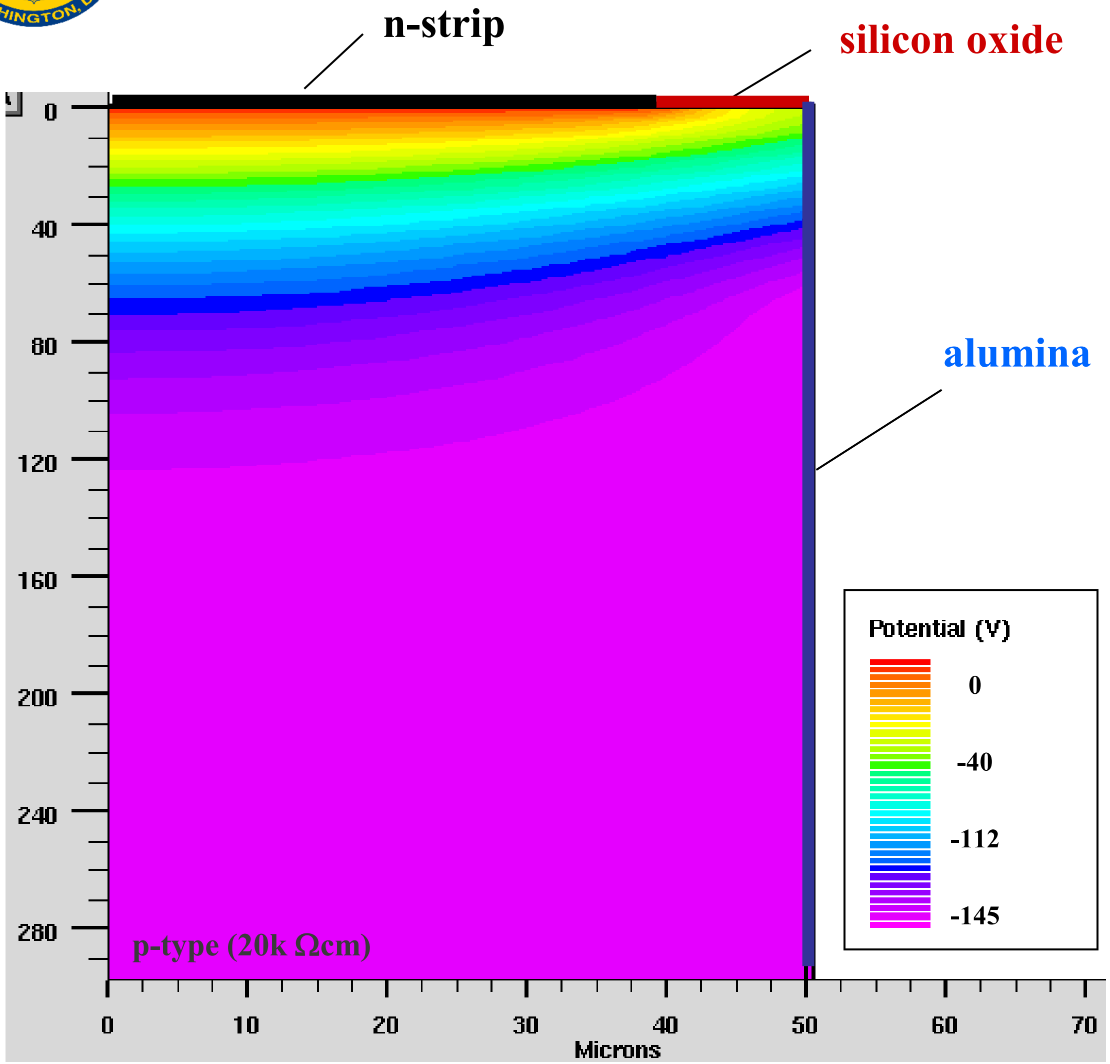
- Since each pair of gas pulses (one cycle) produces exactly one monolayer of film, the thickness of the resulting film may be precisely controlled by the number of deposition cycles.
- One TMA (trimethylaluminium) and H_2O vapor pulse per cycle, ~ 1 Å per cycle, pumping ~ 3 sec per cycle.

Two reaction steps in each cycle:

$$Al(CH_3)_{3\,(g)} + :Al\text{-}O\text{-}H_{\,(s)} \longrightarrow :Al\text{-}O\text{-}Al(CH_3)_{2\,(s)} + CH_4$$

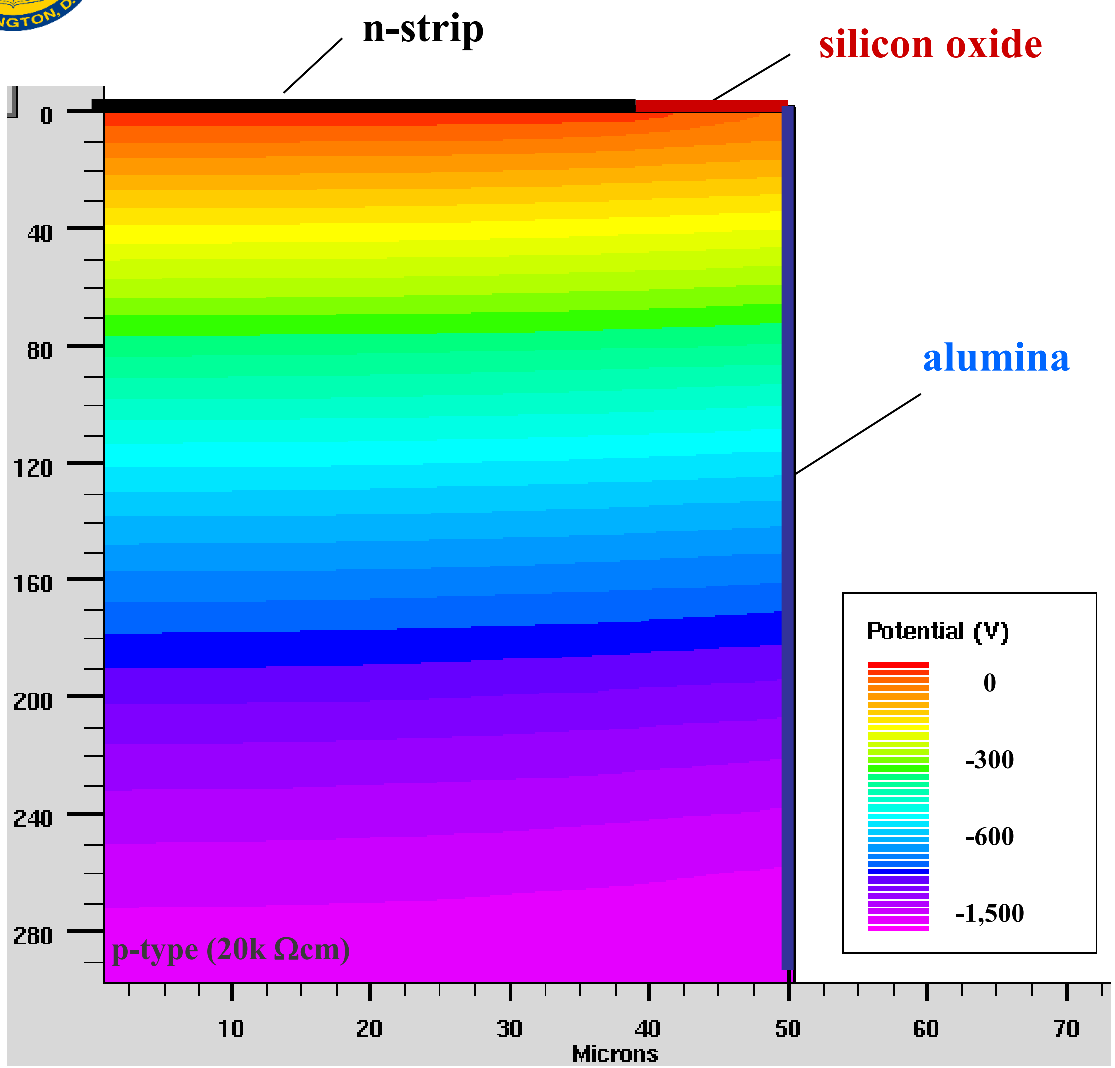
$$2\,H_2O_{\,(g)} + :O\text{-}Al(CH_3)_{2\,(s)} \longrightarrow :Al\text{-}O\text{-}Al(OH)_{2\,(s)} + 2\,CH_4$$

Potential Distributions for Combined SiO_2 and Al_2O_3 Passivation



Since we use finished dies, there is SiO_2 passivation (or nitride) with positive interface charge at top surface. We deposit Al_2O_3 on sidewall.

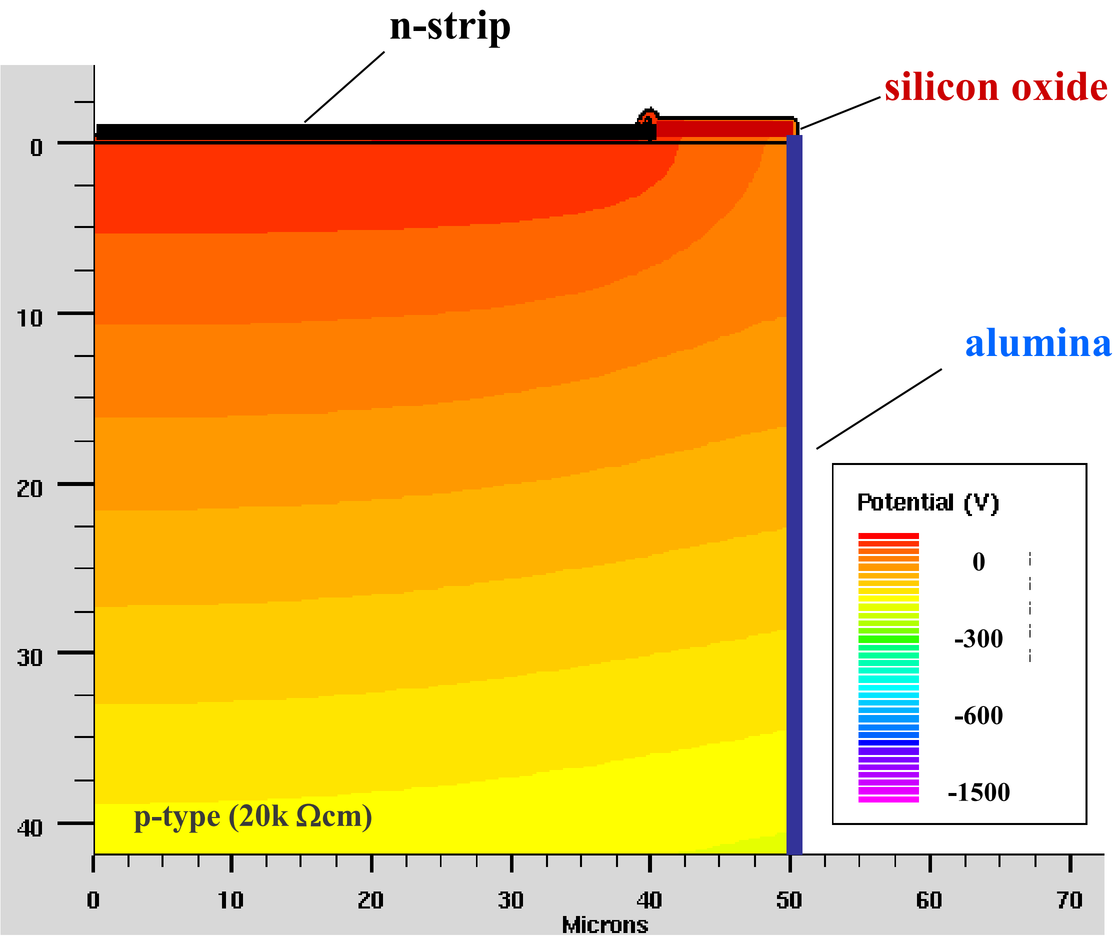
Potential Distributions for Combined SiO_2 and Al_2O_3 Passivation

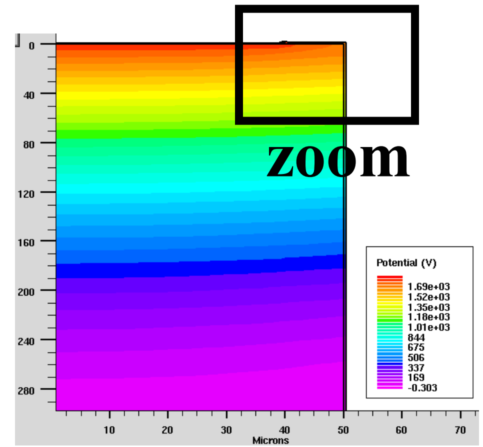


At high voltage:

- no high electric field at trench edge,
- controlled potential drop towards the cut edge.

Potential Distributions for Combined SiO_2 and Al_2O_3 Passivation

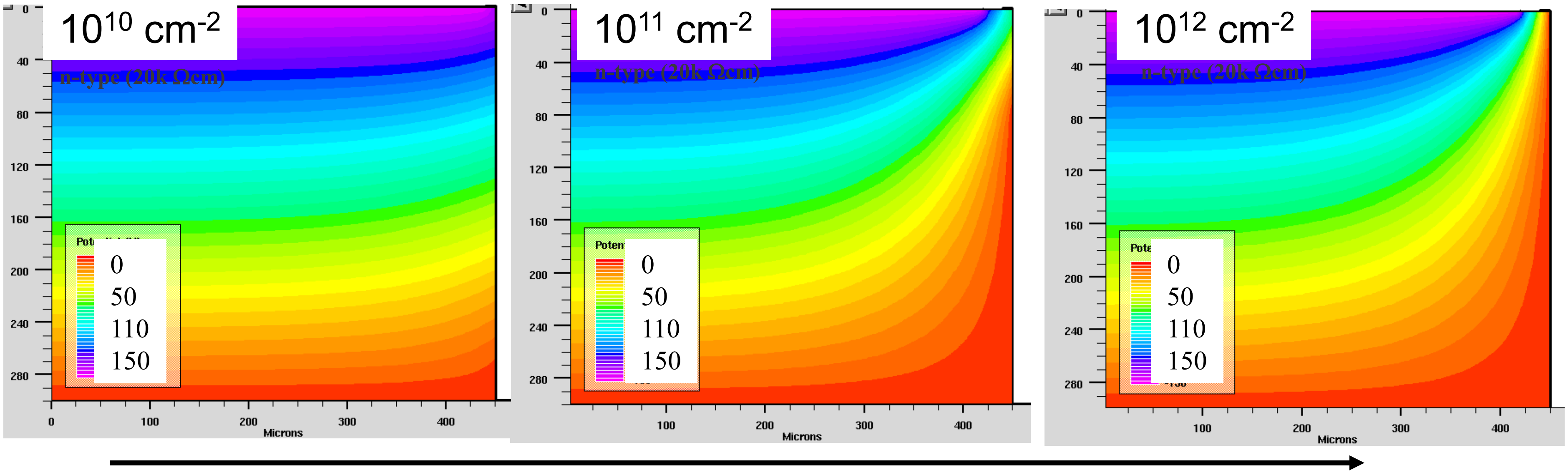




At high voltage:

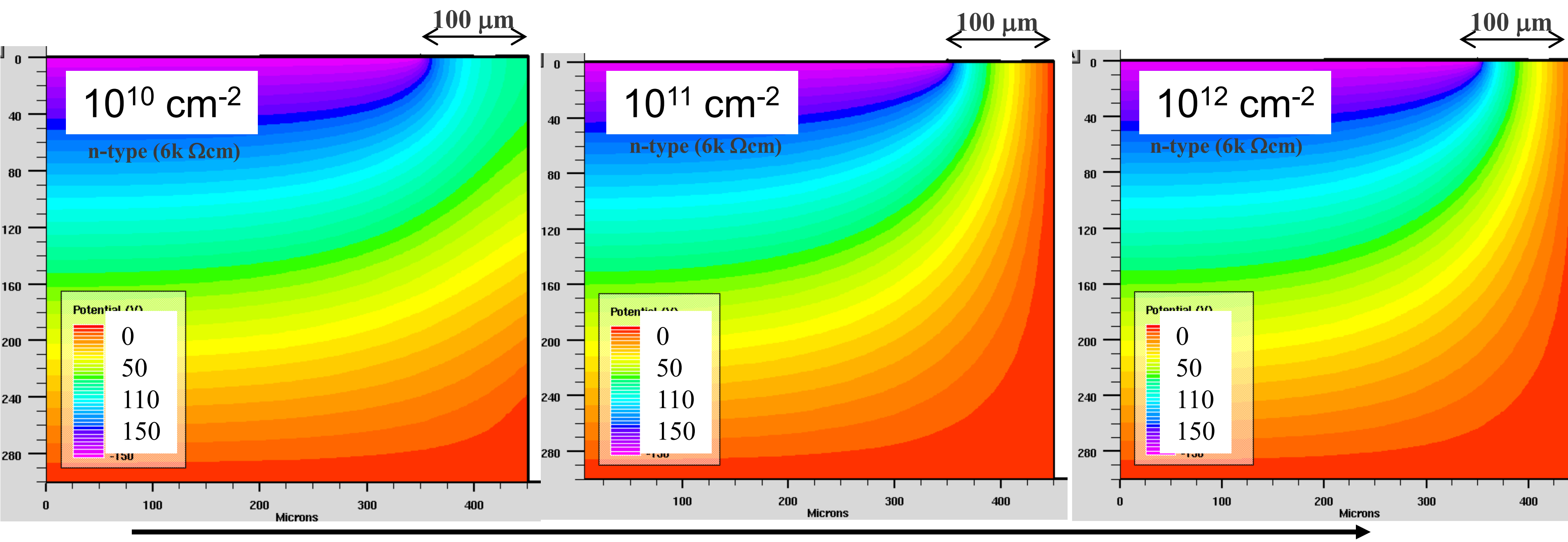
- no high electric field at trench edge,
- controlled potential drop towards the cut edge,
- no potential at surface.

Influence of Surface Charge Concentration: N-Si/SiO_2



increasing positive surface charge

Influence of Surface Charge Concentration: N-Si/SiO_2



increasing positive surface charge

The simulation is done for p-on-n strips on top surface.