Silicon n-in-n pixel detectors: Sensor productions for the ATLAS upgrades, first slim-edge measurements and experiences with detectors irradiated up to SLHC fluences

6th Trento Workshop on Advanced Radiation Detectors

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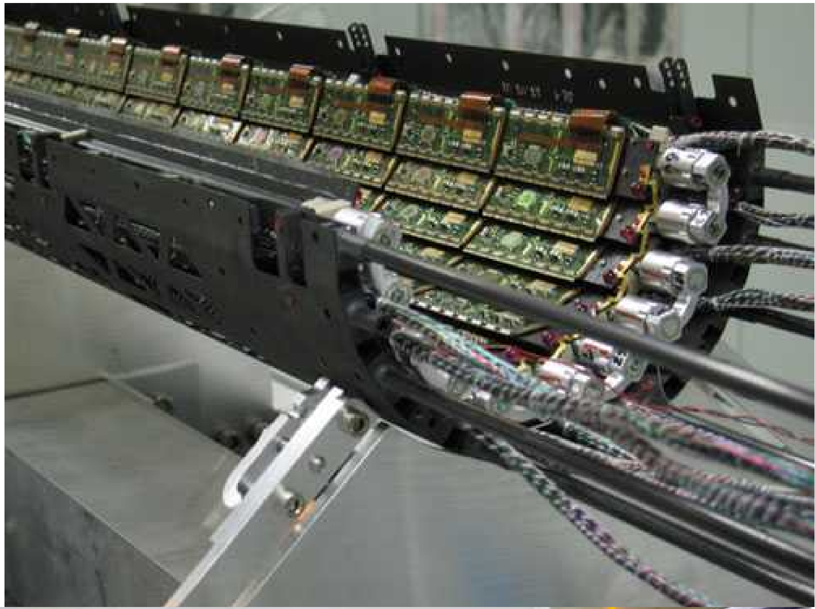
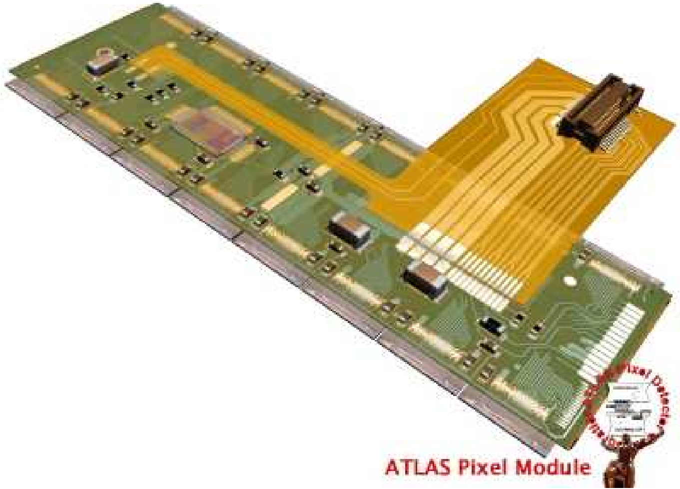
Planar Sensors: Basic Information

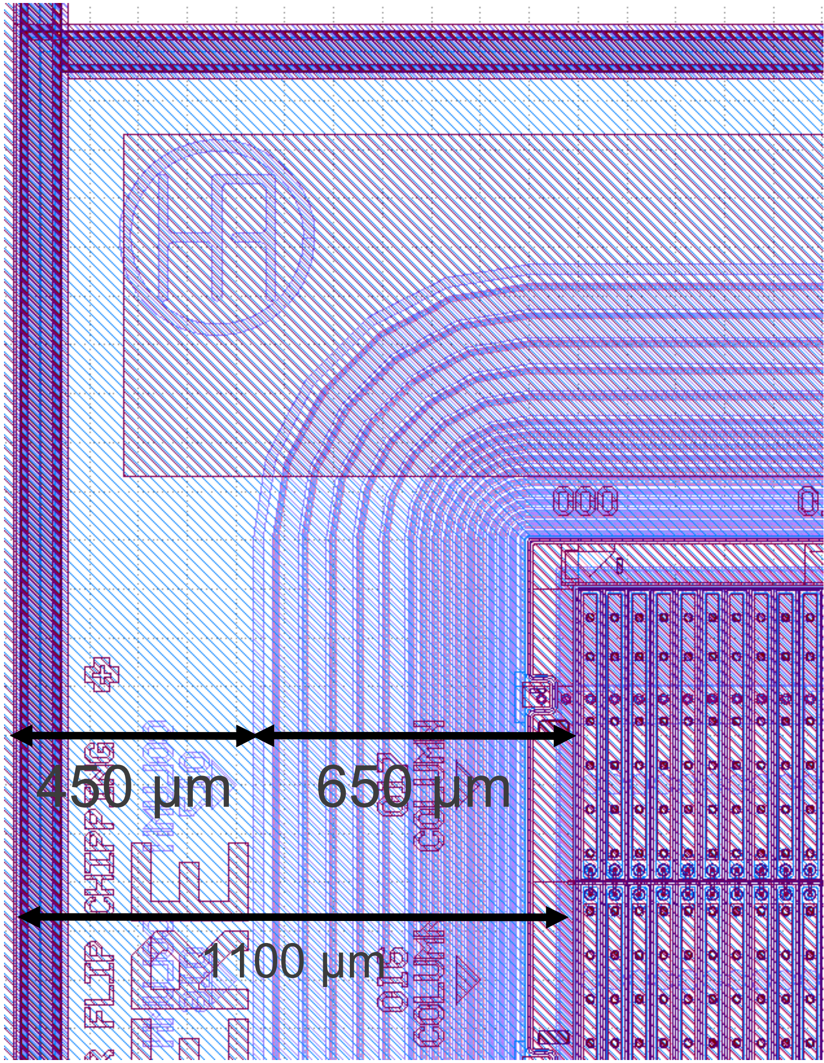
- The current ATLAS Pixel detector is based on planar sensors
- Planar sensors were already shown to yield charge even after SLHC fluences of $2 \cdot 10^{16}\ n_{eq}/cm^2$
- IBL specifications to qualify:
  - Power dissipation < 200 mW/cm^2
  - Leakage current < 100 nA/pixel
  - Operation temperature -15°C on sensor
  - Inactive edges < 450 µm
  - Thickness between 150 and 250 µm
  - Sufficient hit efficiency
    - after a benchmark fluence of $5 \cdot 10^{15}\ n_{eq}/cm^2$
    - at a maximum bias voltage of 1 kV





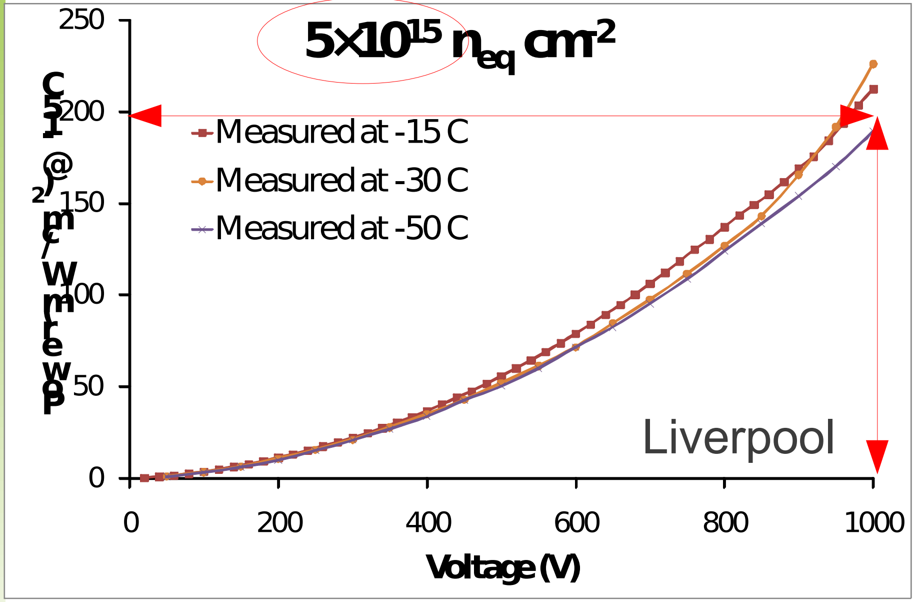
Initial point

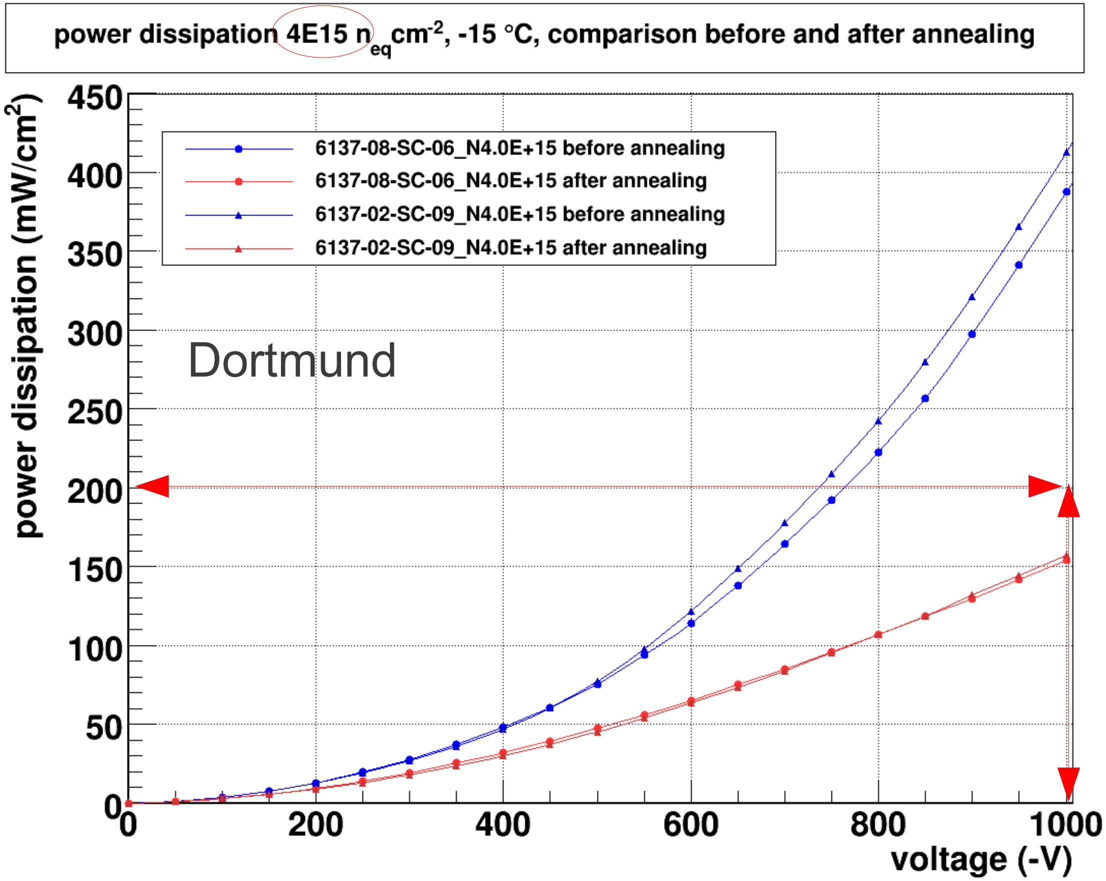
- Standard SingleChip Sensors taken from ATLAS Pixel production wafers
- n^+-in-n design produced by CIS
- 16 guard rings with overhanging metal
- 250µm thick DOFZ bulk
- 400µm by 50µm pixel cells
- 2880 pixel cells
- Current (n^+-in-n) pixel detector has been shown to be rad hard up to $1 \cdot 10^{15}$ n_{eq}/cm^2
- Planar n^+-in-n technology is proven and reliable
- Results gained with strip sensors showed promising results with regard to collected charge (charge amplification)!
- New production in 2009 and 2010:
  - varied bulk thicknesses (150µm – 285µm)
  - several special layouts (e.g. w/o bias grid) and FE-I4 compatible sensors



Leakage current/power dissipation

- Power dissipation can be kept below 200 mW/cm² at 1 kV and at -15°C
  - Some (few days at 20°C) annealing might be necessary.
- Leakage current below 200 µA/cm² at 1kV, i.e. < 25 nA/pixel

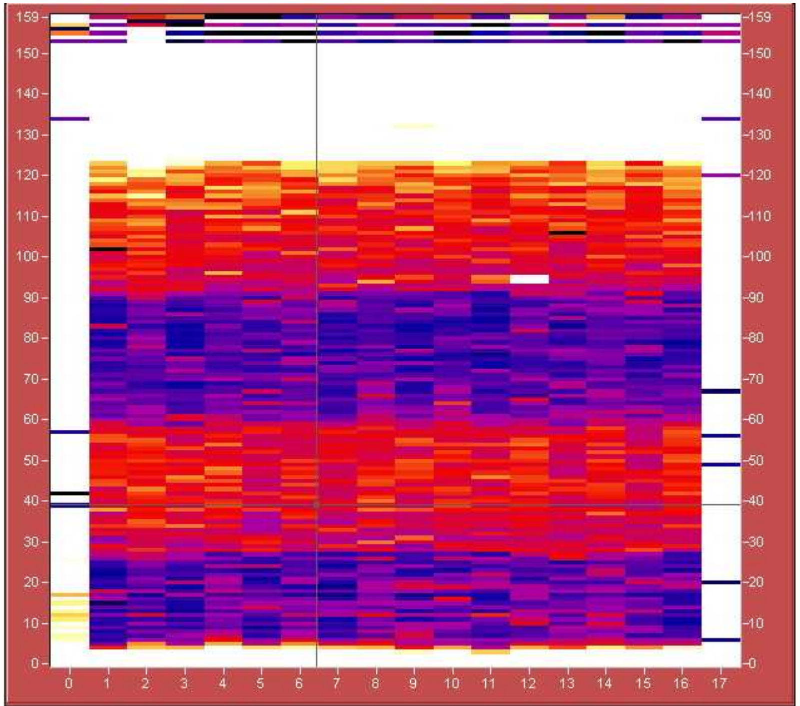




Operating FE-I3 after severe irradiation

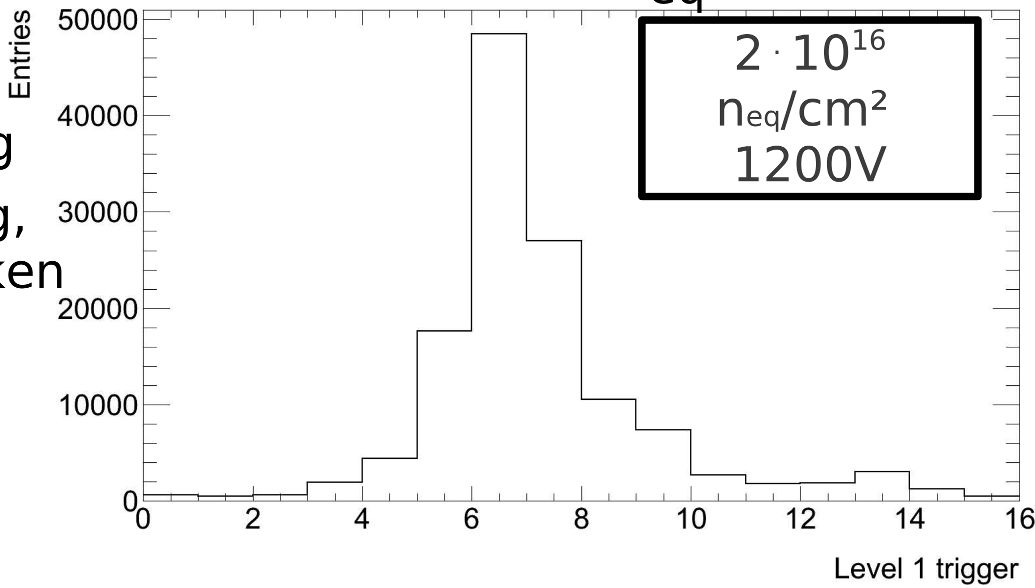
Main challenges:

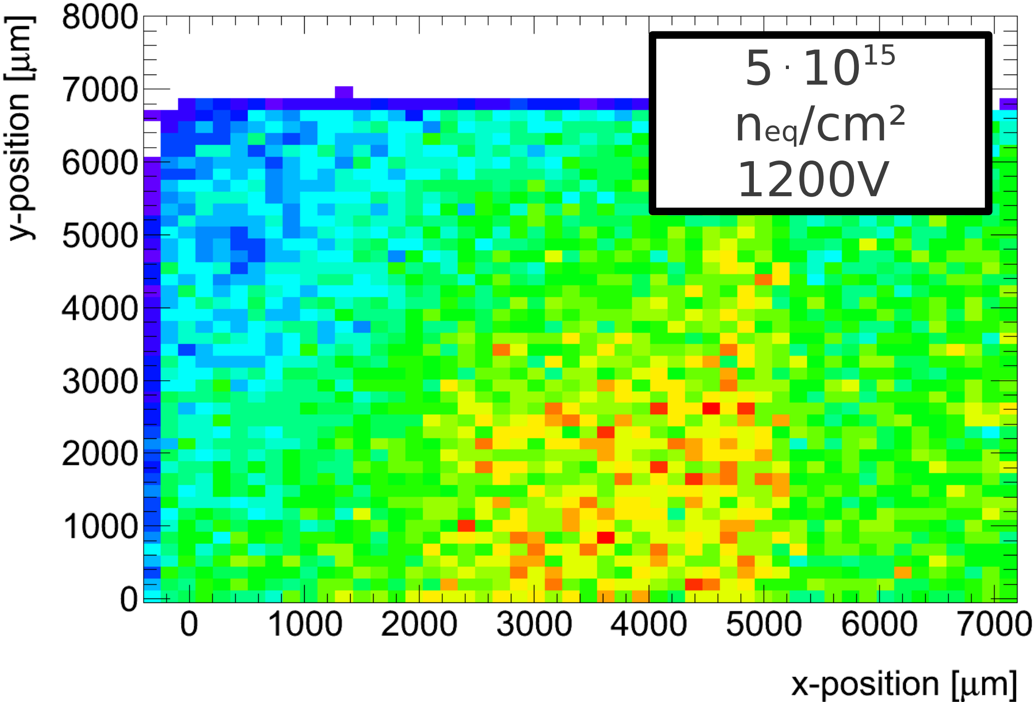
- *Very* cold operation necessary (below -40°C for $2 \cdot 10^{16}$ n_{eq} cm^{-2})
- Low signal: low thresholds required
  - Usual ATLAS FE-I3 threshold rather high: 3000 – 4000 electrons
- Irradiated sensors will not survive a bump-bonding thermal cycle → operation with irradiated LHC readout chips
- ATLAS FE-I3 readout chip was designed for LHC flucences and is generally not rad-hard enough
  - neutron irradiation (less damaging for electronics)
  - threshold tuning and digital communication always works
  - but: erratic behaviour observed, even from the same irradiation batch:
    - on some days, source scans only yield noise/empty events/stripes
    - on some days, chip works fine
    - some chips never work
    - some chips always work

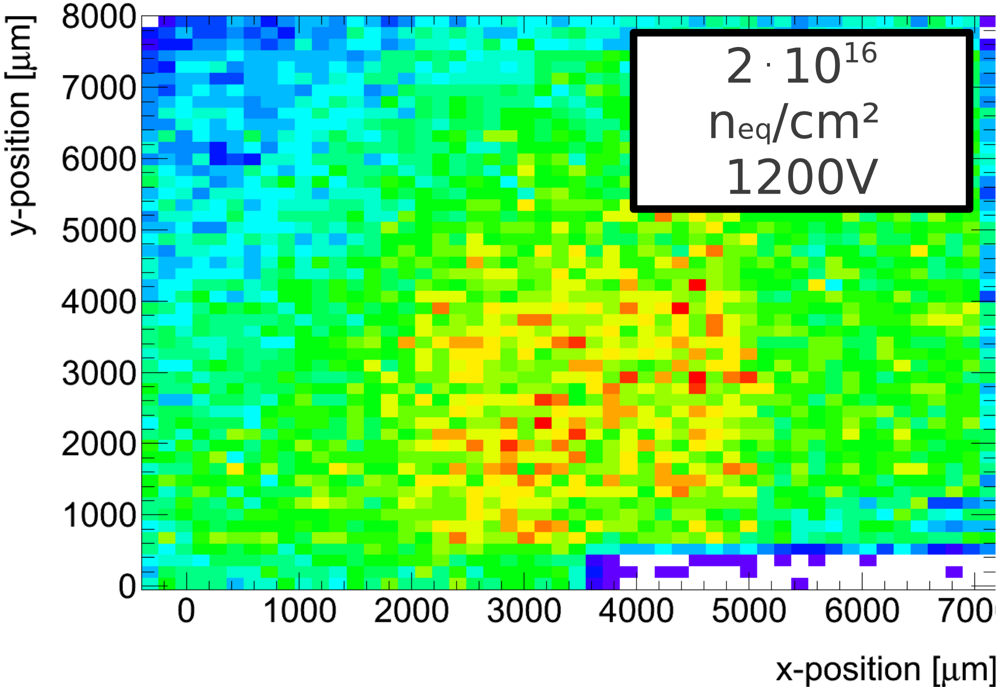


A challenge: $5 \cdot 10^{15}\ n_{eq}/\mathrm{cm}^2$ and $2 \cdot 10^{16}\ n_{eq}/\mathrm{cm}^2$

- Operation at below -50°C to exclude self-heating effects
- $2 \cdot 10^{16}\ n_{eq}/\mathrm{cm}^2$ sample always working
- $5 \cdot 10^{15}\ n_{eq}/\mathrm{cm}^2$ sample mostly working, data with more such samples was taken and is currently being analysed
- Testbeam hitmaps look good
- Trigger-distribution shows little noise

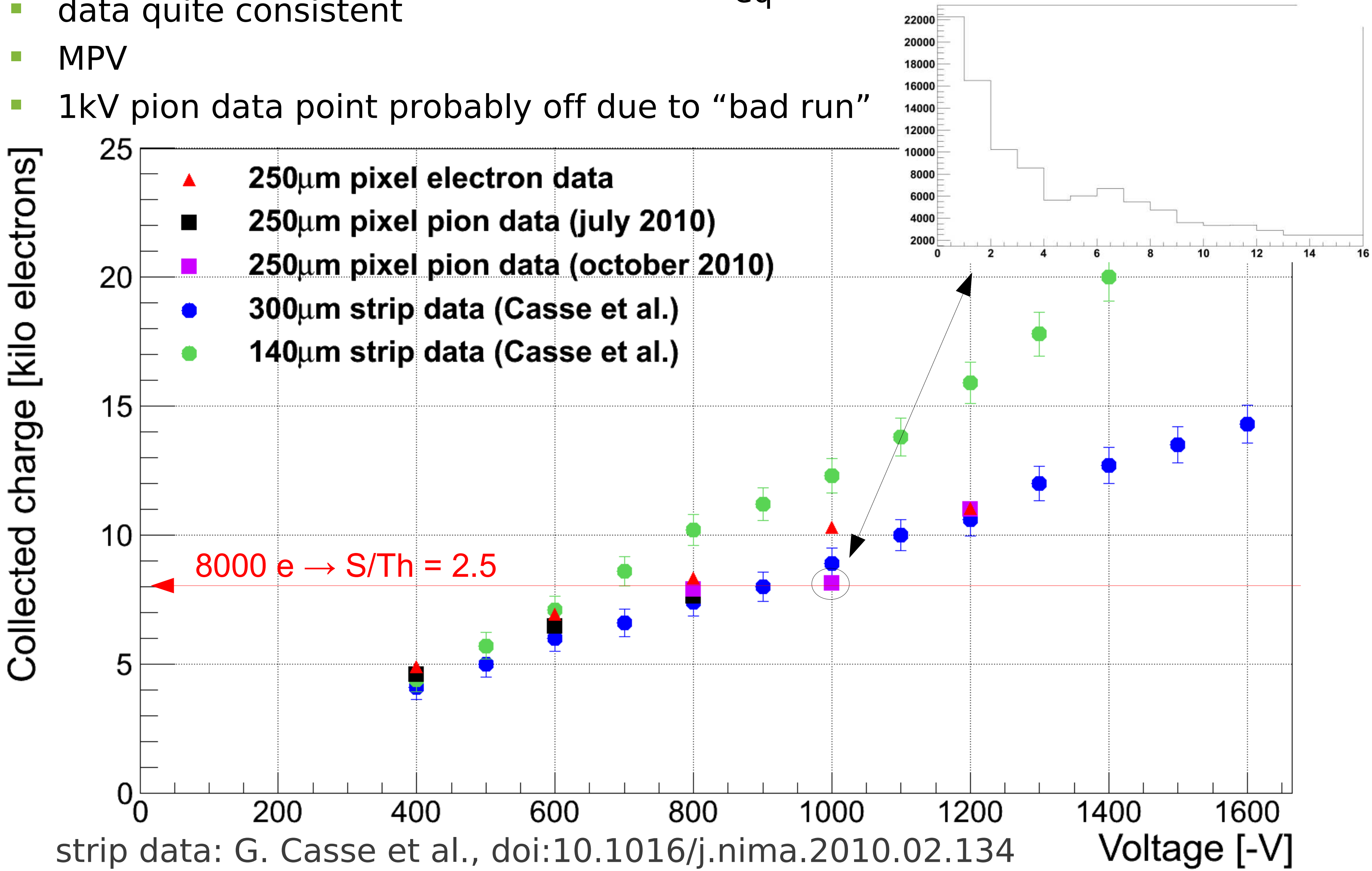






Charge Collection $5 \cdot 10^{15}$ n_{eq}/cm^2 summary

- data quite consistent
- MPV
- 1kV pion data point probably off due to “bad run”

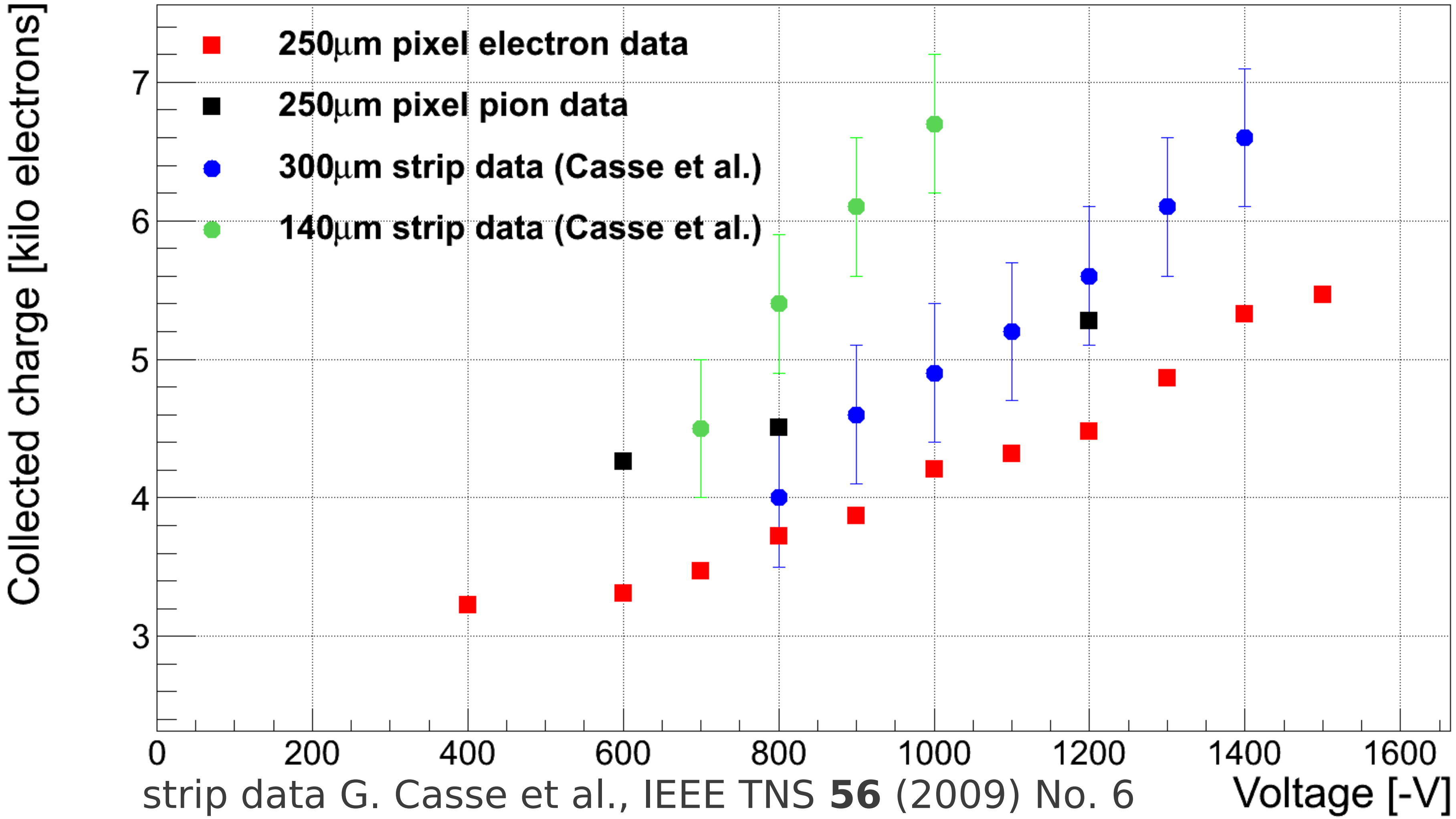


strip data: G. Casse et al., doi:10.1016/j.nima.2010.02.134

Charge Collection $2 \cdot 10^{16}$ n_{eq}/cm^2 summary

- Pixel electron data lower than pion data and lower than strip data
- Might be a charge-sharing effect
- MPV

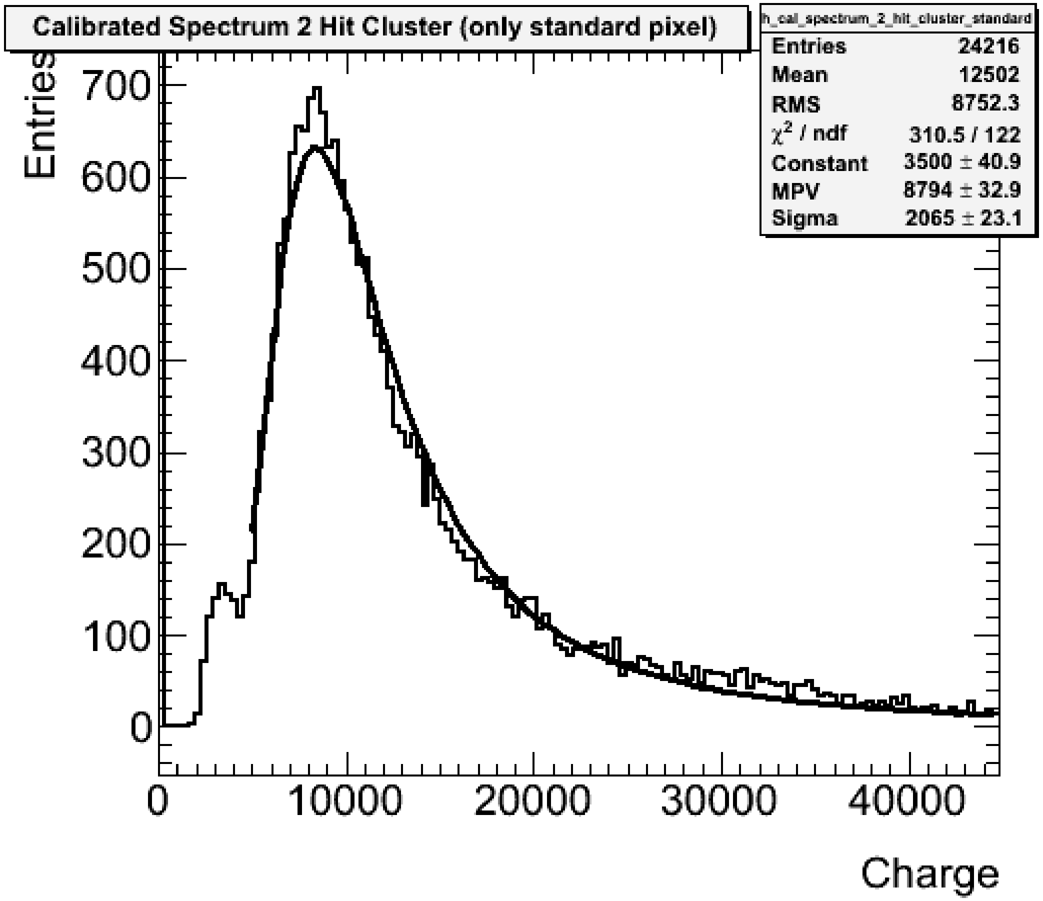
doi:10.1016/j.nima.2010.11.186

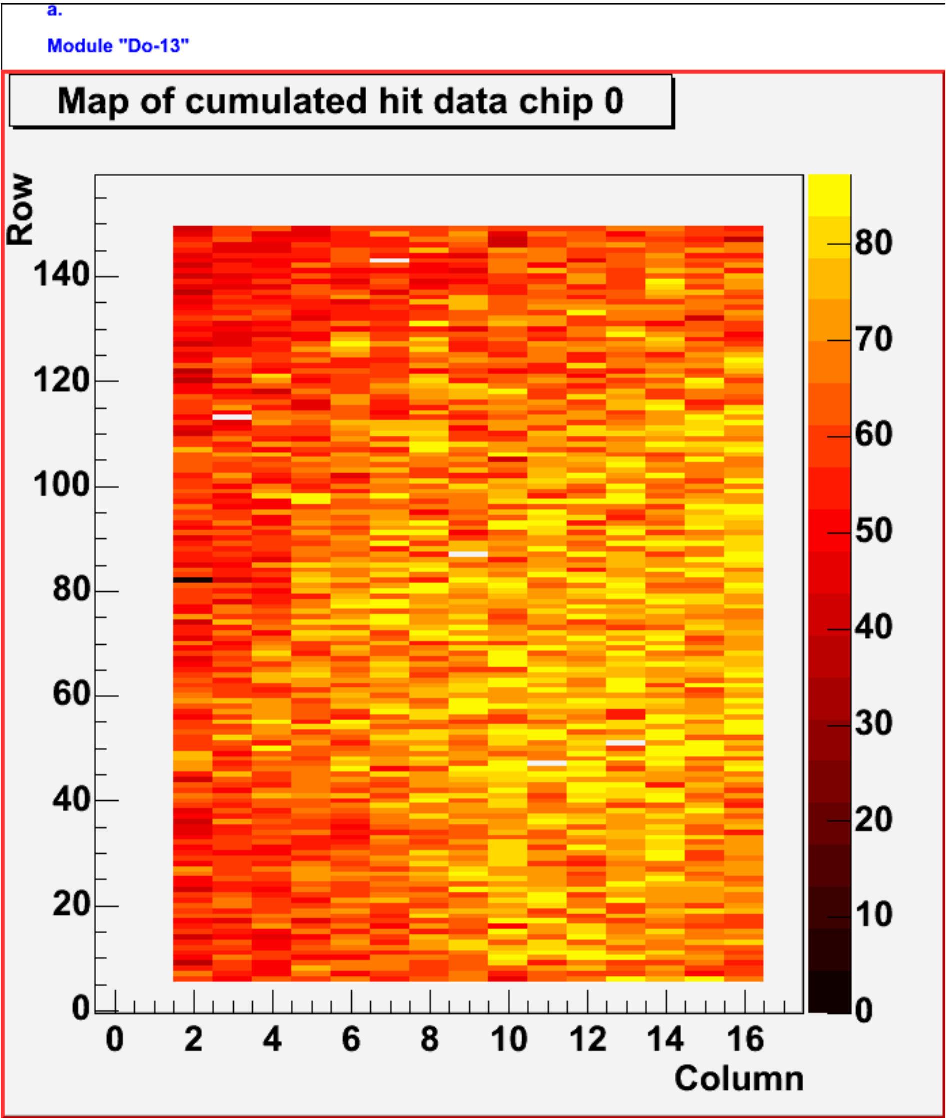


strip data G. Casse et al., IEEE TNS **56** (2009) No. 6

Operation at -15°C

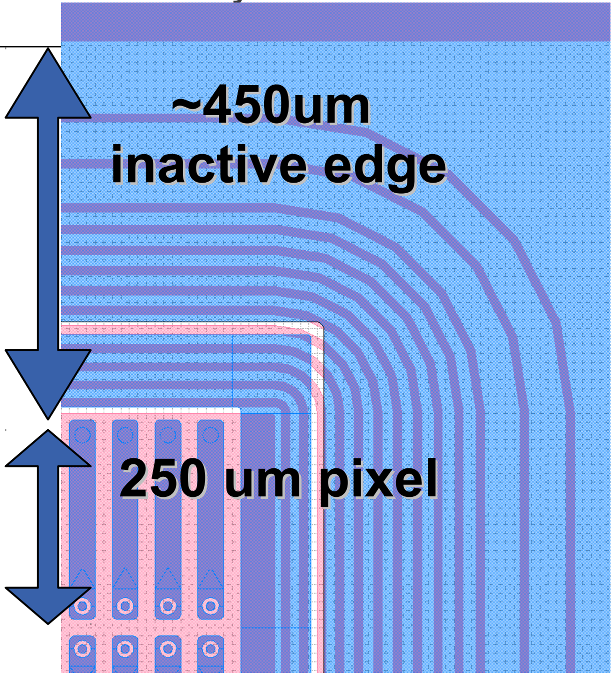
- Up to now: dry-ice cooling to cope with large DeltaT values
- First measurements with a low-temperature chiller which allowed to tune the sensor temperature to roughly -15°C (some °C warmer)
- leakage current ~180 µA/cm² @ 800V
  - no annealing yet
- collected charge ~9 ke⁻ @ 800V

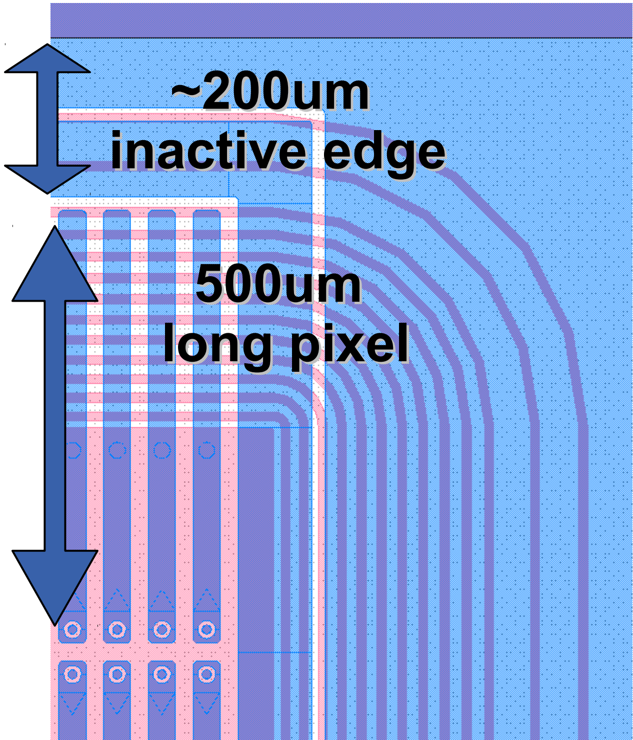


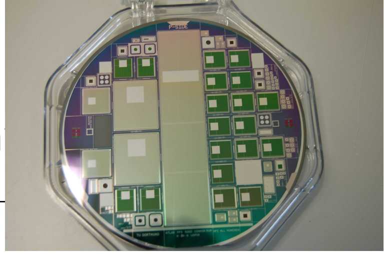


Inactive edge widths

- 2 official n-bulk designs produced:
  - n-in-n: mature technology
  - double sided processing, 4” wafers
  - CiS one of the ATLAS Pixel production vendors
- Conservative design
  - as similar as possible to current ATLAS design
  - ~450 µm inactive edge width
  - electric field at edges homogenious
- Slim edge design
  - guard rings on p-side are shifted beneath the outermost pixels → least possible inactive edge (< 200 µm)
  - less homogenious electric field, but charge collection after irradiation dominated by region directly beneath the pixel implant → only moderate deterioration expected
- Three parameters:
  - Safety margin (doi:10.1016/j.nima.2010.06.004)
  - Number of guard rings
  - Pixel opposite guard rings

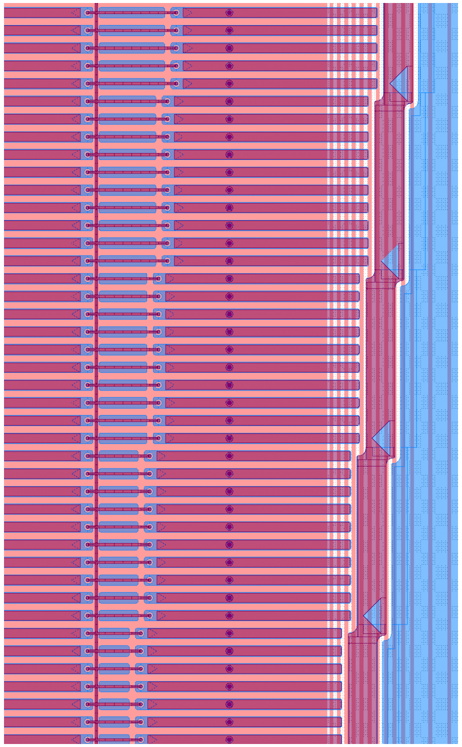


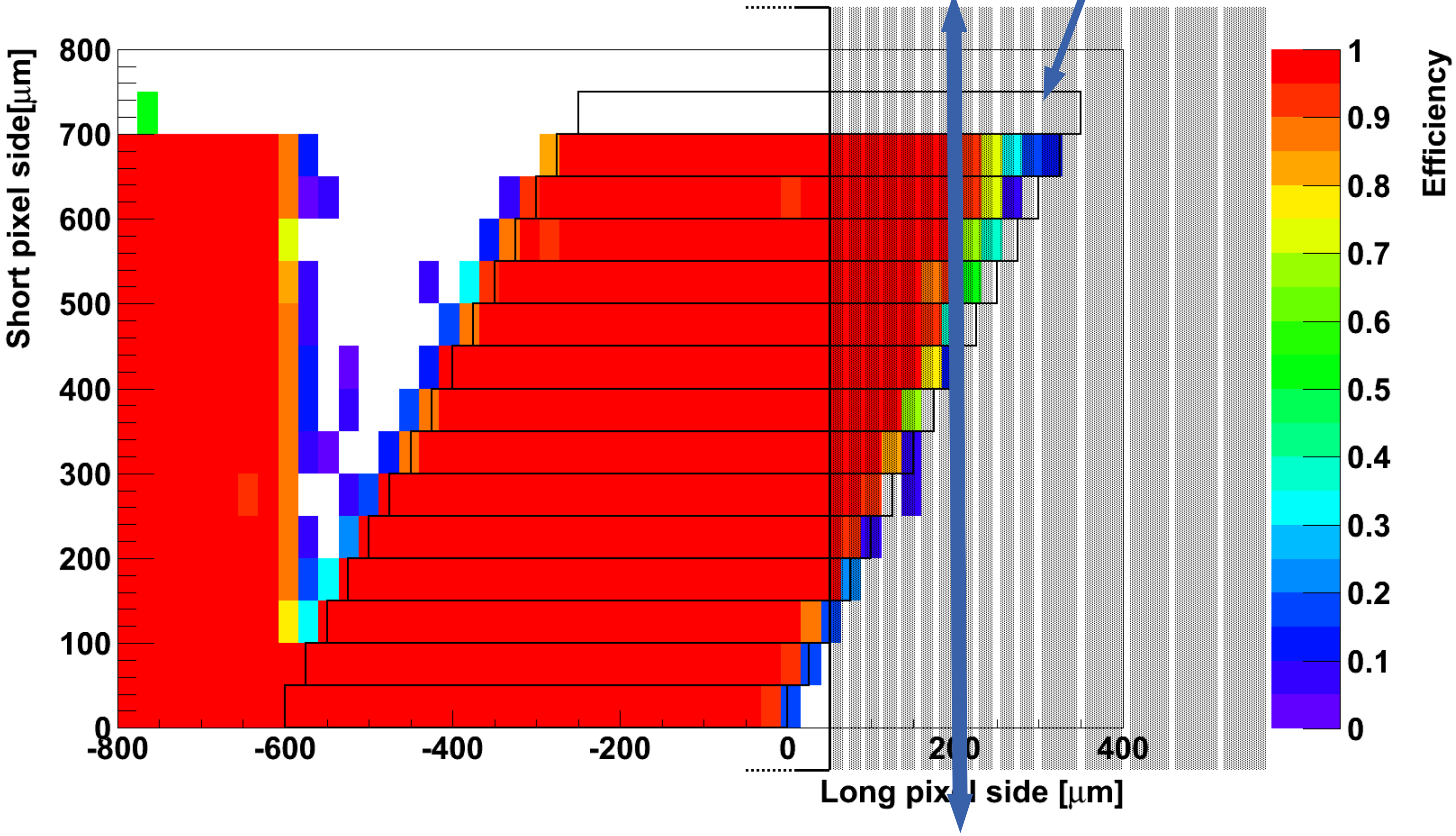




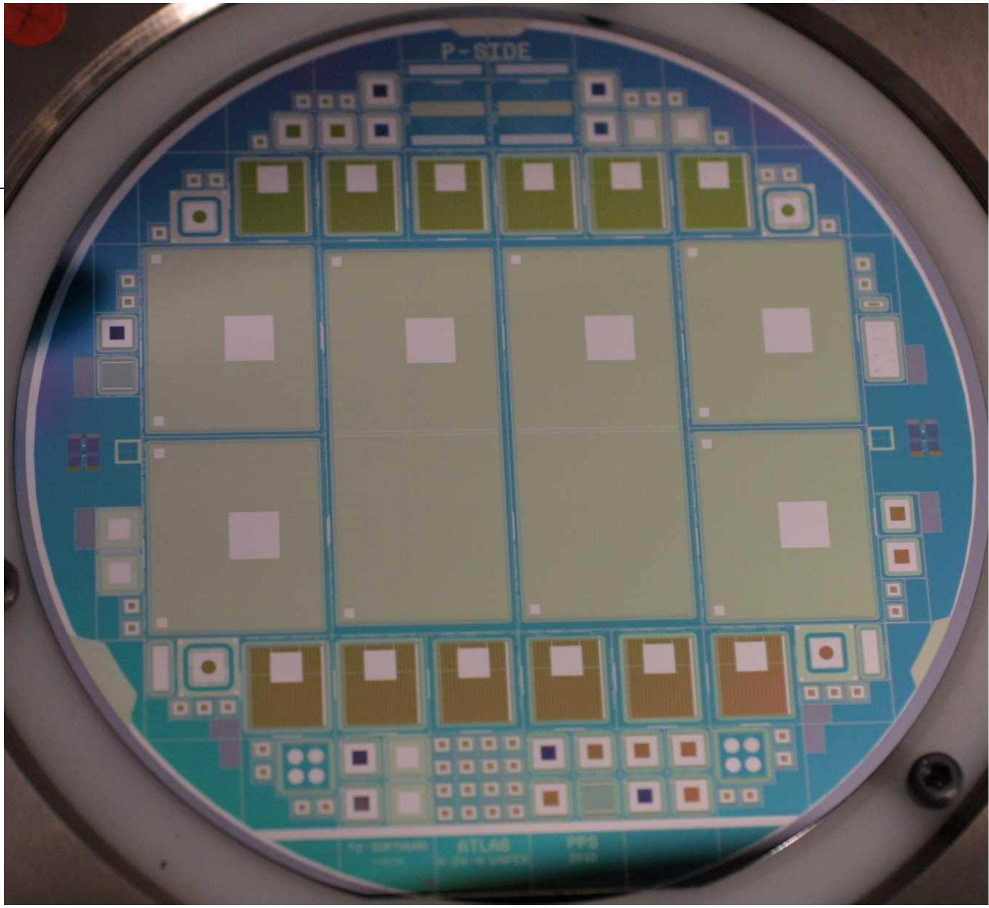
Slim-edge: testbeam results available up to now

- dedicated test structure ('pixel shifted stepwise') confirms that charge is collected opposite of the guard rings
- estimated region of high (>99%) efficiency before irradiation: up to ~200 µm from the HV implant (i.e. ~250 µm inefficient edge)
- looks promising (strongly supported by simulation results at LAL by M. Benoit)





n-bulk qualification wafer

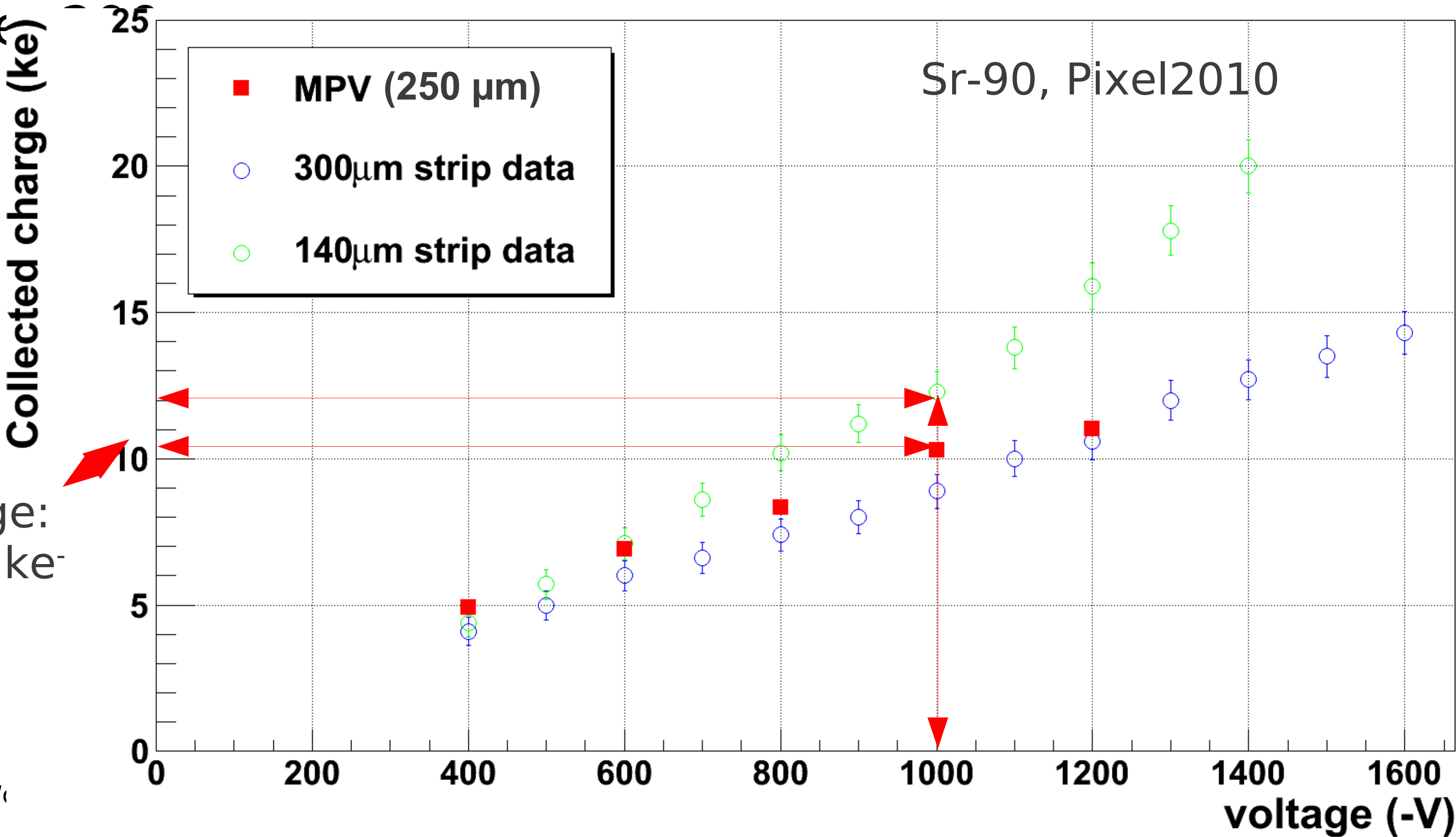


- 6 FE-I4 sensors:
  - conservative (no long pixels, no pixel overlap)
  - slim edge (long pixels (500um), pixels shifted over guard rings)
  - 1 2-chip and 2 1-chip sensors of each design
- 12 FE-I3 SCs
  - various guard ring designs
- diodes, test structures...
- vendor: CiS
- 5 thicknesses:

thickness	wafers ordered	wafers received
250um	12	18
225um	6	11
200um	6	10
175um	6	11
150um	6	8

Wafer thickness

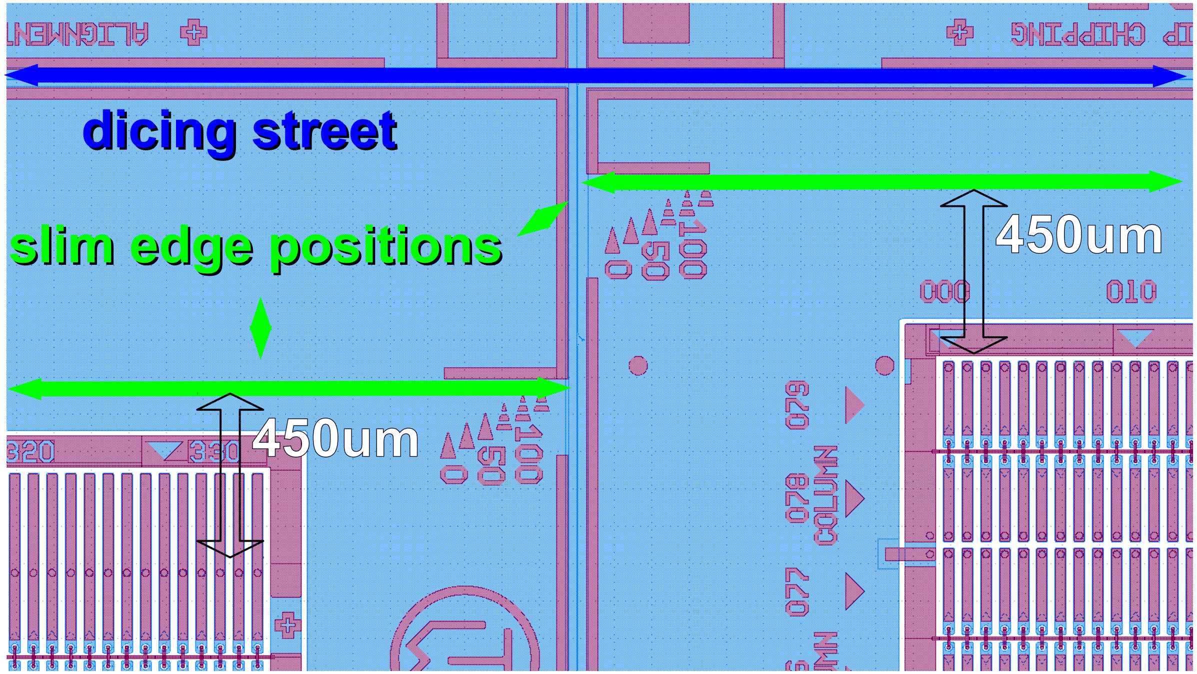
- Thinner sensors
  - generate about 1-2 ke$^-$ more charge after $5 \cdot 10^{15}$ n_{eq}/cm^2 at 1 kV
  - have less radiation length
- Baseline: 250 µm (ATLAS production)
- Extreme: 150 µm
- Compromise

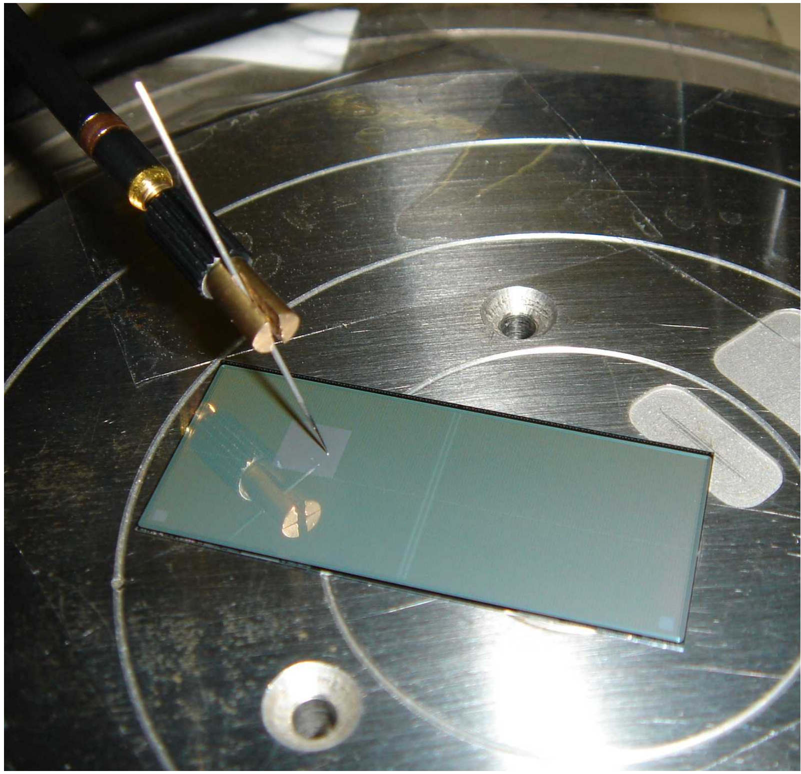


Expected charge:
10-12 ke$^-$

Status 250um wafers

- FE-I4 sensors of 12 wafers are already tested and diced at IZM
    - two dicing positions
        - conventional dicing street
        - slim edge position (IBL constraints)
- IV measurements to compare the process steps
    - after UBM
    - after two dicing positions

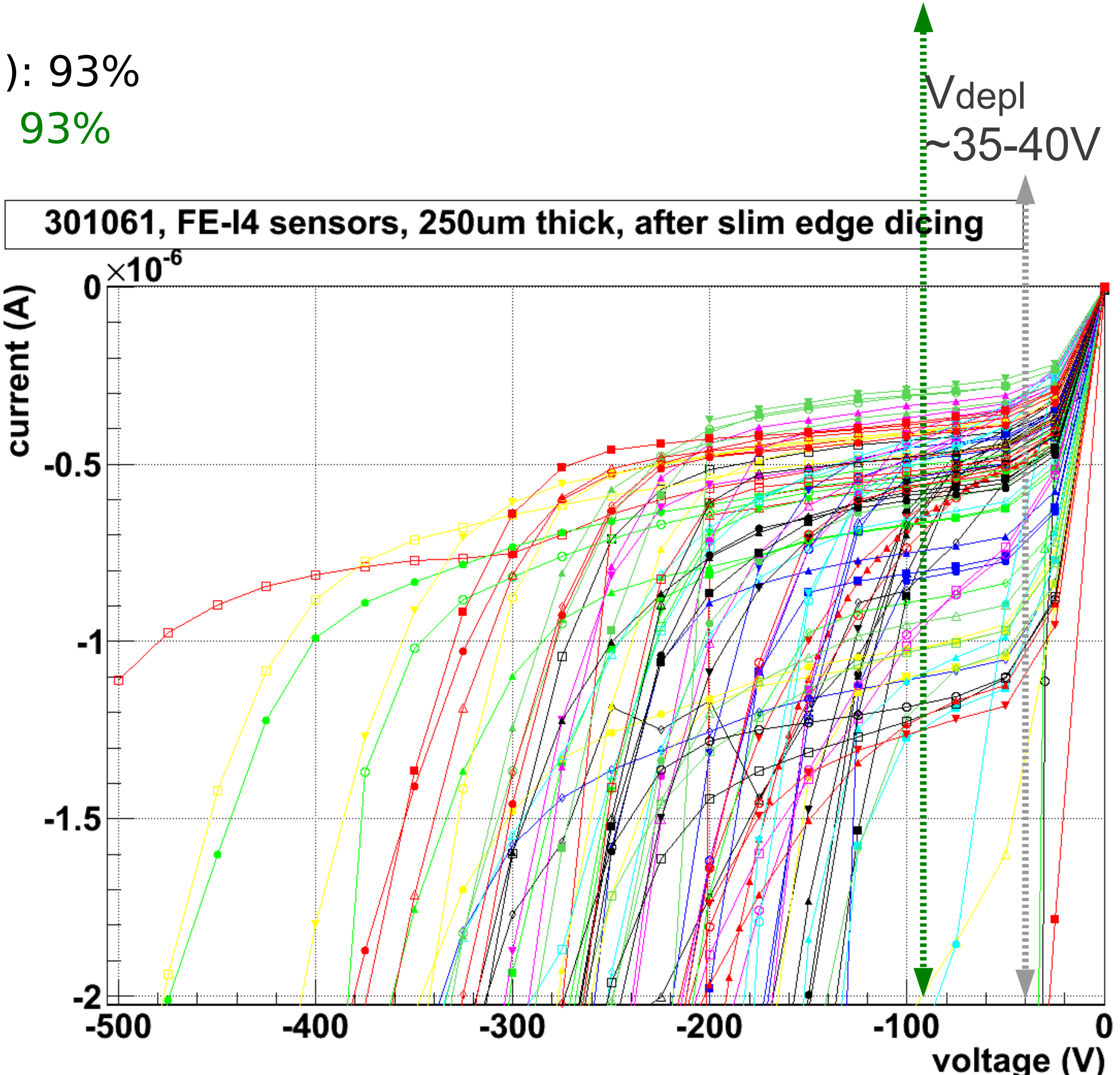




Status 250um wafers - results

- Vdepl ~=35-40V; quality criterium: Vbreakdown >= Vdepl + 50V ~= 90V
- yield (SC & MCM combined)
    - production (before UBM): 93%
    - IZM part: UBM + dicing: 93%
    - production + UBM + dicing: 86%
- Up to now 7+9 SCAs
- more sensors available

Vdepl + 50V



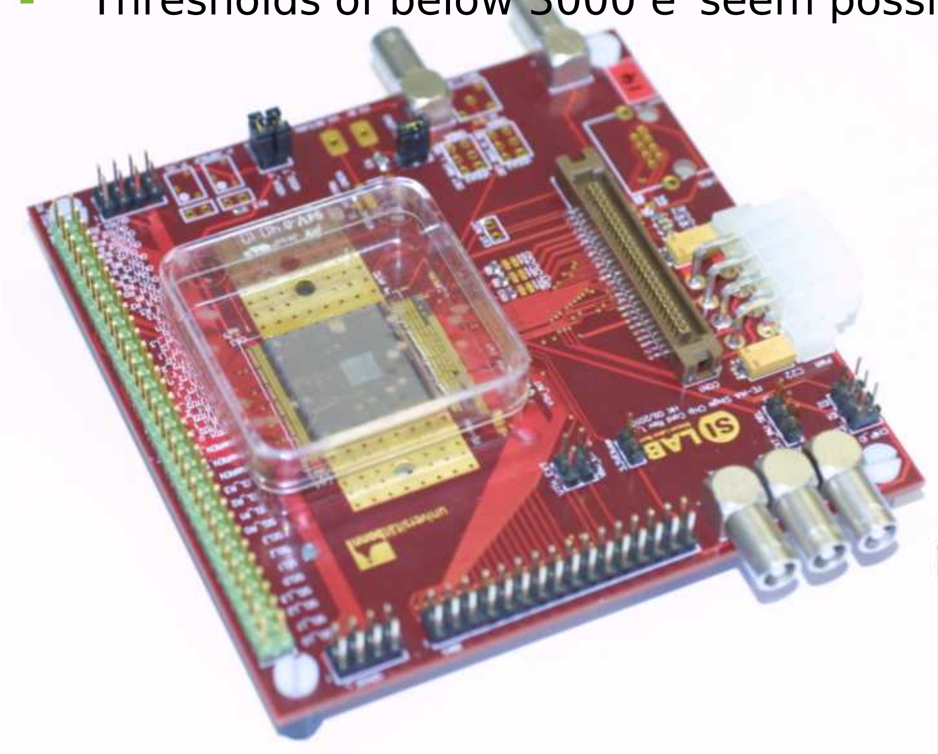
Vdepl ~35-40V

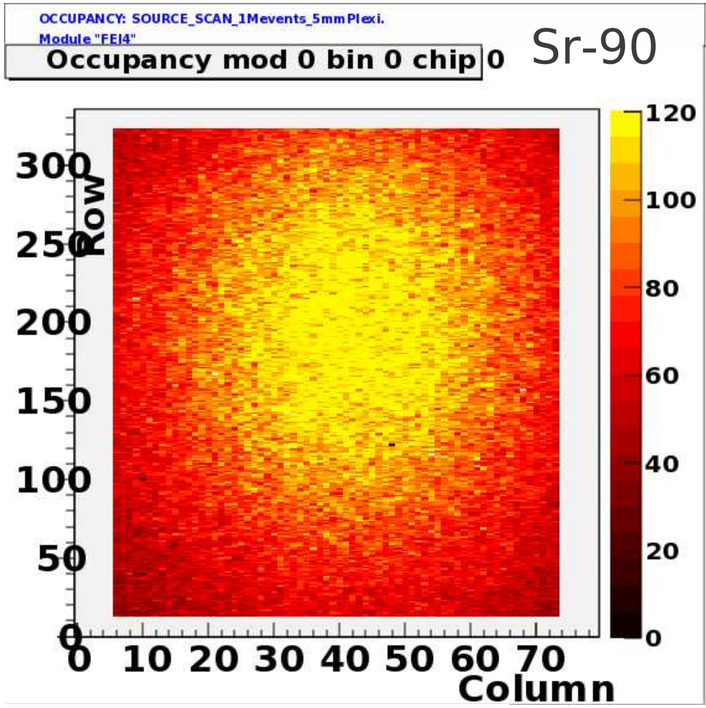
301061, FE-I4 sensors, 250um thick, after slim edge dicing

T. Wittig

First 250 µm sensor FE-I4 assem

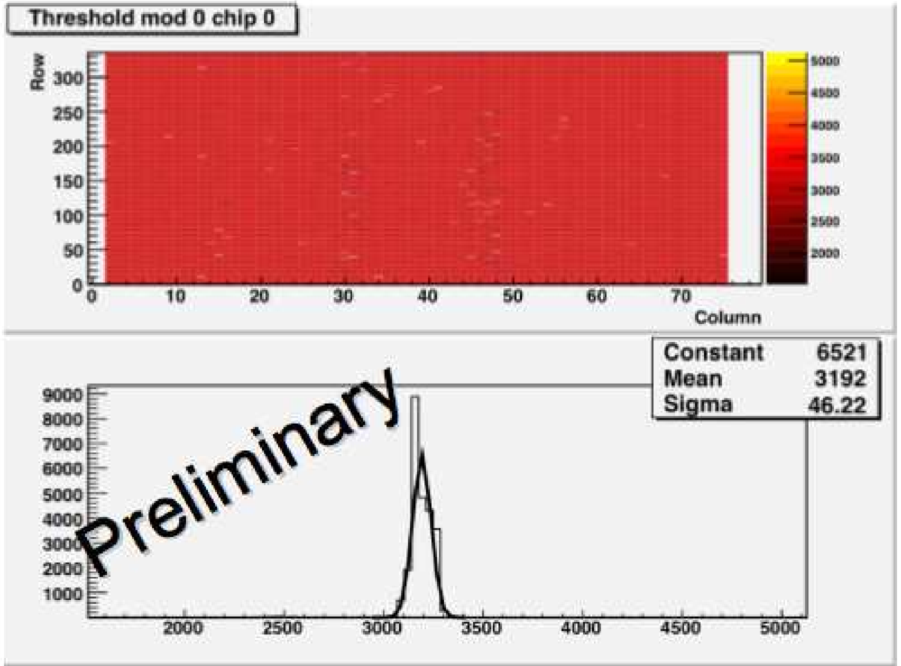
- First 7 assemblies under test and working well
- Thresholds of below 3000 e$^-$ seem possible





Sr-90

J. Jentzsch



- Currently: Testbeam with 6 assemblies at DESY

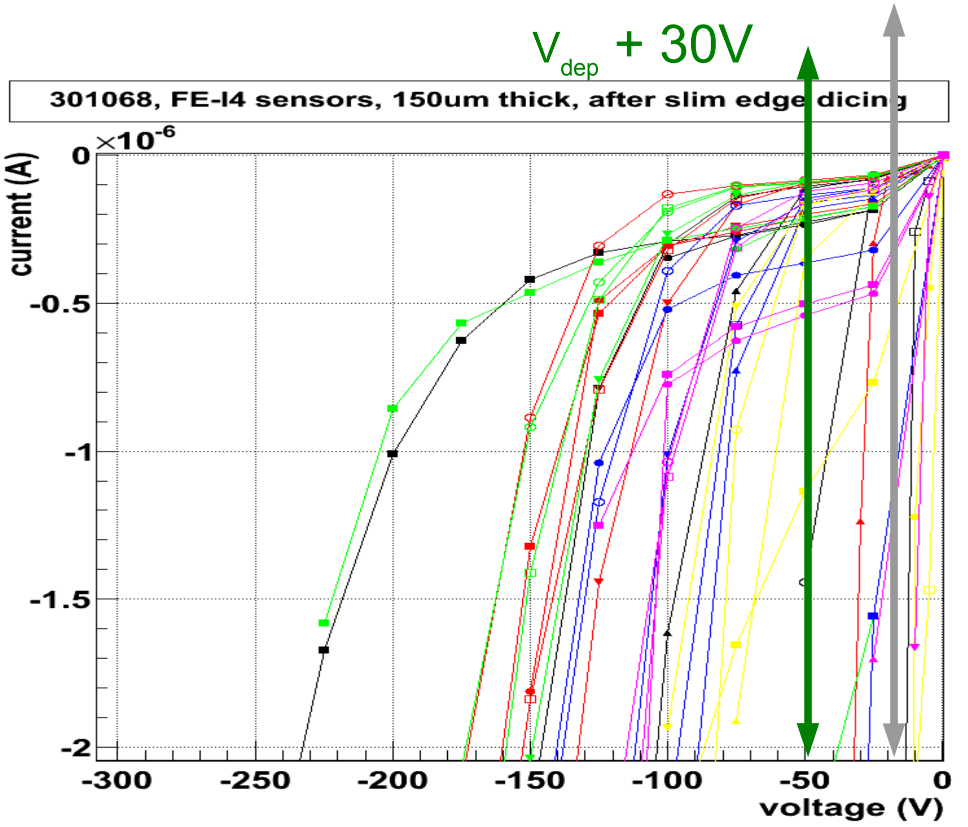
Status 150um wafers

- Vdepl ~=15-20V
- FE-I4 sensors of 6 wafers were already diced and tested at IZM
- IV measurements were done after slim edge dicing
- reduction of the breakdown voltage for most sensors
  - likely cause: dicing blade
- for $V_{breakdown} > V_{depl} + 30V$:
  - 83% yield (UBM + dicing)
- Several SCAs already available

T. Wittig

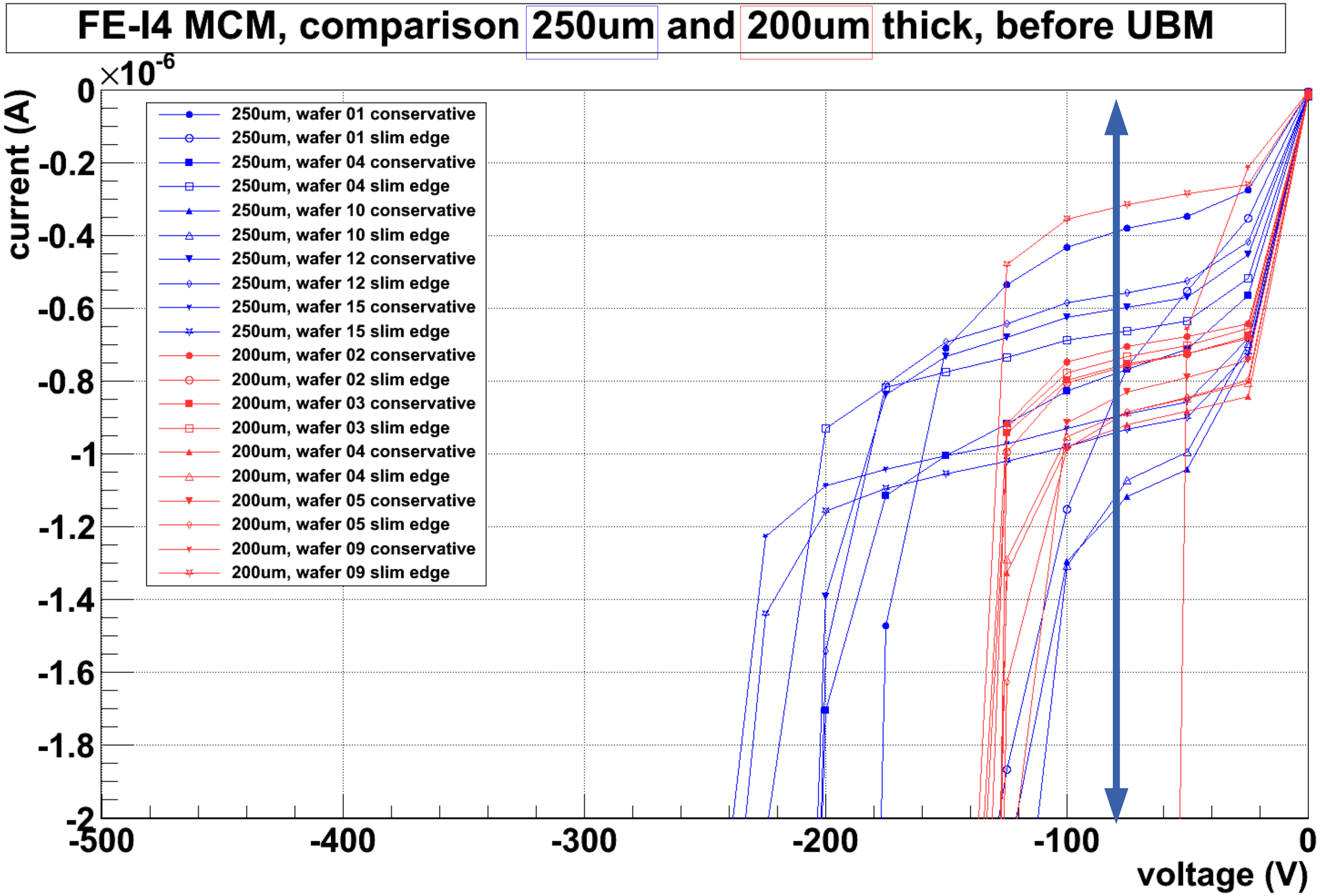
Vdepl
~15-20V

$V_{dep} + 30V$



Status 200um wafer

- UBM process finished and will be diced next week
- results from CiS (before UBM):
  - no differences of the yield are observed (compared to the 250um)
- 200 µm is the smallest thickness which IZM will process without using a handling wafer

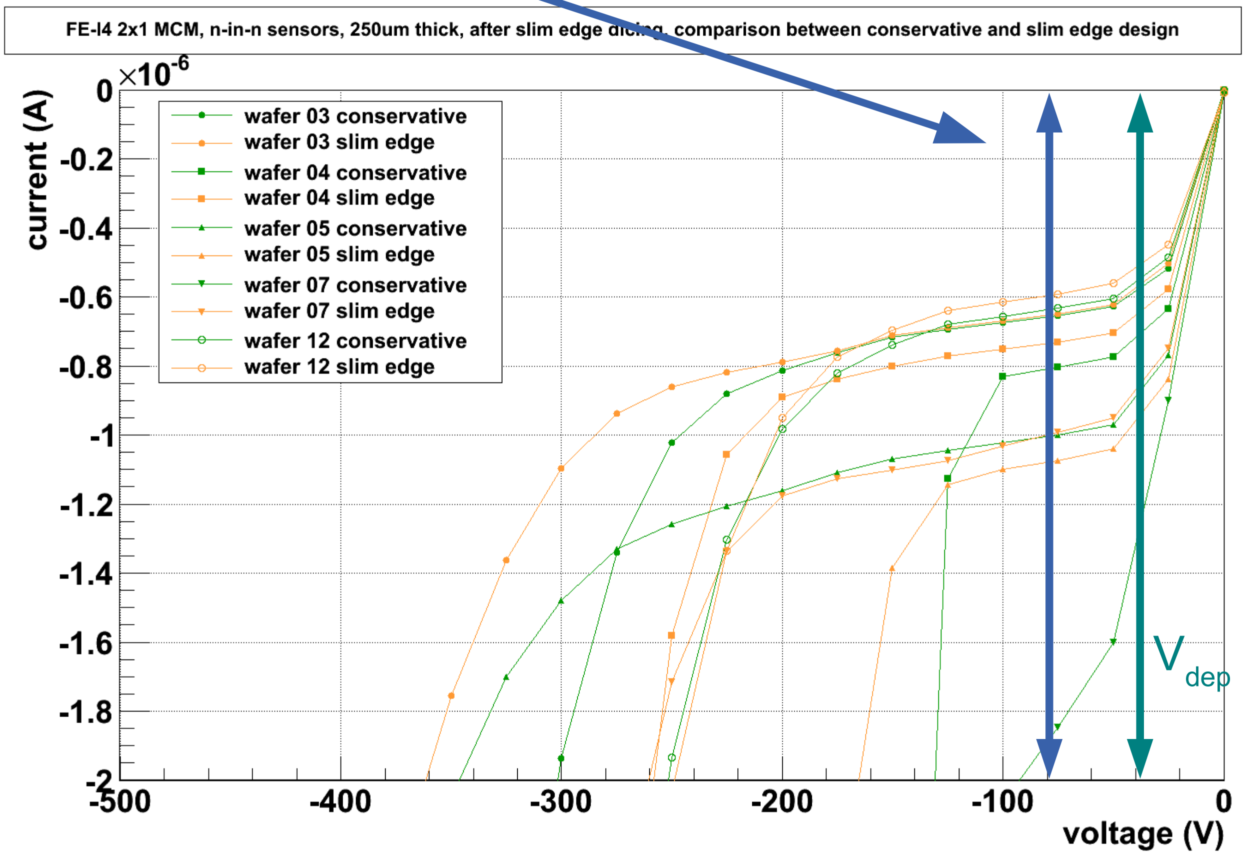


T. Wittig

Slim-edge yields

- First Measurement results: Total yield after dicing of 72 structures
  - Conservative design (2-chip and 1-chip): 86%
  - Slim-edge design (2-chip and 1-chip): 86%
  - 2-chip yield (conservative+slim-edge): 79%
  - 1-chip yield (conservative+slim-edge): 90%
- Yield is based on $V_{breakdown} > V_{depletion} + 50V$
- (Only) concern:
  early breakdown
- No difference observed between conservative and slim-edge (as expected!)
- Yield scales with sensor area (as expected)

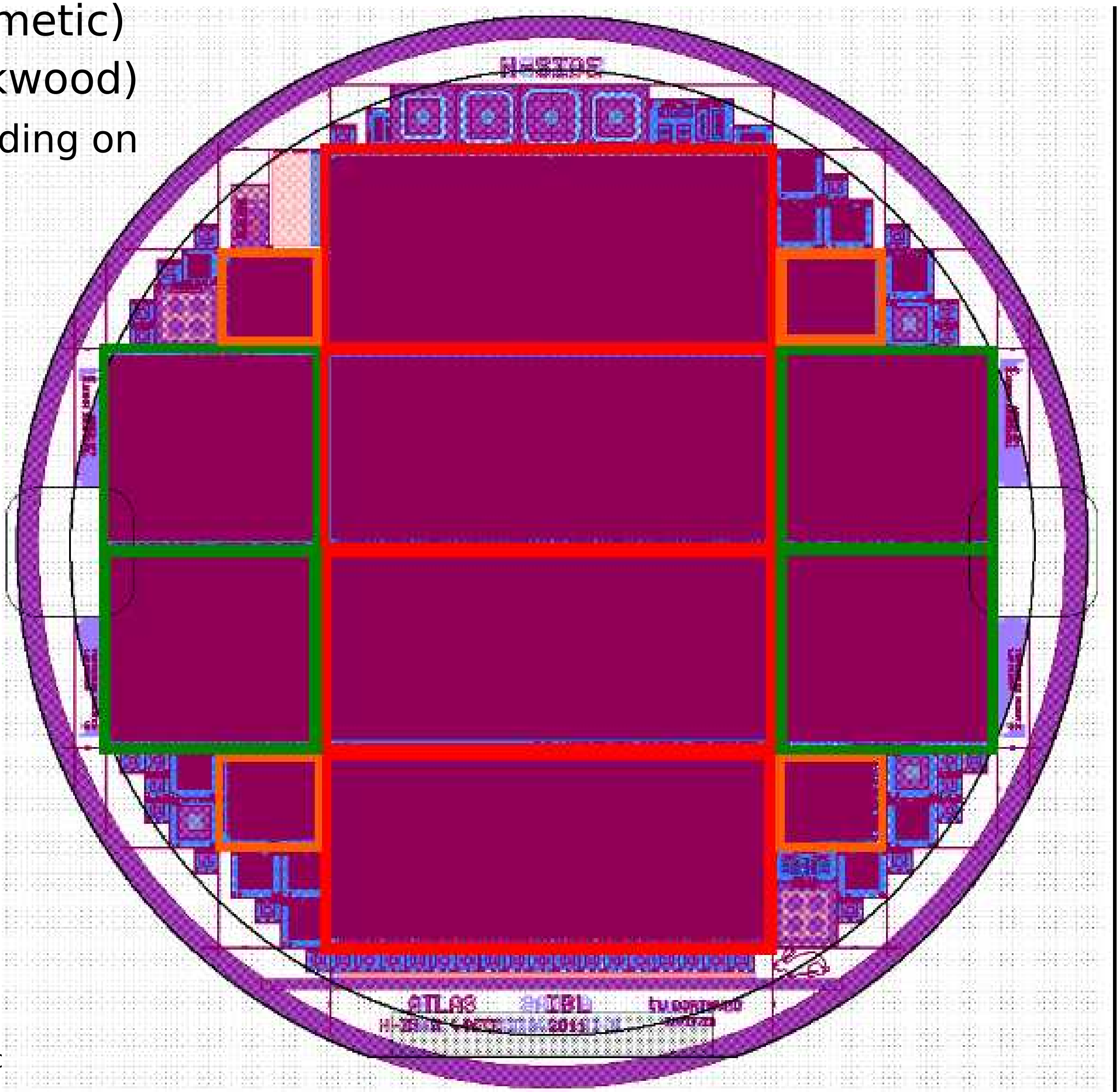
→ go for n-bulk slim-edge



T. Wittig

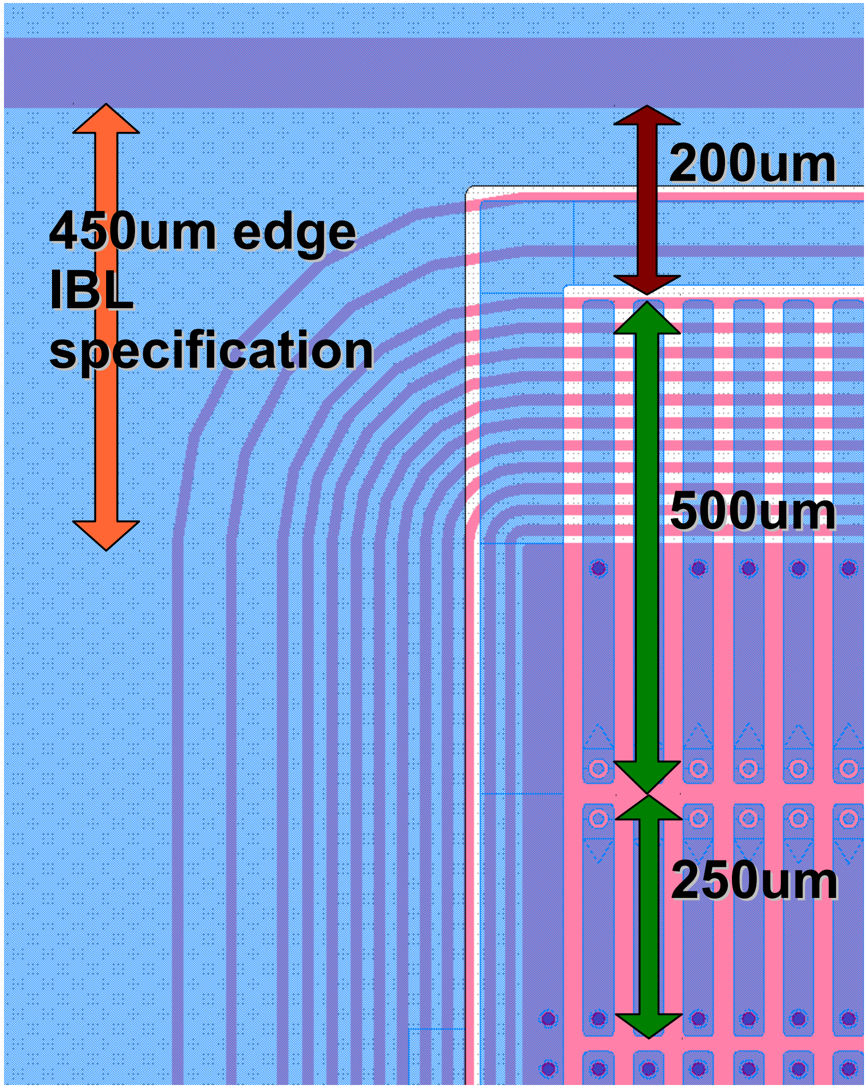
The planar IBL production wafer

- thinning and polishing of raw wafers is outsourced:
  - 250um – 100 wafers (Okmetic)
  - 200um – 50 wafers (Rockwood)
- will decide by mid-march depending on
  - thinning results
    200 µm UBM/flipping experience
- 4” n-bulk wafer
  - slim-edge design
  - 4 FE-I4 2x1 MCMs
  - 4 FE-I4 SCs
  - 4 FE-I3 SCs
  - diodes
  - test structures



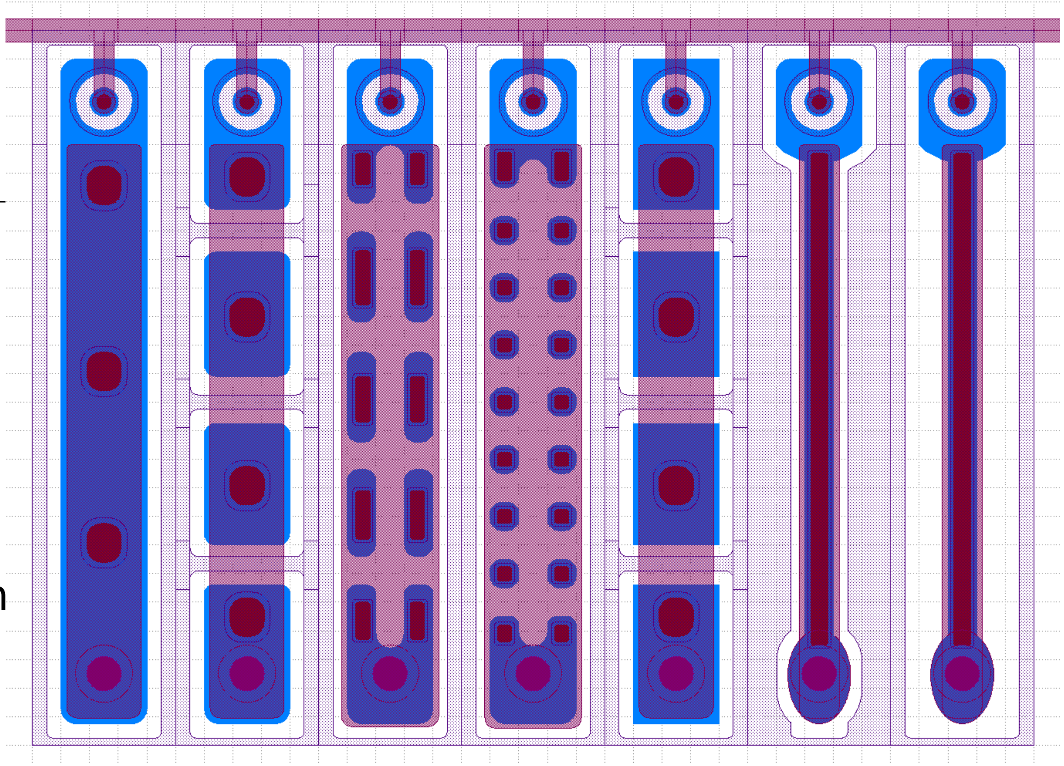
FE-I4 sensor design

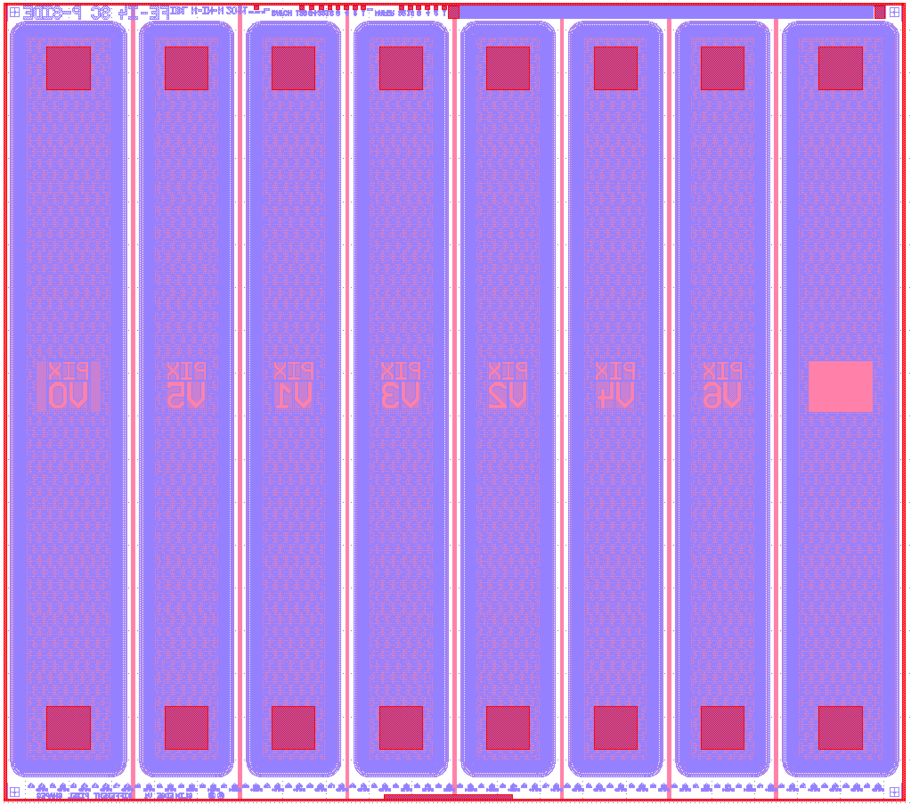
- we decided to use the “slim edge” design:
  - with long pixels (500um)
  - 13 guard rings shifted 250um beneath the pixels to reduce the inactive area
  - no disadvantage in comparison to the conservative design
  - only ~200-250um inactive edge expected
- same design for the MCMs and for the SCs
  - for comparability



segmented FE-I4 SC

- on one FE-I4 SC we implemented pixels with different shaped implantations
  - to enforce different field configuration
  - study of charge amplification at high fluences
- always 5 double columns contain same pixel version
  - every double column will only see one sort of pixels (same capacities)
- The HV-pad is segmented into strips
  - the different pixel versions can be operated seperately
  - possibility to do slim edge studies with two double columns (of each version) opposite of guard rings

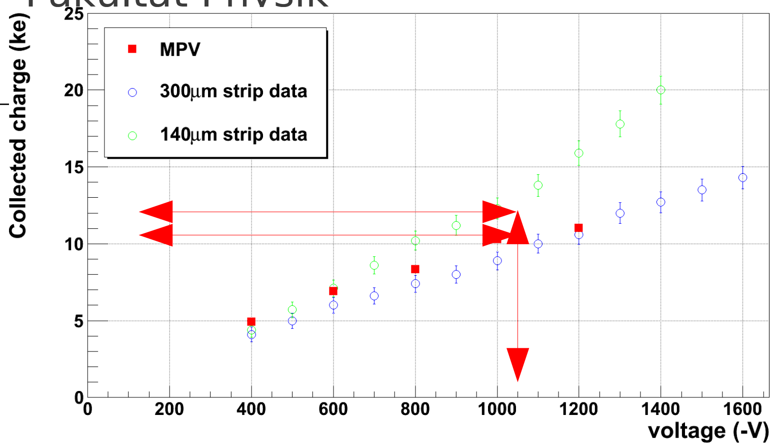




Time schedule

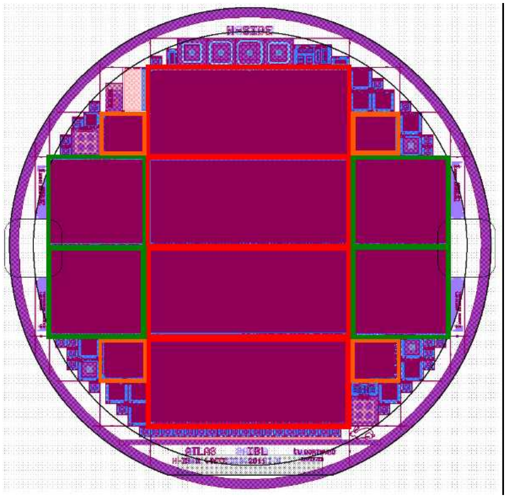
- final design review was held on January 28th
- after final changes the design was submitted to CiS in the begin of February
- 50 wafers will be ordered in March
- time table:
  - Mid-January the wafer-thinning was ordered
    - 4-6 weeks delivery time
  - ~ mid-March: start processing at CiS
    - 16-18 weeks processing time
  - ~ mid-July: wafers delivered from CiS
    - start UBM & dicing at IZM, ~4-6 weeks
  - -> ~ end of August: ~150 2-chip sensors available for flip chipping

- Subsequent order of ~100 wafers could (should?) be placed soon
  - would allow to get ahead of schedule



Conclusions and Outlook

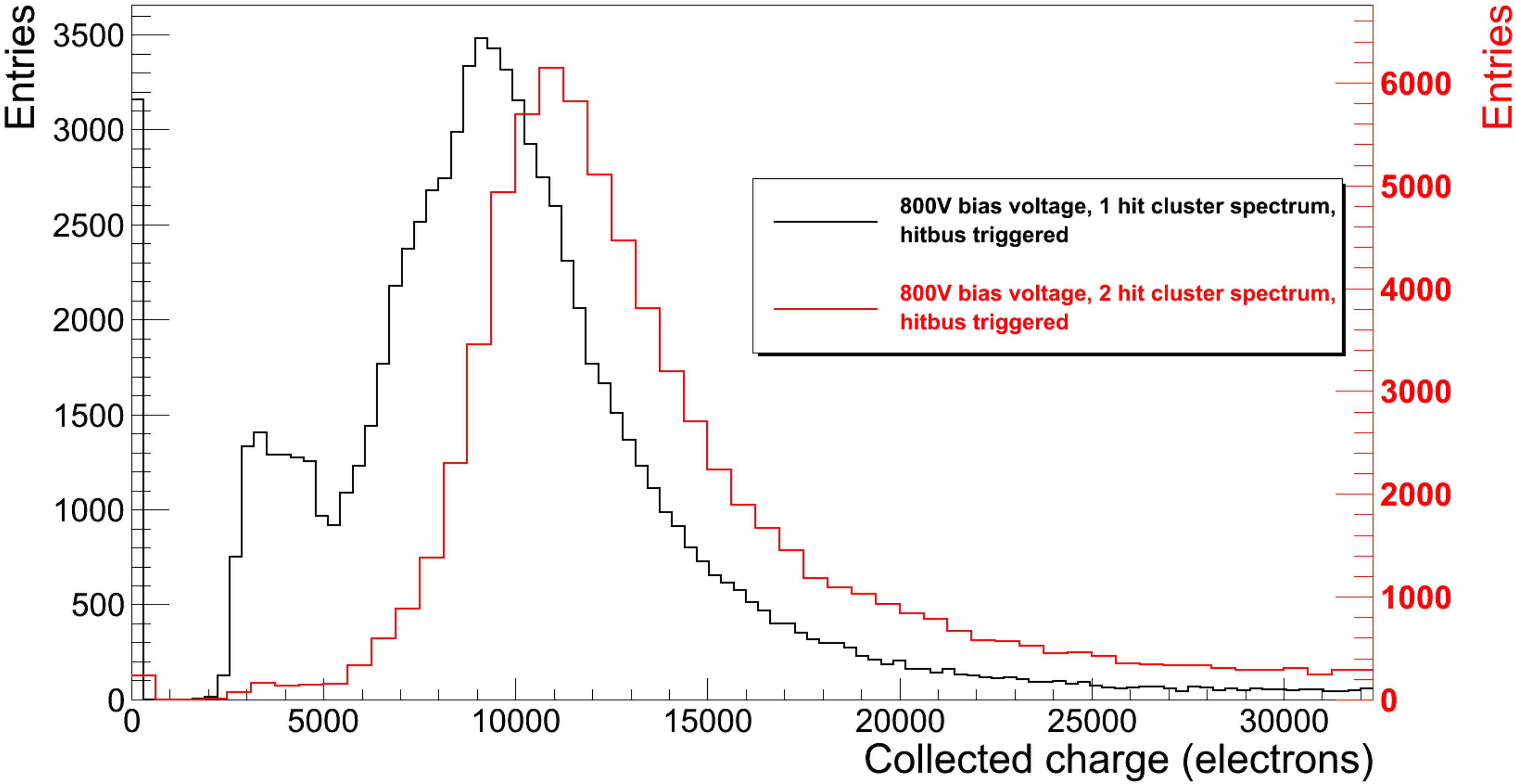
- Planar sensors have been shown to yield more than 10 ke$^-$ after $5 \cdot 10^{15}$ n$_{eq}$/cm^2 at 1 kV
  - this should be sufficient for good efficiency with FE-I4 and will be demonstrated soon
- Operation of irradiated pixel detectors tricky
  - Sensors ok, but currently available readout chips not rad-hard enough → FE-I4 now available, crosscheck with analog readouts
- Planar pixel sensors still yield charge at 'SLHC innermost layer' conditions
- Lot of progress in the last three years
- The n-bulk IBL sensor qualification production was very successful
  - high yield (~80% for 2-chip modules)
  - slim-edge design (~200-250 µm inactive edge) working well
  - first FE-I4 modules in the testbeam at DESY as we speak
- Planar IBL (pre-)production
  - wafer design has been submitted
  - delivery expected by mid-July



Backup

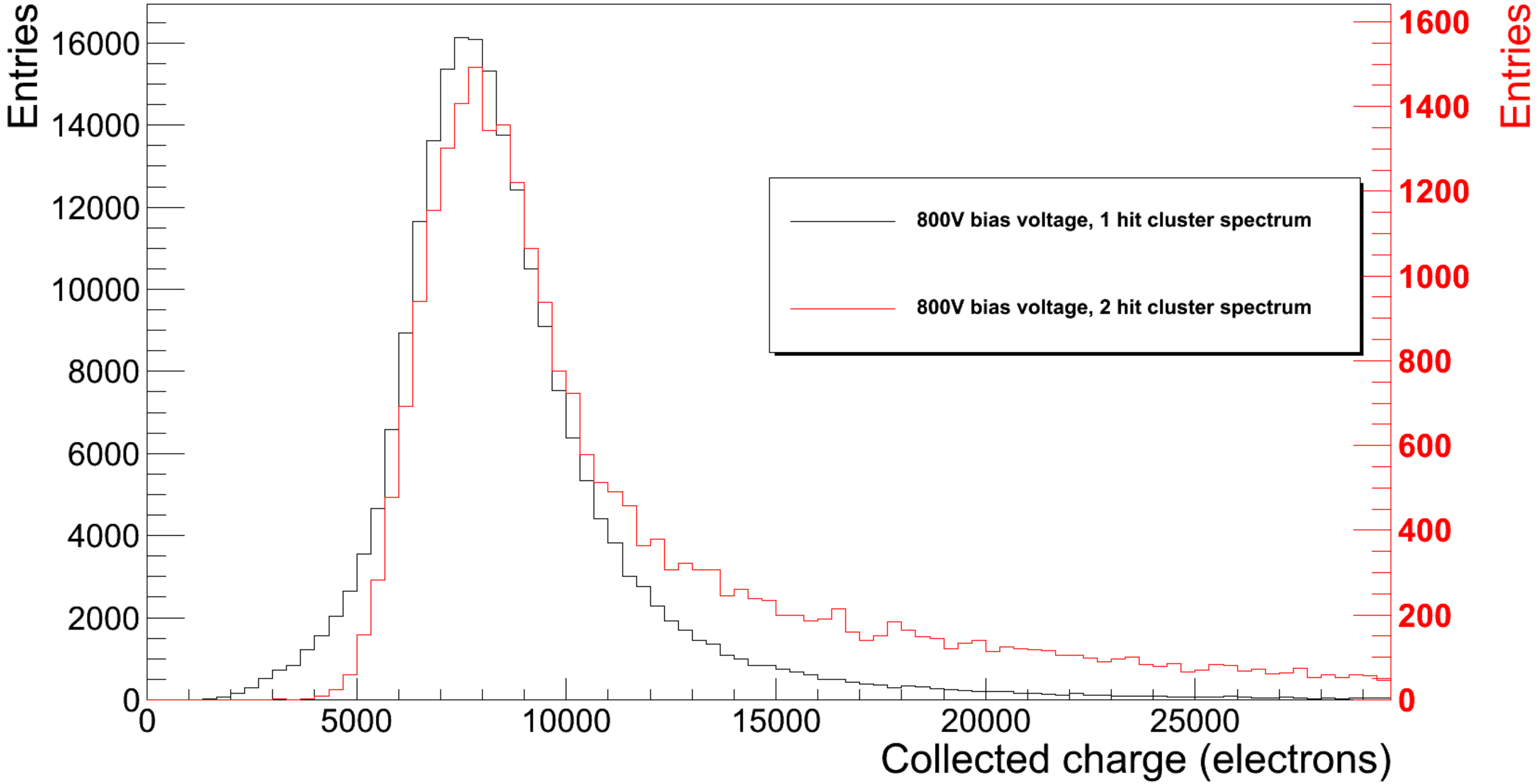
$5 \cdot 10^{15}$ n_{eq}/cm² @ 800V, Sr-90 electrons

- Difference between cluster charge of 1-hit and 2-hit clusters:



$5 \cdot 10^{15}$ n_{eq}/cm² @ 800V, pions

- With pions, this effect is negligible



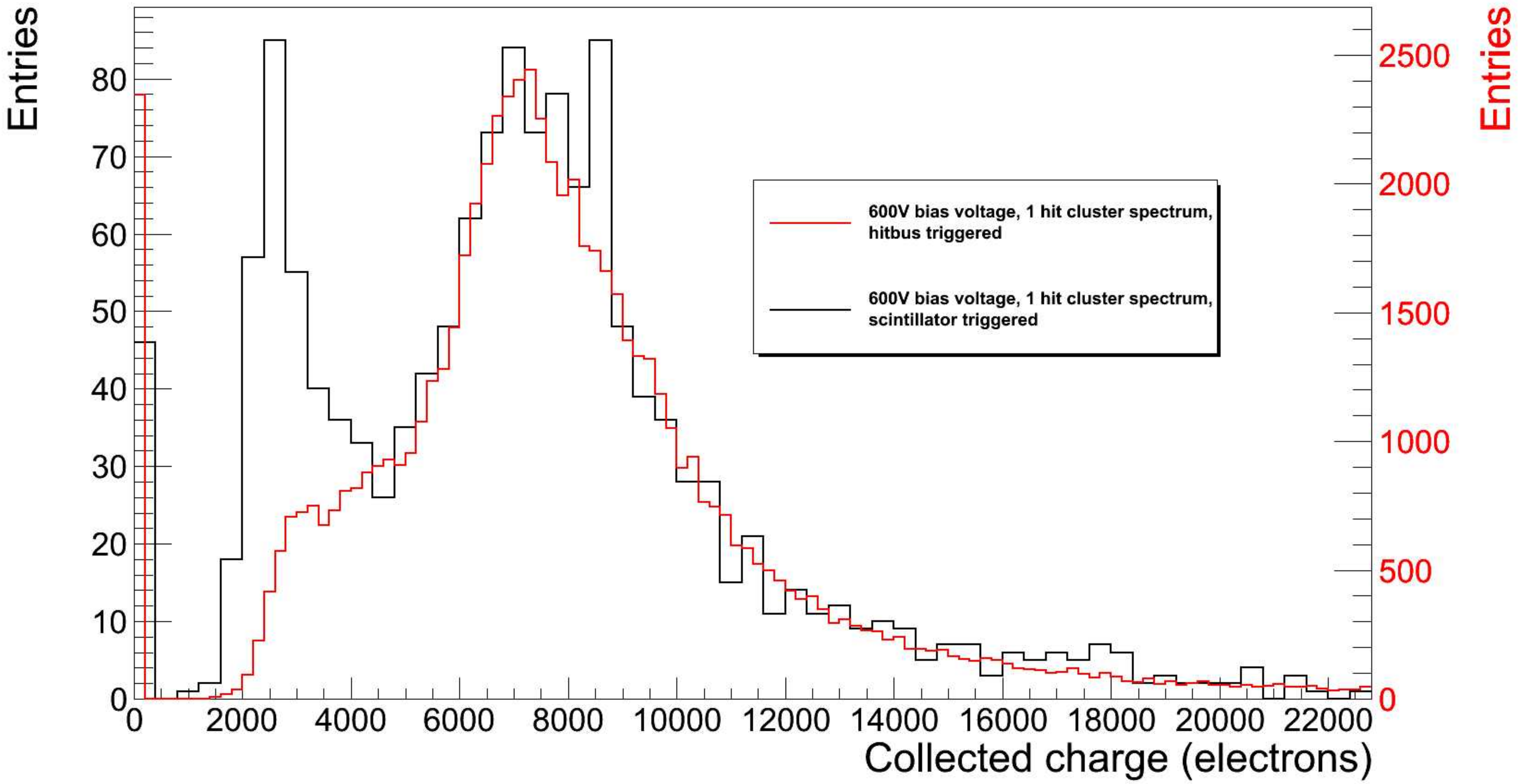
1 hit vs. 2 hit clusters

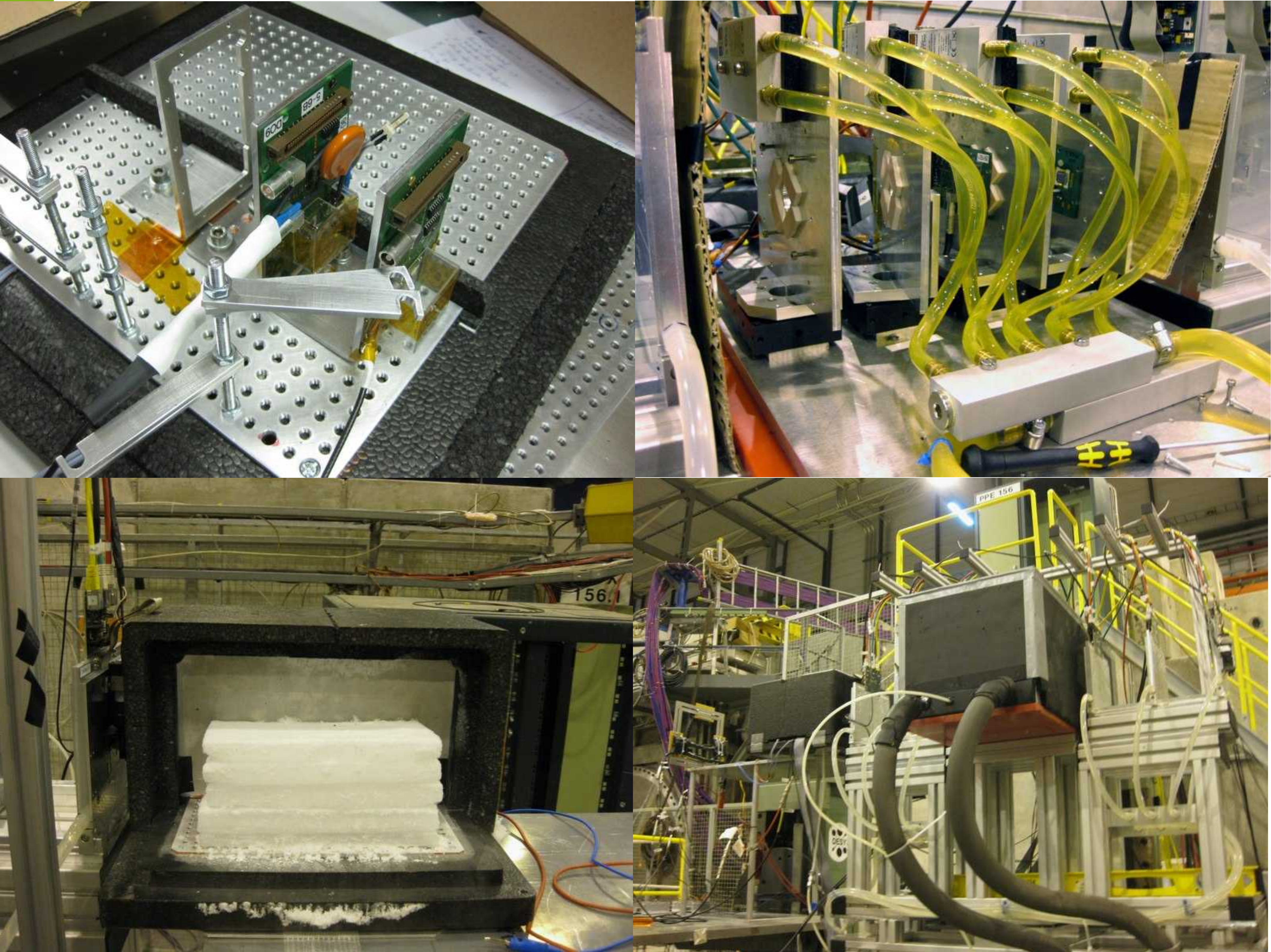
- For testbeam data with high energy pions there seems to be little difference between the charge spectra of 1-hit and 2-hit clusters.
- Low energy electrons (Sr-90) show increased charge deposition for two hit clusters

  → Only 1 hit clusters regarded for Sr-90 data, conservative choice

Trigger: $5 \cdot 10^{15}$ n_{eq}/cm² 600V electrons

- No visible difference for MPV between scintillator and hitbus-triggered data

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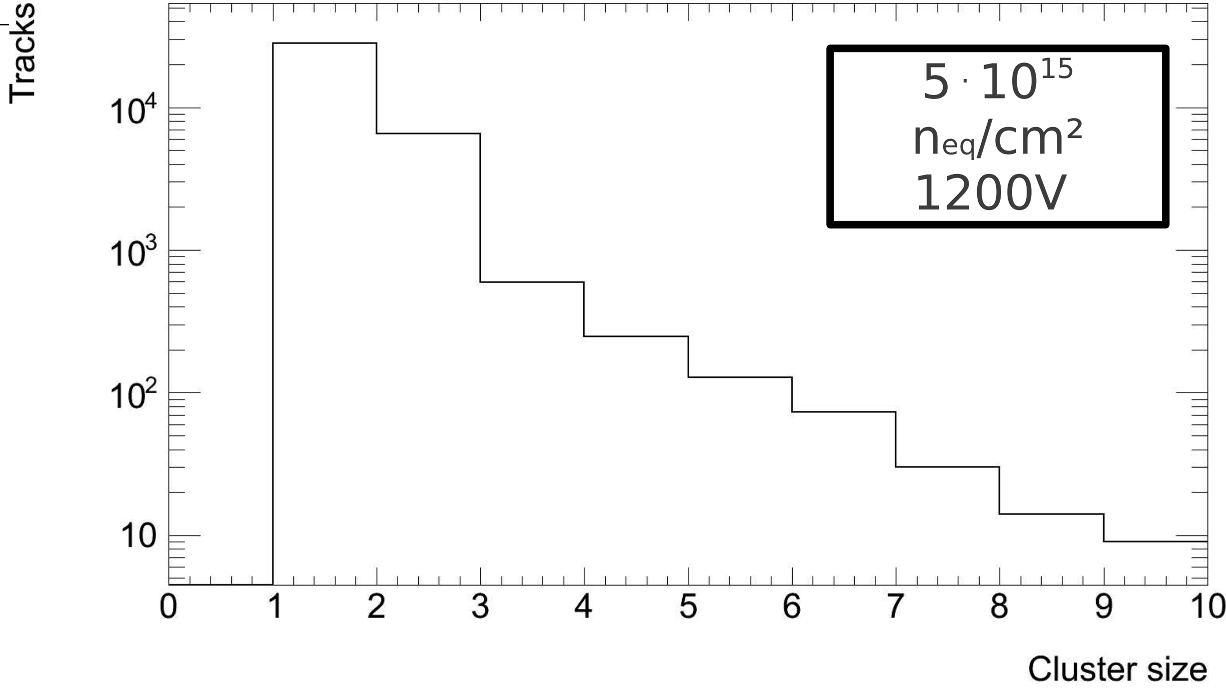
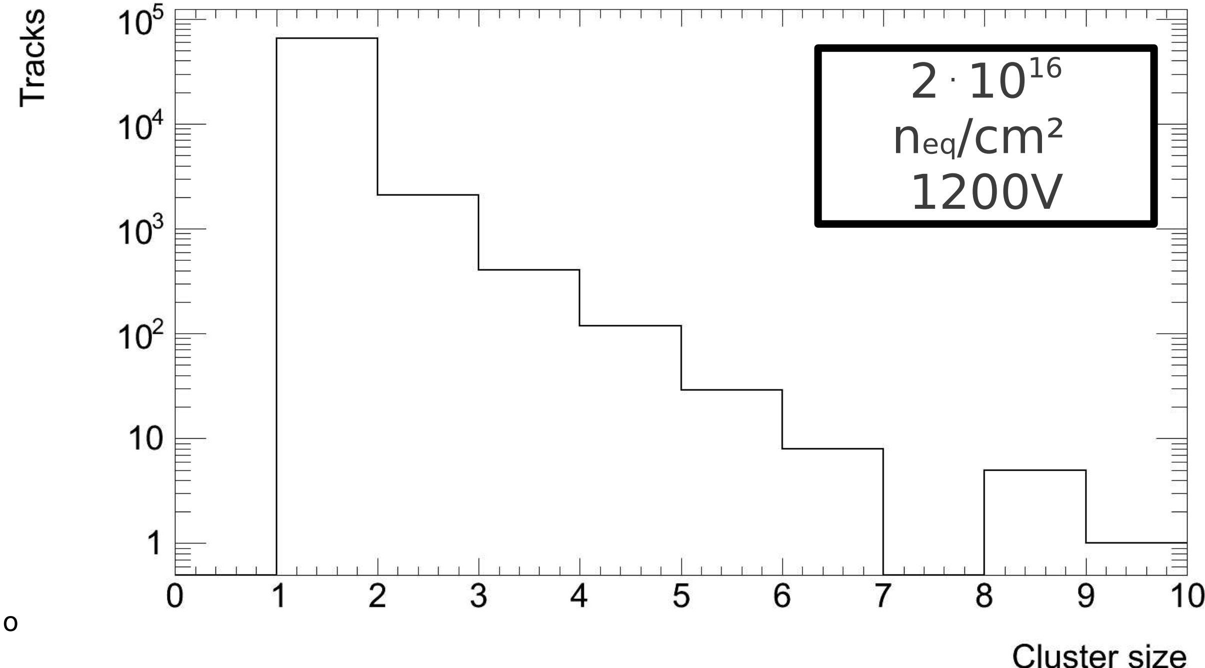
Charge sharing?

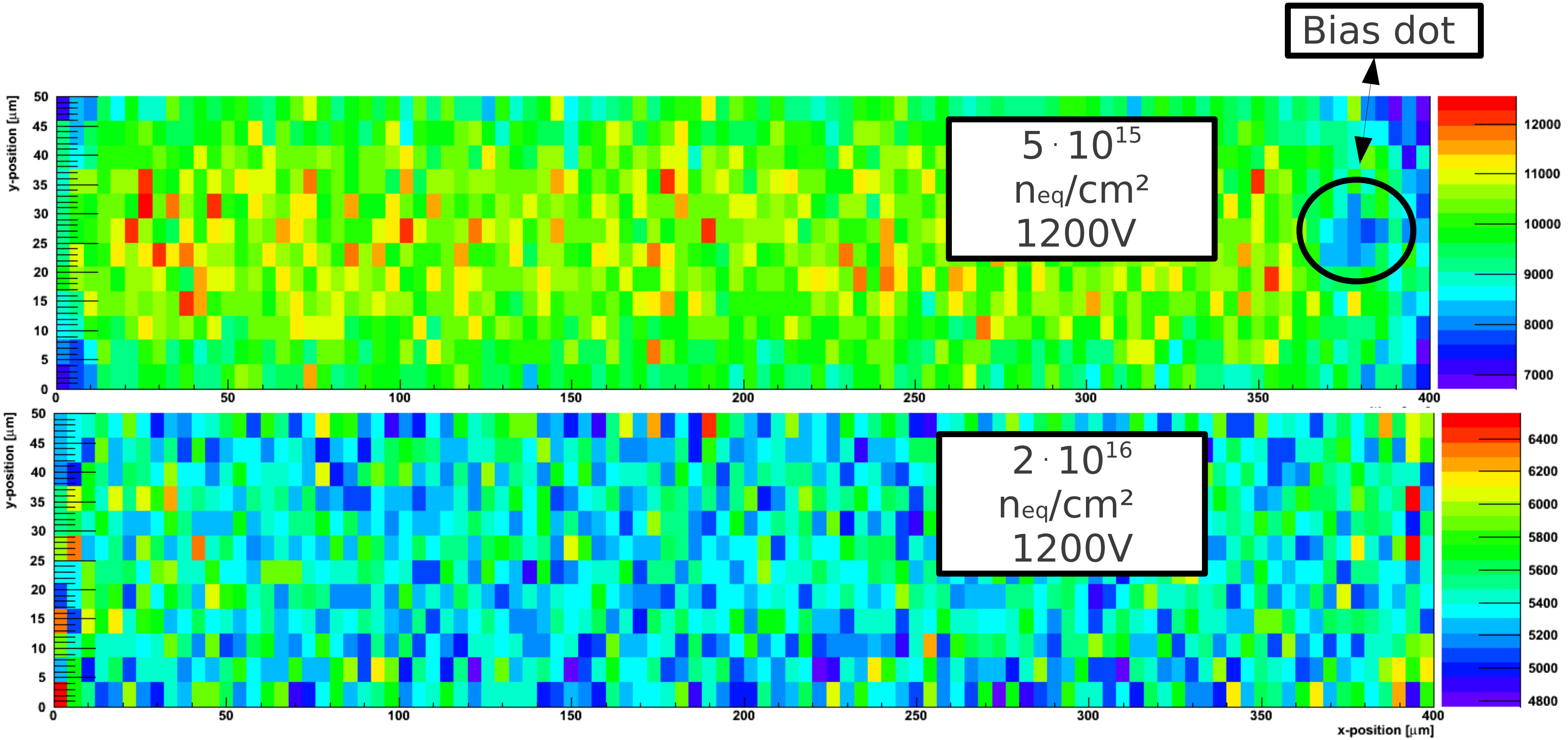
- Single-hit cluster fraction grows with fluence (as expected)
- (Much) more shared charge not seen due to threshold effect in the neighbouring pixel
- Scattering is larger with electrons, might (partially) explain lower observed charge with electrons





Where is charge lost?

- In a testbeam, the telescope allows to trace how much charge was observed by pions traversing the sensor at a given point
- Resolution of the EUDET telescope o(<10µm), pixel 50µm by 400µm
- $5 \cdot 10^{15}$ n_{eq}/cm^2: less charge in corners and at the bias dot
- $2 \cdot 10^{16}$ n_{eq}/cm^2: rather homogenious → alignment problem?



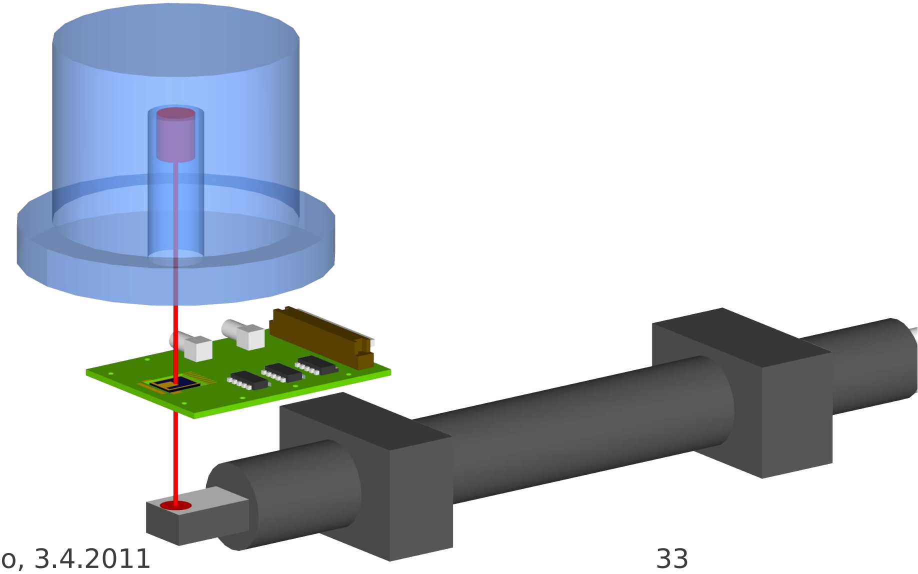
Bias dot

$5 \cdot 10^{15}$
n_{eq}/cm^2
1200V

$2 \cdot 10^{16}$
n_{eq}/cm^2
1200V

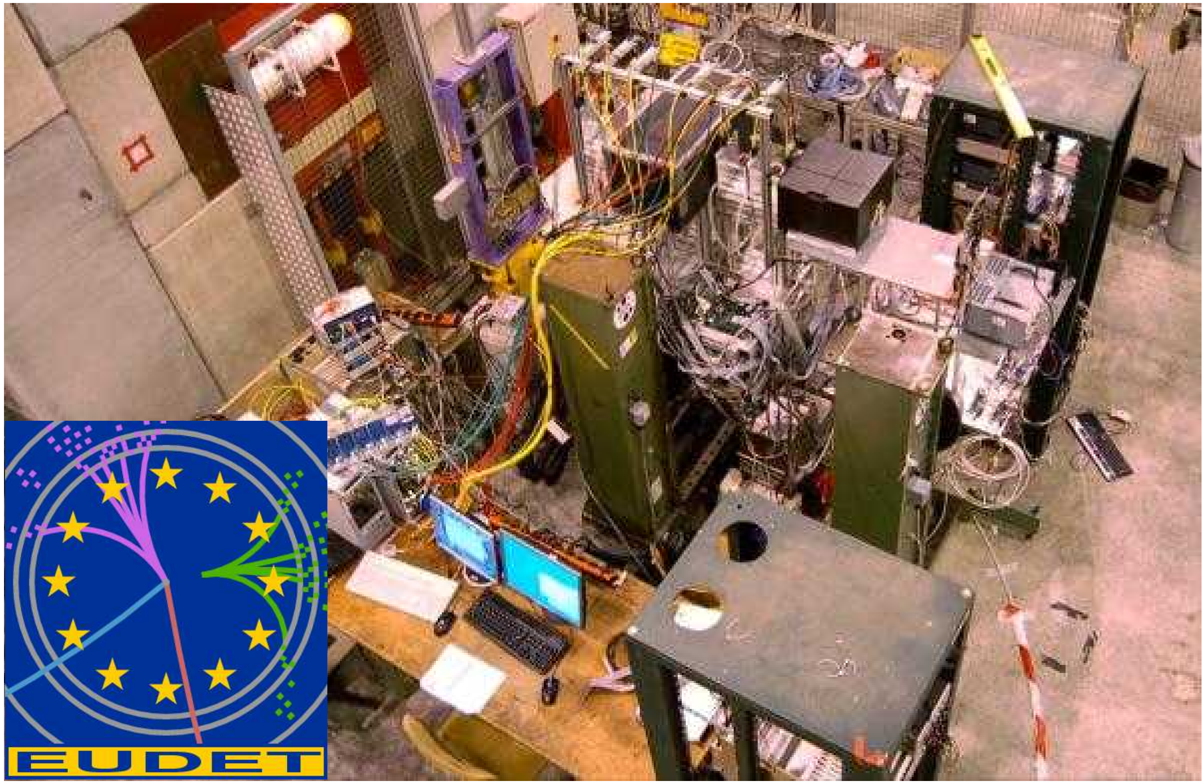
Experimental Methods: electrons

- ^{90}Sr beta electrons:
  - Charge Collection Efficiency measured with a Sr-90 source (landau expected)
  - Operation temperature below -55°C with dry ice in a insulated box
  - Standard ATLAS TurboDAQ readout (already used during the production process)
  - Two possible triggers:
    - trigger scintillator beneath the sensor, only through-going electrons
    - (internal) hitbus trigger, all electrons
- Advantages:
  - easily accessible
  - study of many parameters possible
- Disadvantages:
  - much scattering
  - “no real MIPs”



The PPS Testbeam

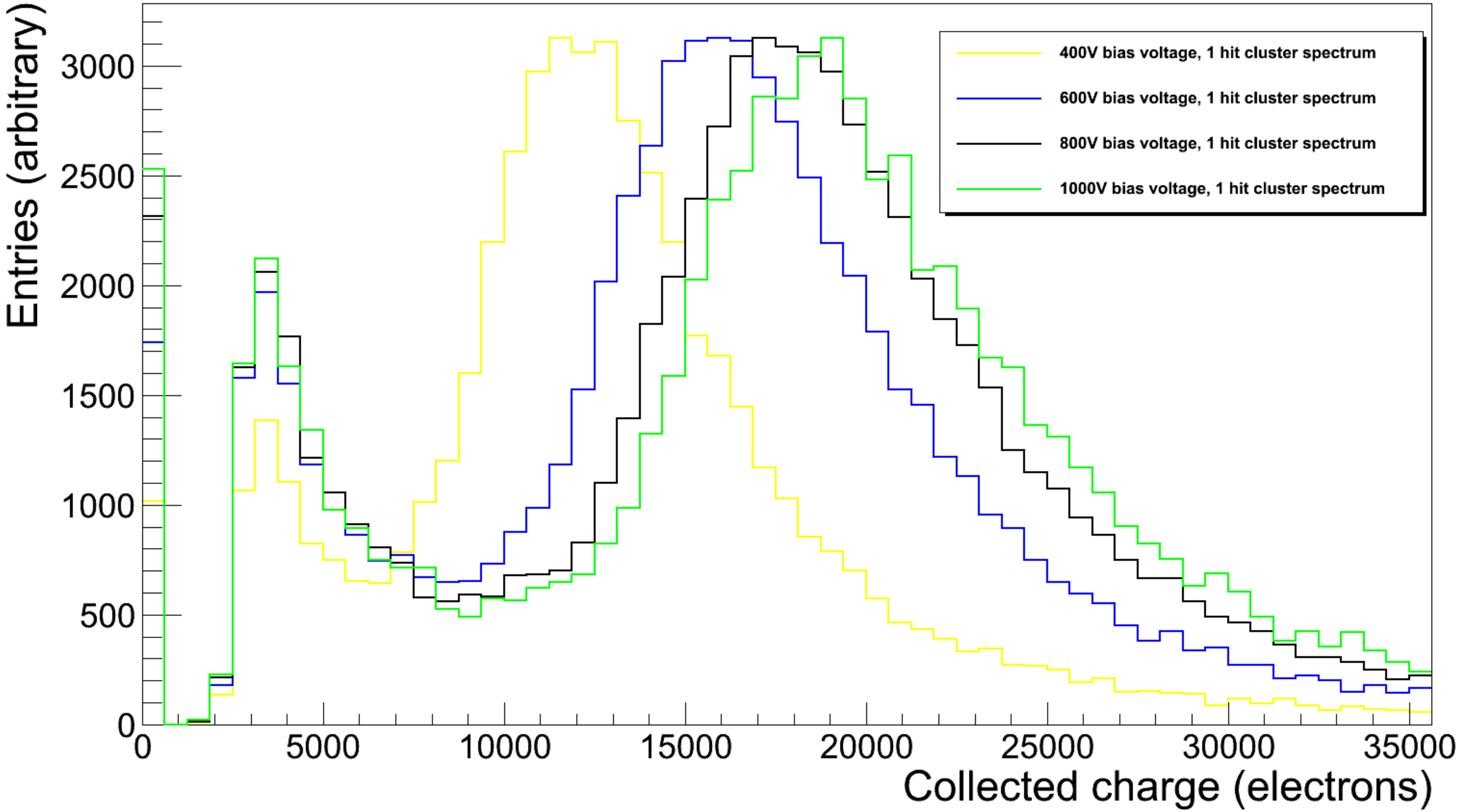
- Testbeam data taken in July and October 2010 at CERN H6B beamline
- EUDET telescope used together with ATLAS pixel specific hard- and software extensions
- Allows to take space resolved data
- Samples were cooled with dry ice in a lab proven system
- Data analysis ongoing



The PPS Testbeam group

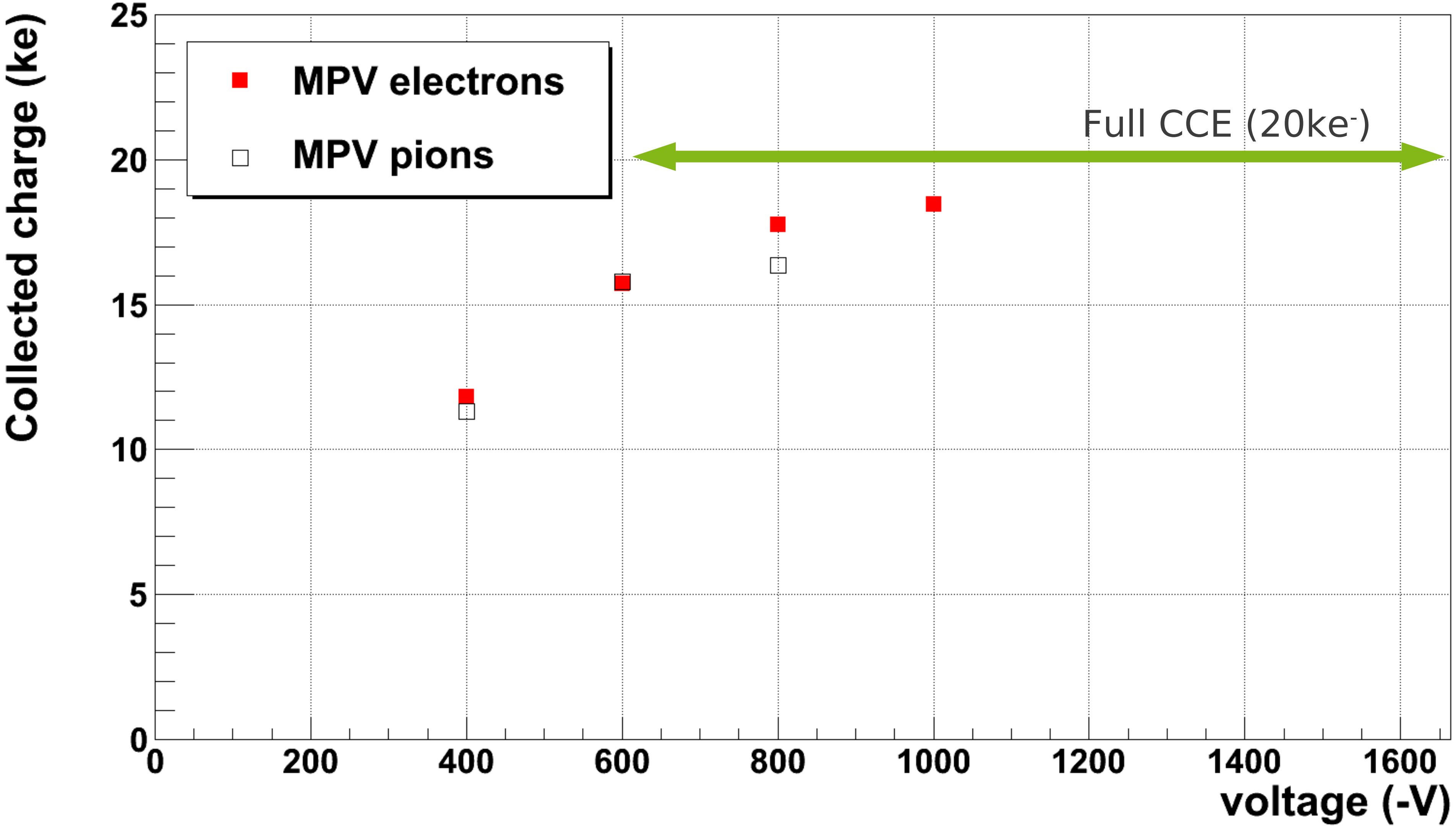
Jens Weingarten,
M. Beimforde, M. Benoit, M. Bomben, G. Calderini, Ch. Gallrapp, M. George, S. Gibson, S. Grinstein, Z. Janoska, J. Jentzsch, O. Jinnouchi, T. Kishida, A. La Rosa, V. Libov, A. Macchiolo, D. Muenstermann, R. Nagai, G. Piacquadio, B. Ristic, I. Rubinsky, A. Rummler, D. Sutherland, Y. Takubo, G. Troska, S. Tsiskaridze, I. Tsurin, Y. Unno, P. Weigell, T. Wittig

$1 \cdot 10^{15}$ n_{eq}/cm^2 with Sr-90 electrons

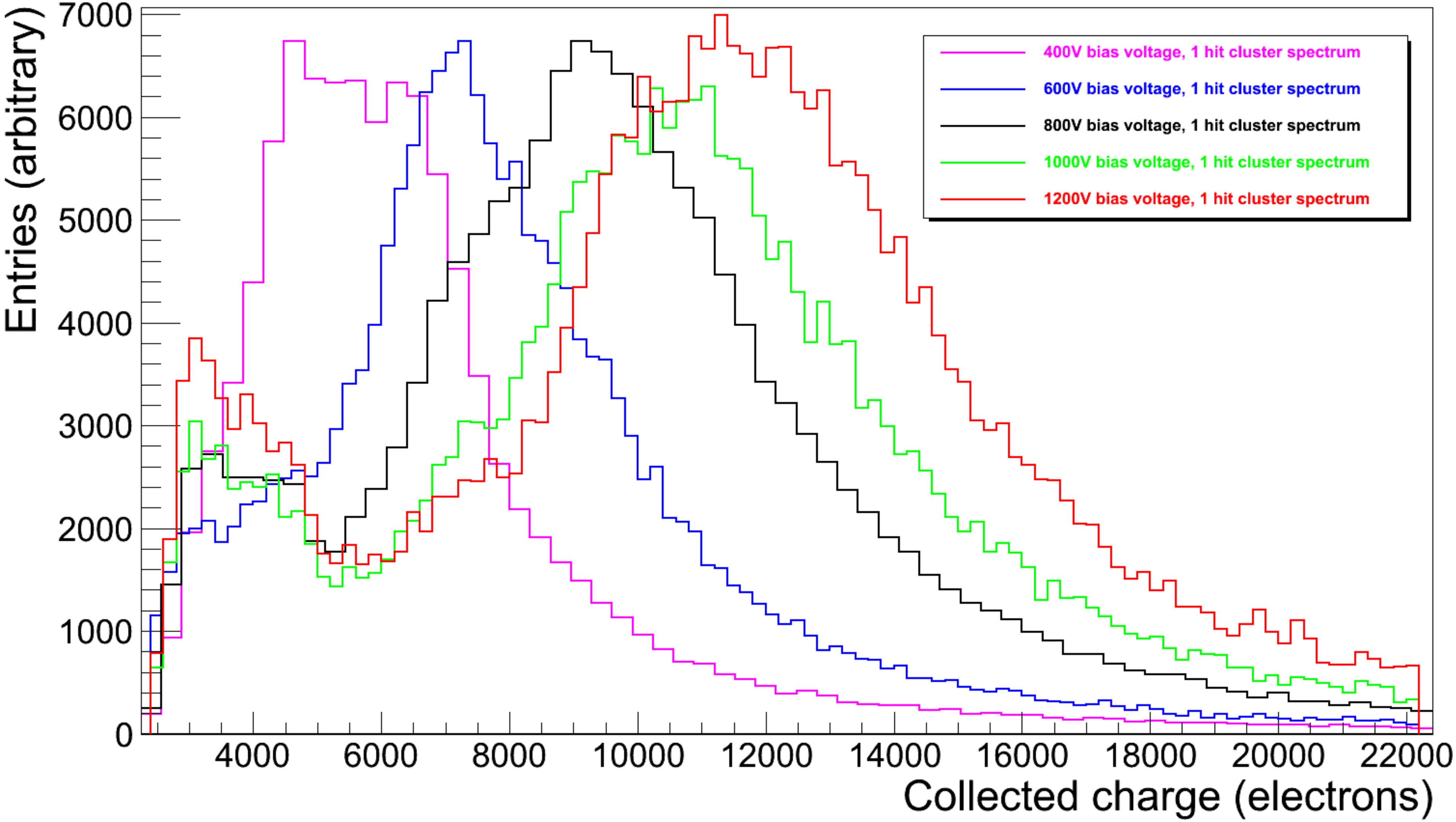


$1 \cdot 10^{15}$ n_{eq}/cm² charge collection summary

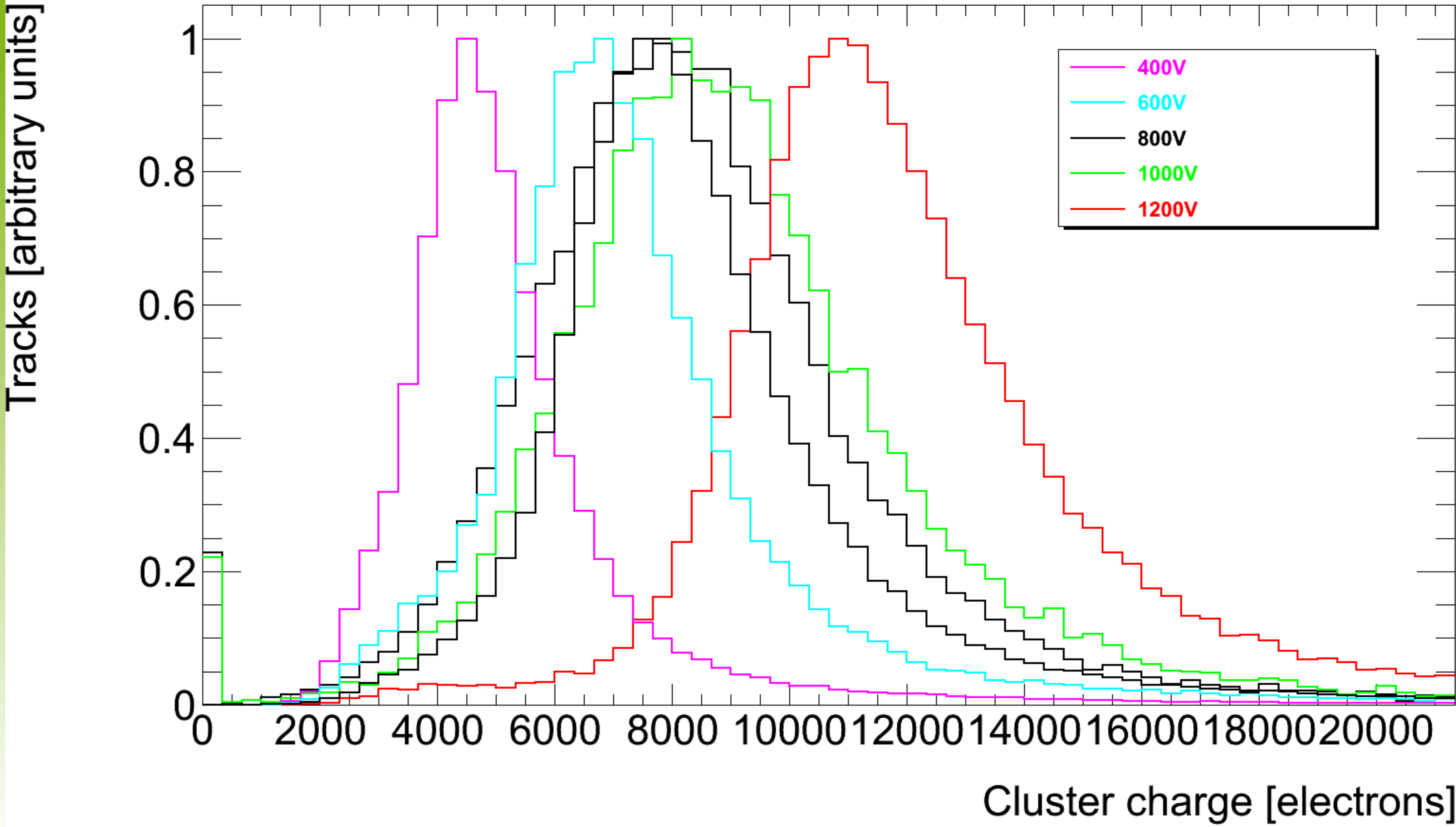
- satisfactory results: 16 ke$^-$ at 600V, almost full CCE at 1kV
- agreement with pion measurements



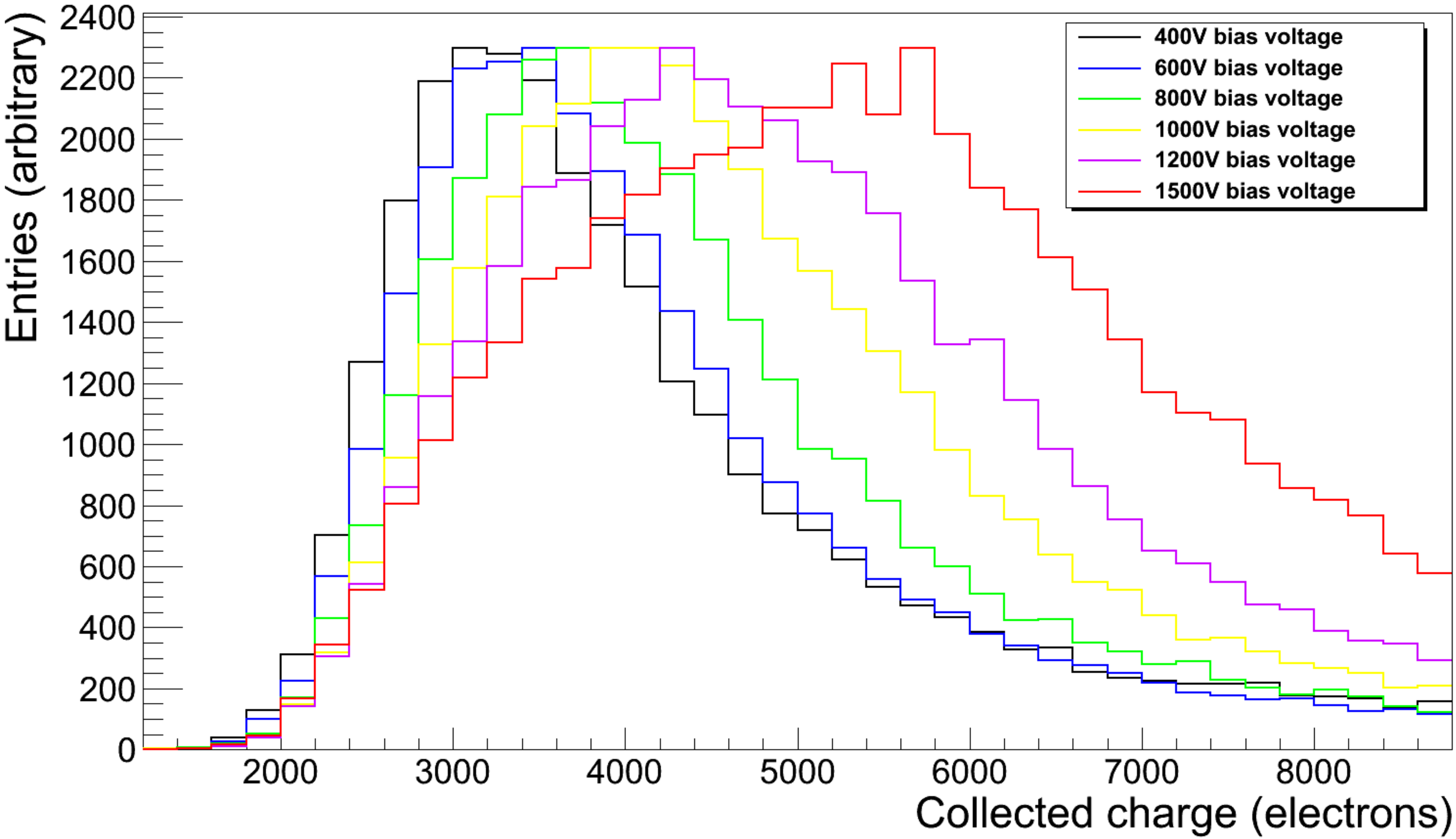
$5 \cdot 10^{15}\ n_{eq}/cm^2$ with Sr-90 electrons



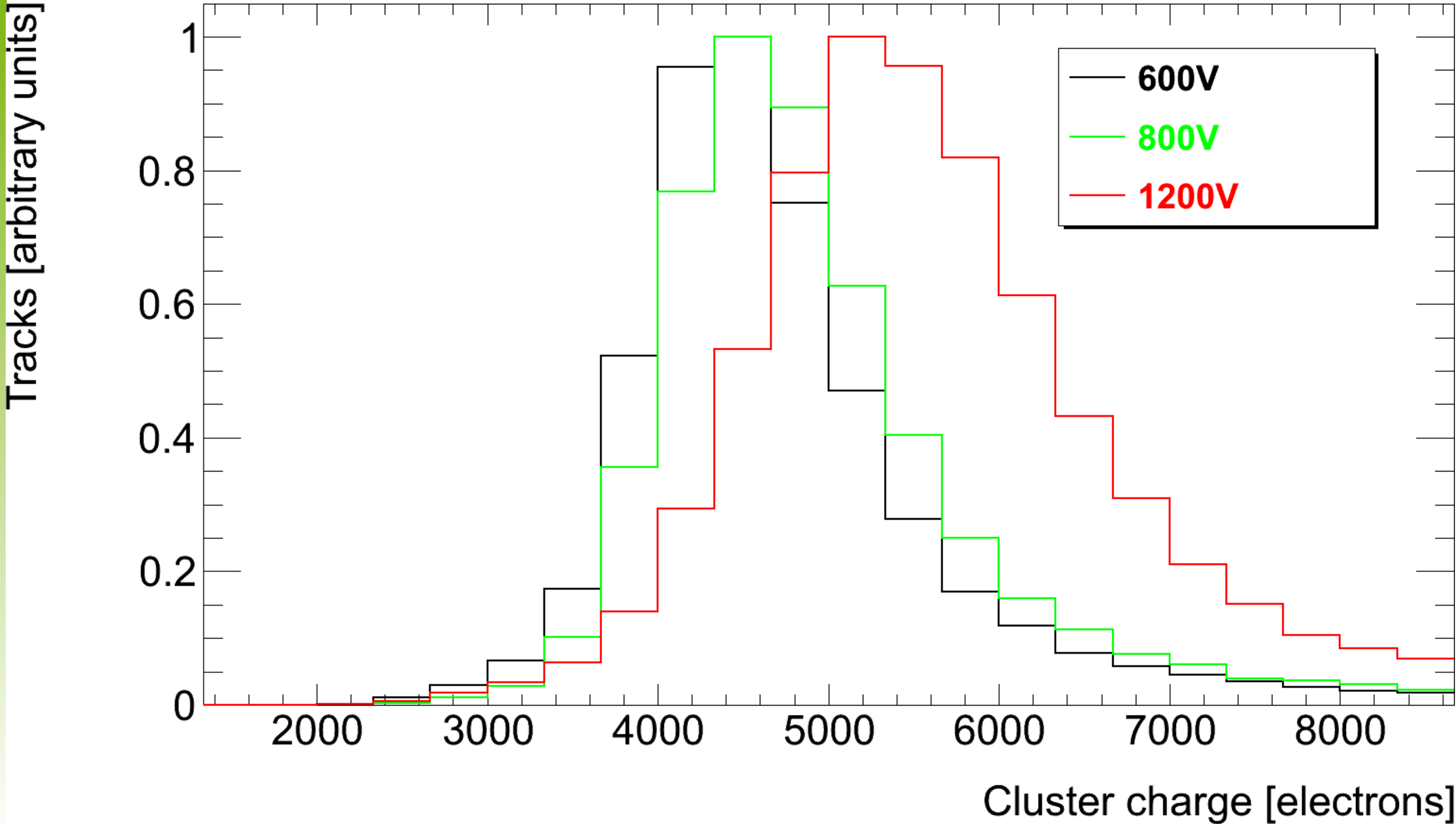
$5 \cdot 10^{15}$ n_{eq}/cm² with pions



$2 \cdot 10^{16}$ n_{eq}/cm² with Sr-90 electrons

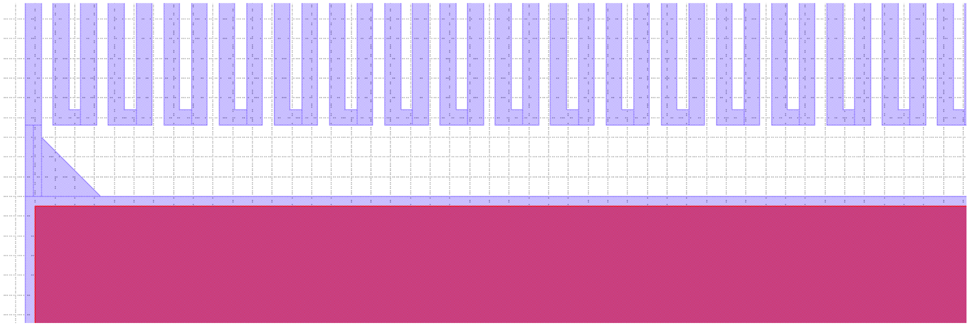


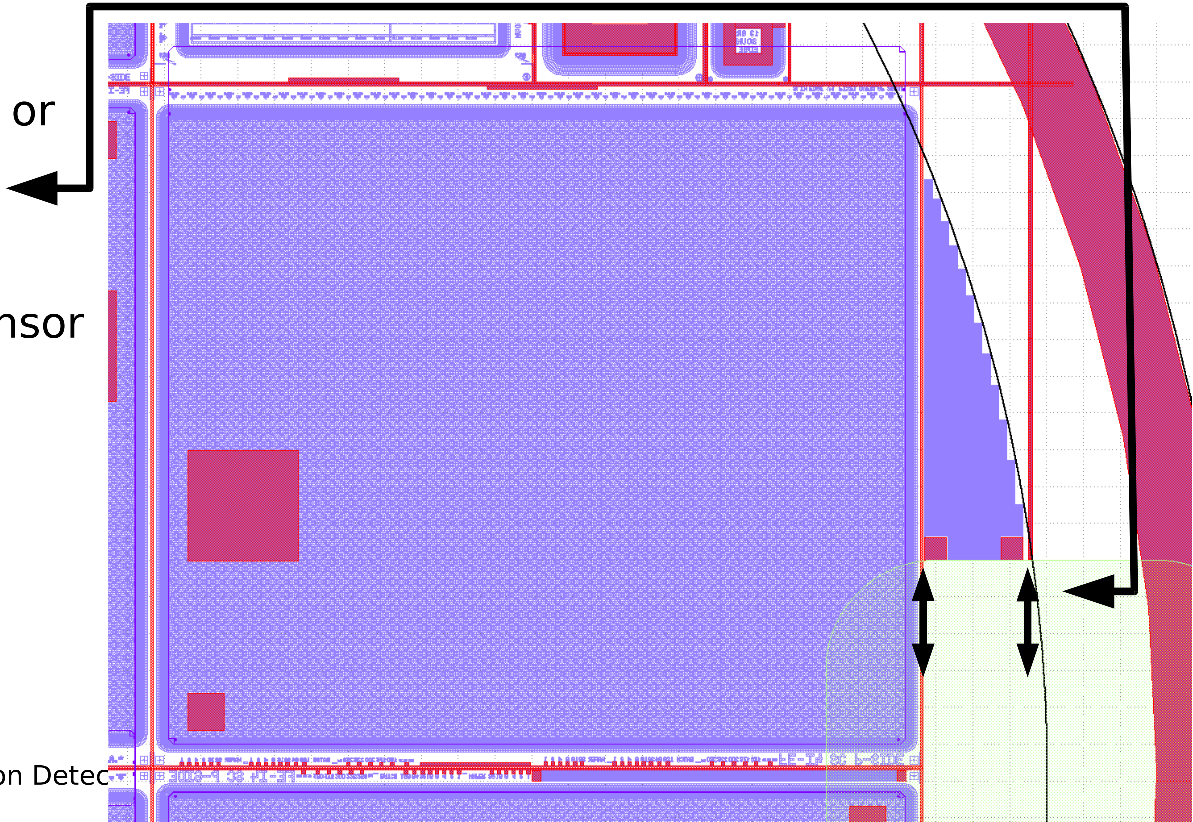
$2 \cdot 10^{16}$ n_{eq}/cm^2 with pions



Integrated temperature sensors

- next to all 4 FE-I4 SC sensors a loop of metal conductor is implemented on the p-side
- possibility to determine the sensor temperature via measurement of (temperature depending) resistance
- length of ~1.2m
    - resistance in the order of ~1-10k ohms
- two dicing streets to have the possibility of cutting away the loop or leave it attached to the sensor
- on three FE-I4 SCs and one MCM a shorter loop (~21cm length) is implemented in the edge of the sensor (within the dicing streets)





Status 150um wafers

- severe damages of the cutting edges
- large scratches into the safety margin on the p-side, probably caused by a defective dicing blade
- could be the reason for the low breakdown voltages
- n-side looks much smoother
- the following slim edge dicing steps will be supervised more closely