TCLink

Phase Determinism Study Meeting
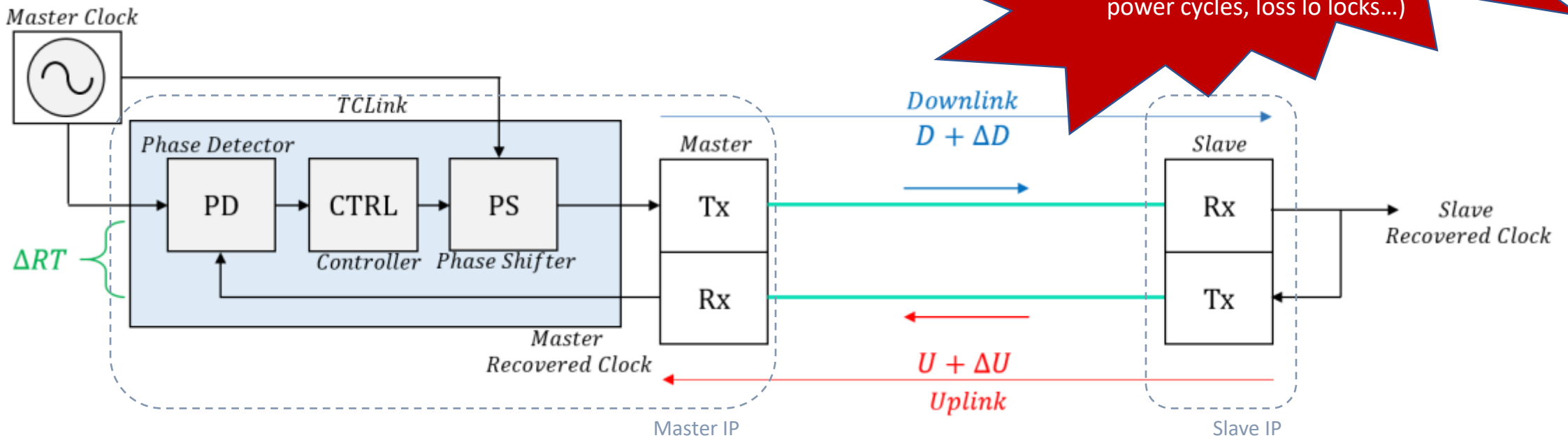
Introduction

S. Baron, E. Mendes

TCLink Principle in 1 slide

- IPs developped for Xilinx Ultrascale and Ultrascale+ Only
- Tested on GTH and GTY transceivers

Objective:
Extreme o(ps) phase stability between Master clock and Slave recovery clock over time (including during resets, power cycles, loss lo locks...)

The configuration of each transceiver has been carefully chosen to match TCLink requirements (see next slides)

TCLink

- Both Tx have exactly the same configuration

- FIFO enabled
  - FIFO half-full Flag used to adjust Phase Interpolator
- Tx PI controlled by the firmware to keep FIFO flag toggling
  - 1.5ps step

- QPLL used
- TxPLLRefClkDiv1
- Delay Aligner Bypassed

- TxOUTCLK used for user logic
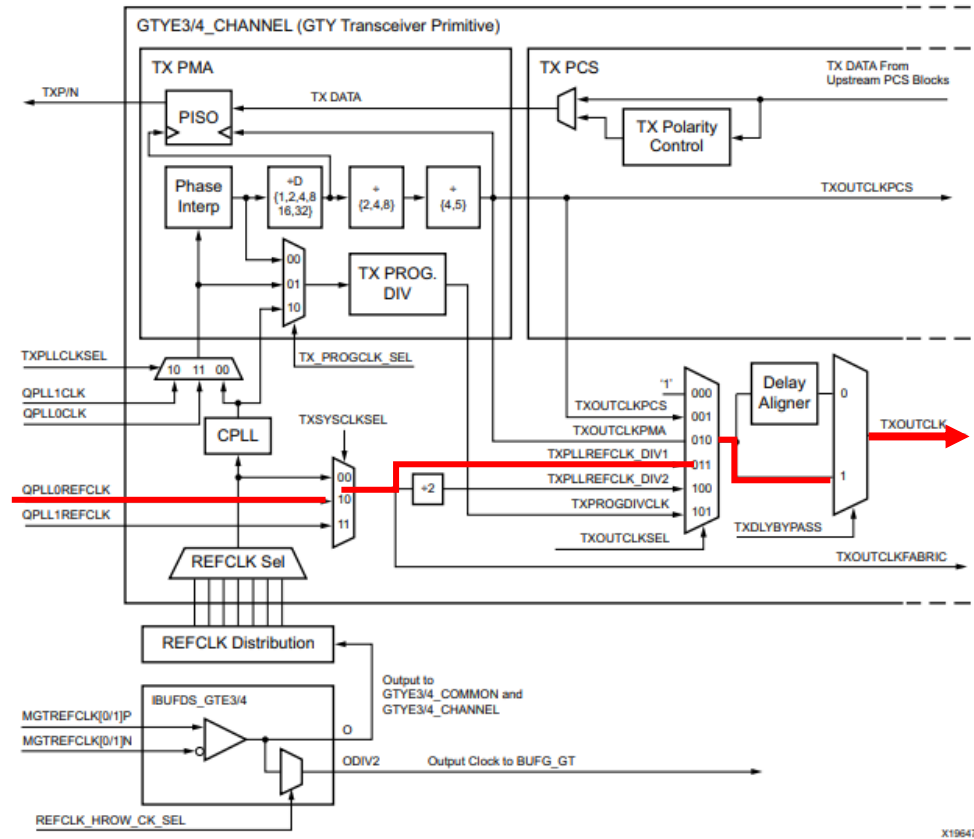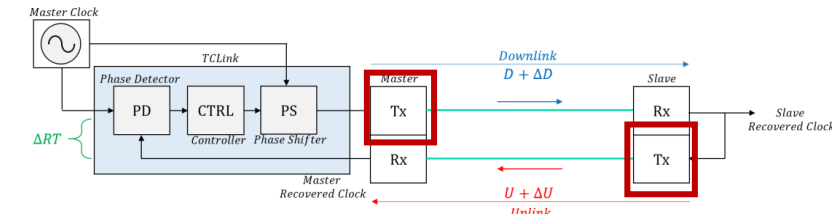
Figure 3-30: **TX Serial and Parallel Clock Divider**
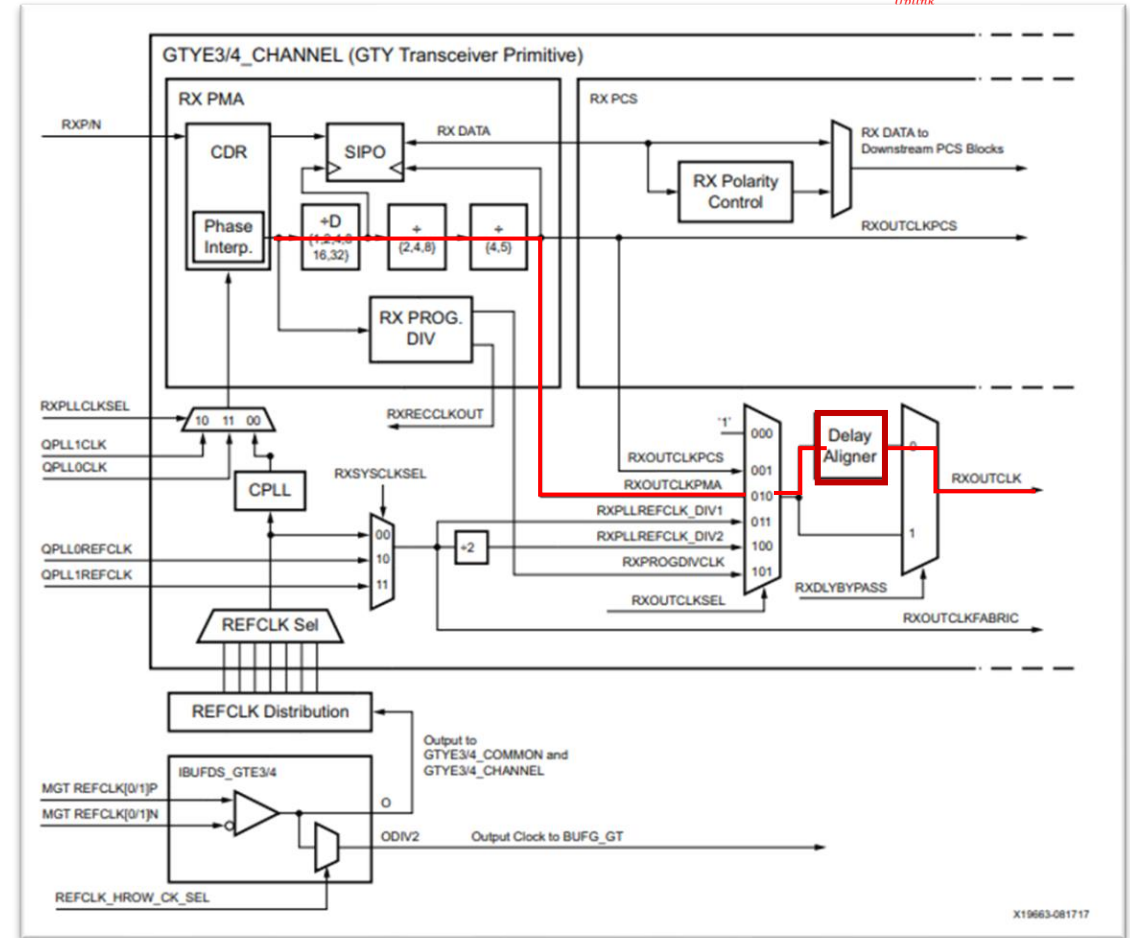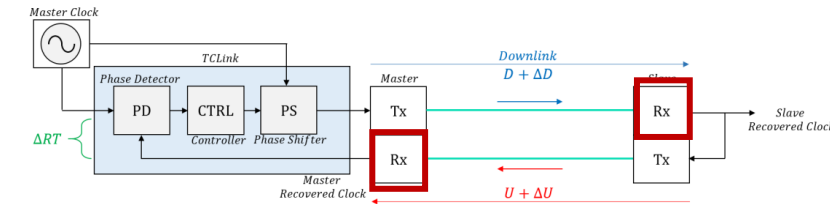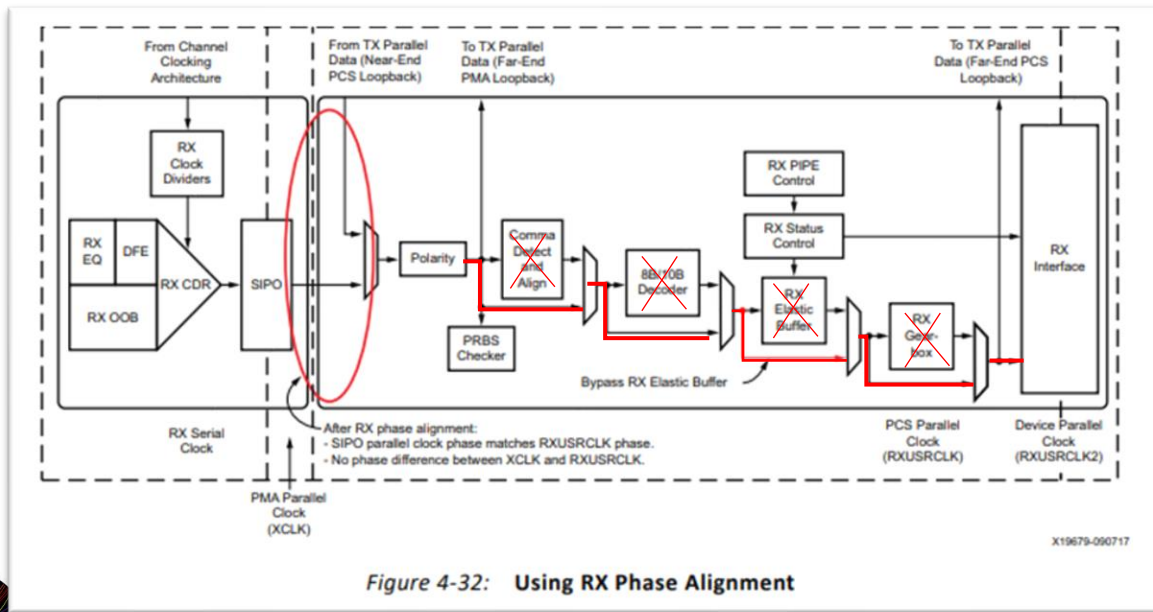
Common features…

- Both have:
  - **Buffer Bypass** (fixed latency for both directions)
    - Although not mandatory for upstream
  - **rxDelayAligner enabled**
    - mandatory by Xilinx in Buffer Bypass mode
  - **RxoutclkPMA** used

Figure 4-32: **Using RX Phase Alignment**
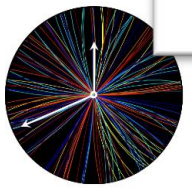
… the differences mostly reside in the **RxSlide Mode** for phase and data alignment

MASTER and SLAVE Rx

Differences…

MASTER

- rxSlide PCS mode
  - Xilinx recommended scheme
  - PCS mode only shifts the data

- Clock Alignment:
  - Rxusrclk is not recovered with fixed phase, but phase has to be known for DDMTD (in UI)
    - Use the rxslide pulses to account the phase difference (in UI) between txusrclk and rxusrclk at startup and adjust the control loop offset

SLAVE

- rxSlide PMA mode
  - Not recommended by Xilinx, forced by an XDC constraints
  - PMA mode shifts both the clock and the data
  - Extensively tested (also used in the PON, the GBT-FPGA…)

- Clock Alignment:
  - Clock and data are shifted to ensure frame alignment AND rxusrclk fixed-phase recovery
    - Clock shifted by 2UI every other rxslide pulse. A reset is implemented in the odd case.

- Two fall back solutions in case of problem with this implementation
  - Roulette approach (reset MGT until the header is aligned)
  - Buffer bypass in PCS mode (only data are shifted), count the rxslide pulses and compensate with external MMCM (not tested but close to the way the Master Rx is implemented)

TCLink