GBT Project Status

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November 2010
CERN

Outline

GBT Project Status:

- GBT project overview
  - Radiation hard link
  - The GBT chipset
- The GBTIA
- The GBLD
- The GBT - SCA
- The GBT Protocol on FPGAs
- The E – Links:
  - SLVS data transmission tests
  - Driver/Receiver
- The GBT – SerDes
  - The GBT – SerDes Architecture
  - Serializer
  - De-serializer
  - Phase-Shifter
  - Logic
  - Power consumption

- The GBTX
  - GBTX block diagram
  - GBT link bandwidth
  - GBTX-to-Frontend communication
  - 8B/10B Transmitter mode
  - GBTX packaging
  - GBTX power consumption
- GBT Project Schedule
- GLIB overview

Radiation Hard Optical Link Architecture

Defined in the "DG White Paper"
- "Work Package 3-1"
  - Objective:
    - Development of an high speed bidirectional radiation hard optical link
  - Deliverable:
    - Tested and qualified radiation hard optical link
 - Duration:
    - 4 years (2008 – 2011)

Radiation Hard Optical Link:
- Versatile link project:
  - Opto-electronics components
  - Radiation hardness
  - Functionality testing
- GBT project:
  - ASIC design
  - Verification
  - Radiation hardness
  - Functionality testing
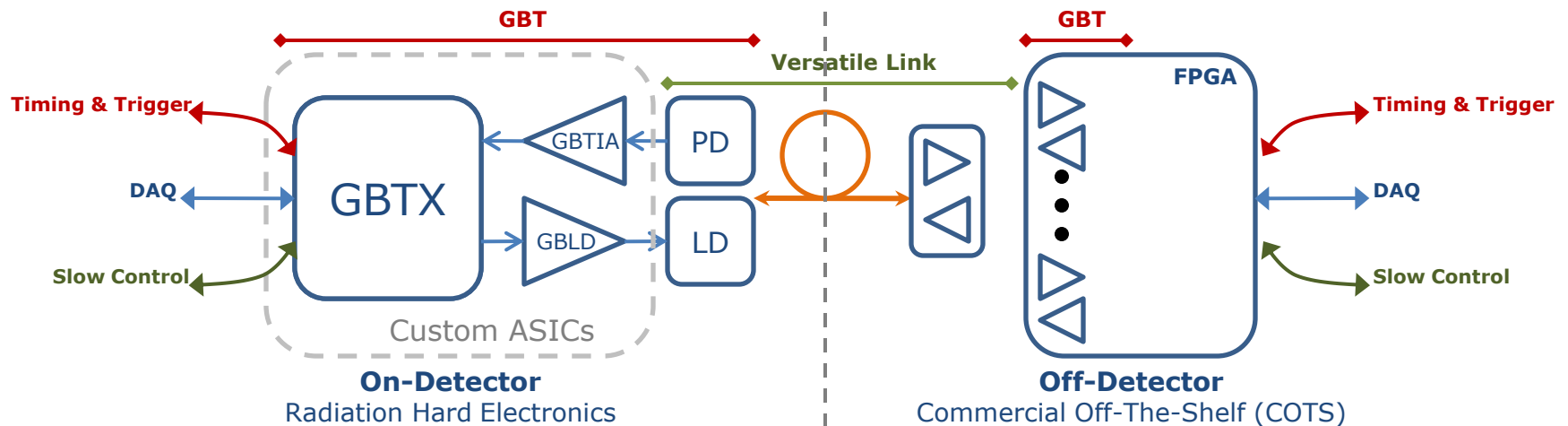
The GBT Chipset

- Radiation tolerant chipset:
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and Timing Transceiver
  - GBT-SCA: Slow control ASIC
- Supports:
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s

- The target applications are:
  - Data readout
  - TTC
  - Slow control and monitoring links.
- Radiation tolerance:
  - Total dose
  - Single Event Upsets
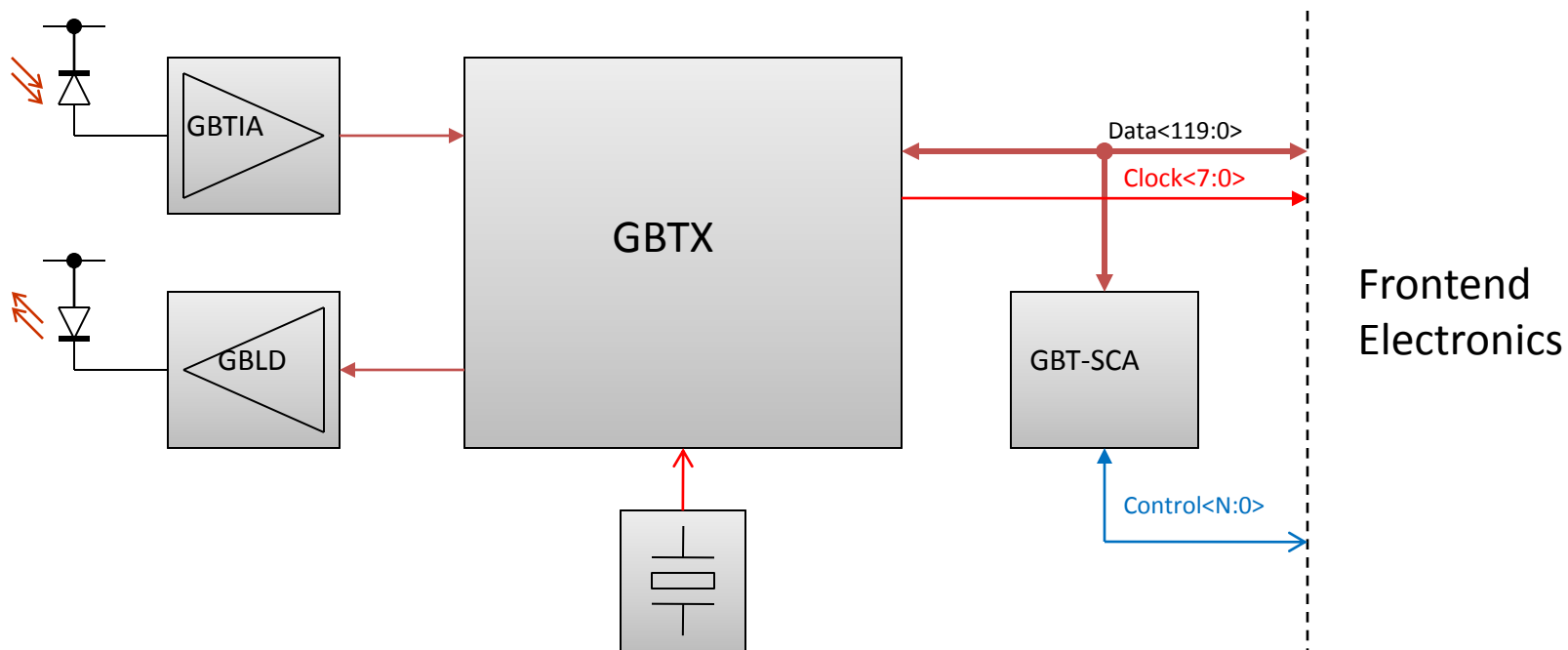
The GBTIA

Main specs:

- Bit rate 5 Gb/s (min)
- Sensitivity: 20 µA P-P (10^{-12} BER)
- Total jitter: < 40 ps P-P
- Input overload: 1.6 mA (max)
- Dark current: 0 to 1 mA
- Supply voltage: 2.5 V
- Power consumption: 250 mW
- Die size: 0.75 mm × 1.25 mm

Engineers :

- Ping Gui – SMU, USA
- Mohsine Menouni – CPPM, France

Status:

- Chip fabricated and tested
- Chip fully meets specifications!
- Radiation tolerance proven!
- GBTIA + PIN-diode encapsulated in a
  TO Package (Versatile link project)

Future:

- Version 2 will address productivity
- Pad positions reworked to facilitate the wire
  bond operation between the package and
  ASIC
- Mean optical power monitoring to facilitate
  pin-diode/fiber alignment
- 2.5 V supply
- Migration from the LM to the DM
  technologies flavor
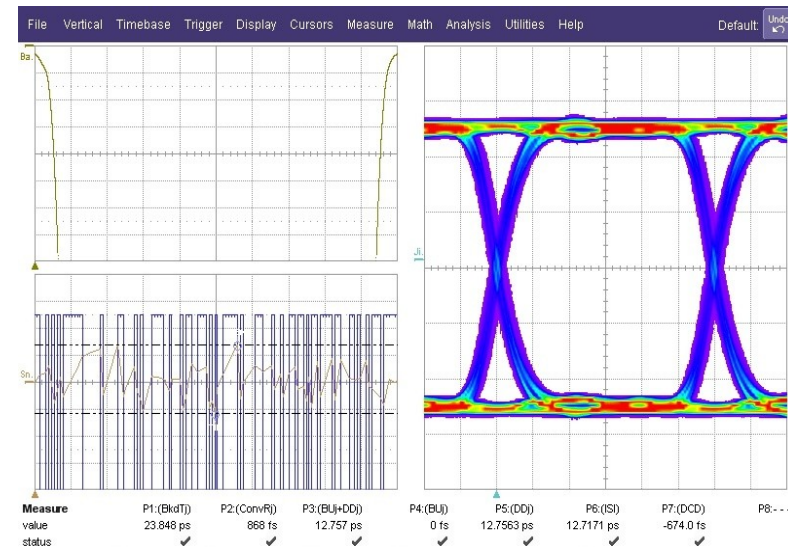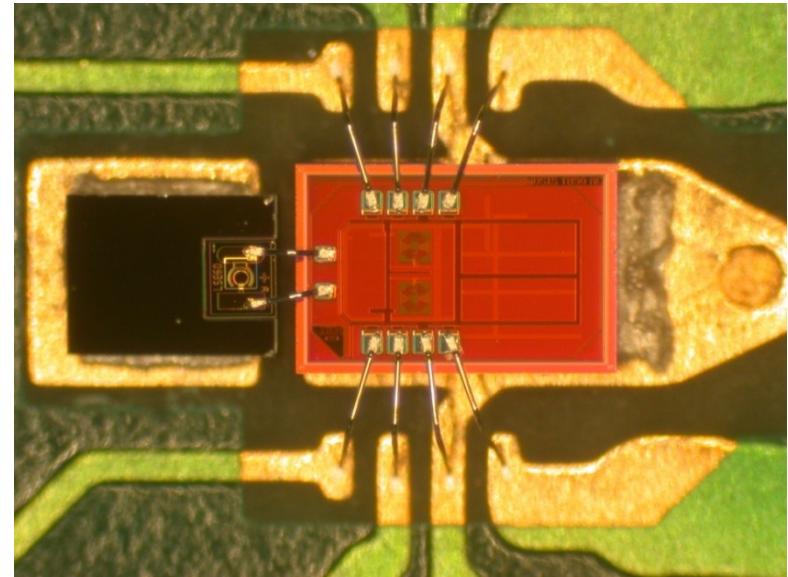
The GBLD

Main specs:

- Bit rate 5 Gb/s (min)
- Modulation:
  - current sink
  - Single-ended/differential
- Laser modulation current: 2 to 12 mA
- Laser bias: 2 to 43 mA
- "Equalization"
  - Pre-emphasis/de-emphasis
  - Independently programmable for rising/falling edges
- Supply voltage: 2.5 V
- Die size: 2 mm × 2 mm
- I2C programming interface

Engineers :

- Gianni Mazza – INFN, Italy
- Angelo Rivetti – INFN, Italy
- Ken Wyllie – CERN
- Ping Gui – SMU, USA

Status:

- Chip fabricated and tested
- Chip fully functional
- Performance according to specs (if corrected for the large input capacitance of the input protection diode)

Future:

- Reduce the area of the input protection diode

Pre-emphasis = 2.4mA
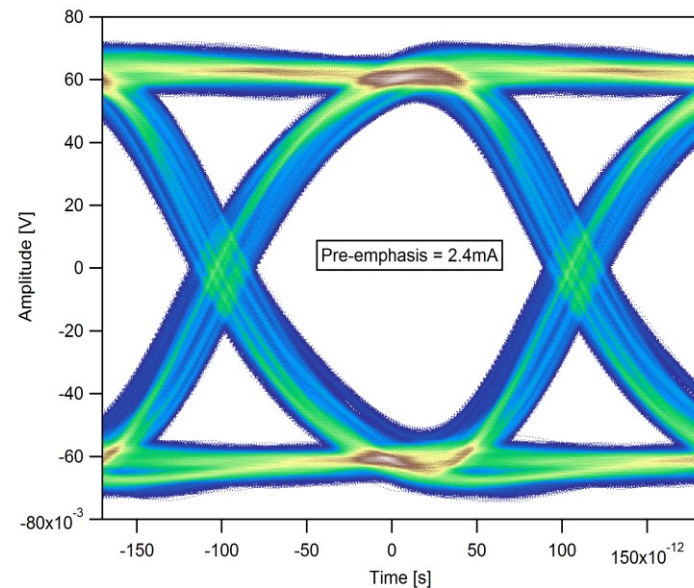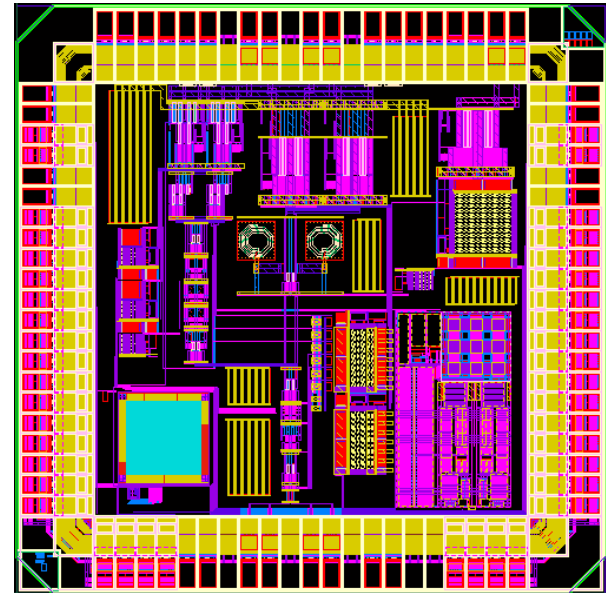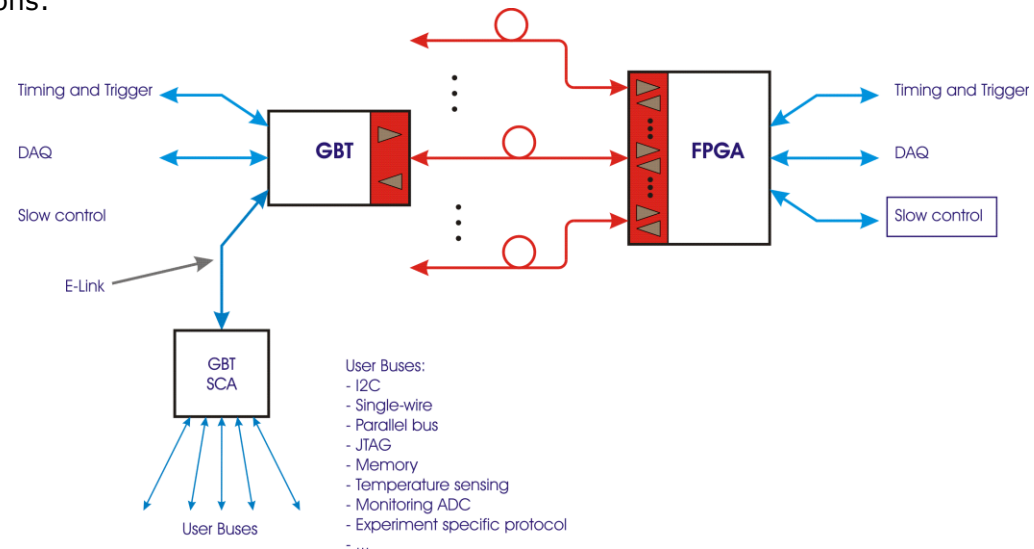
The GBT – SCA

GBT-SCA Main specs:

- Dedicated to slow control functions
- Interfaces with the GBTX using a dedicated E-link port
- Communicates with the control room using a protocol carried (transparently) by the GBT
- Implements multiple protocol busses and functions:
    - I2C, JTAG, Single-wire, parallel-port, etc…
- Implements environment monitoring functions:
    - Temperature sensing
    - Multi-channel ADC
    - Multi-channel DAC

Engineers:

- *Alessandro Gabrielli – INFN, Italy*
- *Kostas Kloukinas – CERN, Switzerland*
- Sandro Bonacini – CERN, Switzerland
- *Alessandro Marchioro – CERN, Switzerland*
- *Filipe Sousa – CERN, Switzerland*

<u>Status</u>

- Specification work undergoing:
- 1st Draft already available
- RTL design undergoing
- Tape-out: 2011
- 10-bit ADC prototype submitted for fabrication in April 2010

The GBT Protocol on FPGAs

- GBT-SERDES successfully implemented in FPGAs:
  - Scrambler/ Descrambler + Encoder/ Decoder + Serializer/CDR
- FPGA Tested:
  - XILINX Virtex-5FXT and 6LXT
  - ALTERA Stratix II and IV GX
- Optimization studies:
  - Optimization of use of resources (2009)
  - Low and "deterministic" latency (2010)
- Firmware:
  - "Starter Kit" is available for download with various resources optimization schemes for
    - StratixIIGx and Virtex5FXT
  - Available soon for:
    - StratixIVGx and Virtex6LXT
    - Low latency
- Engineers:
  - Sophie Baron – CERN, Switzerland
  - Jean-Pierre Cachemiche – CPPM, France
  - Csaba Soos – CERN, Switzerland
  - Steffen Muschter - Stockholm University
- Users:
  - 30 registered users from all over the world (most users from collaborating institutes)
  - LHC experiments, but also CLIC, PANDA, GBT
  - Very active users are now part of the development team

Xilinx - 4.8 Gb/s
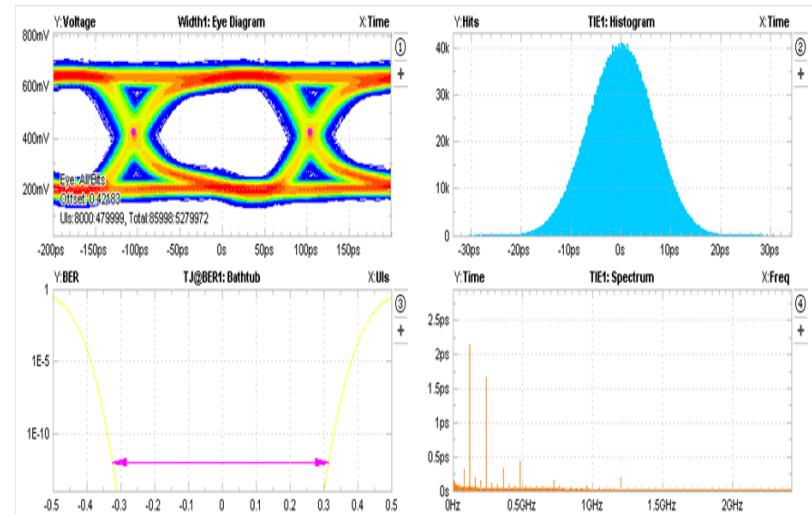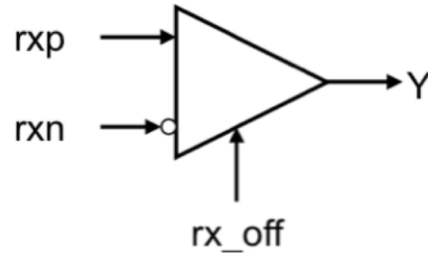

Altera + opto TRx - 4.8 Gb/s
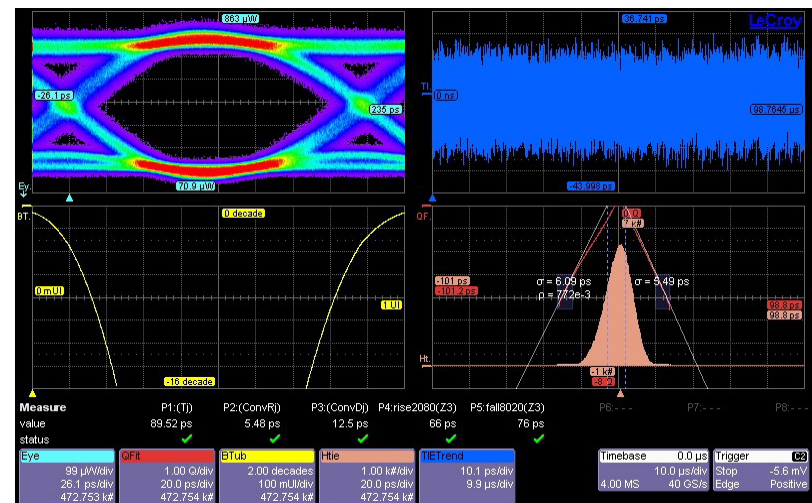
SLVS Driver/Receiver

- Receiver
  - *Power Supply: 1.2V to 1.5V*
  - *Power Dissipation:*
    - *150uW @ 320Mbs, 1.2V supply*
   - *<1uW @ power down*

rxp →
rxn →
→ Y
rx_off ↑

- Driver
  - *Power Supply: 1.2V to 1.5 V*
  - *Power Dissipation:*
    - *3.1mW @ 320Mbs, 1.2 V supply*
    - *<10uW @ power down*

tx_csel[3:0]
A →
→ txp
→ txn

- Engineer
  - Sandro Bonacini – CERN, Switzerland

Status:
  - Chip currently under testing

Electrical Specifications

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_{IDH}	Differential input high threshold			3.8	5.9	mV
V_{IDL}	Differential input low threshold		0	2.2		mV
V_{CM}	Common-mode voltage range		-300		V_{DD}+300	mV
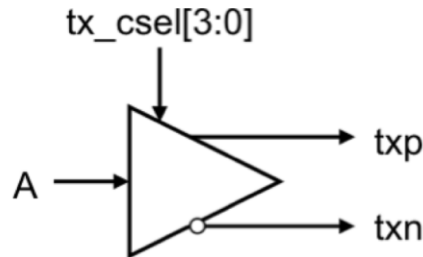
Electrical Specifications

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_{OD}	Differential output voltage		110	200	320	mV
ΔV_{OD}	Differential output voltage change	(fig.1)	0	14	20	mV
V_{OS}	Driver offset voltage		100	200	350	mV
I_{SCO}	Output short-circuit current	V_{OS}=0, V_{OD}=0		-25	-60	mA
I_{SCOD}	Differential output short-circuit current	V_{OD}=0		-3	-5	mA
I_{DD}	Supply current			2.5	4.0	mA

Programmable Output Current

csel[3:0]	Output current [mA]	Driver power dissipation [mW]
8	2.0	3.0
4	1.3	2.1
2	0.8	1.4
1	0.5	1.0
(sleep) 0	0	<.01

Note: All values are given at 1.2V power supply voltage, typical conditions.

E – Links: SLVS Data Transmission Tests

- **Scalable Low Voltage Standard (SLVS)**
  - JEDEC standard: JESD8-13
  - Main features:
    - 2 mA Differential max
    - Line impedance: 100 Ohm
    - Signal: +- 200 mV
    - Common mode ref voltage: 0.2V
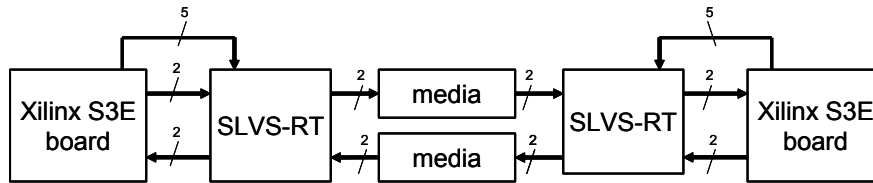
- Tests on SLVS-RT chip
  - 1 driver
  - 1 receiver
- **Various types of transmission media tested:**
  - Kapton
  - PCB
  - Ethernet cable
- **Test equipment**
  - Bidirectional link
 - FPGAs perform pseudo-random data generation and checking

at 320Mbps	140 mV min swing	200 mV half swing	400 mV nominal
20cm kapton	< 1.00E-13	< 1.00E-13	< 1.00E-13
3cm UTP	< 1.00E-13		< 1.00E-13
1m PCB microstrip	< 1.00E-13	< 1.00E-13	< 1.00E-13
2m PCB microstrip	3.20E-12	9.00E-13	8.00E-13
2m PCB stripline	1.05E-08	1.00E-12	8.00E-13
5m ethernet	* 2.37E-12	* 1.60E-12	

(*) PRELIMINARY

X-ray Irradiation Results

Pre-rad

Input

Output

Post-rad

Pre-rad cycle-to-cycle jitter measured using a PRBS sequence generator (Agilent 81133A) is about 17 ps (rms)

SLVS receiver supply current
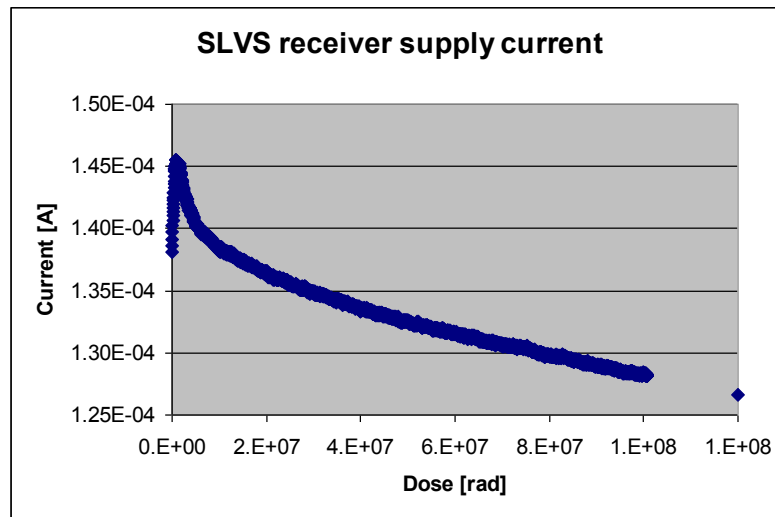
- All chips show a peak in the SLVS receiver supply current and then a decrease to a value smaller than the pre-rad.
- SLVS transmitter supply current doesn't change significantly with irradiation.
- Chips show a worse jitter performance after irradiation
    - Sequence-dependence, most likely due to the receiver becoming slower for the decrease in supply current
    - PMOS threshold increase responsible for bias current degradation.
- New chip submitted July 2010 with a resized bias circuit

Input from Xilinx S3E
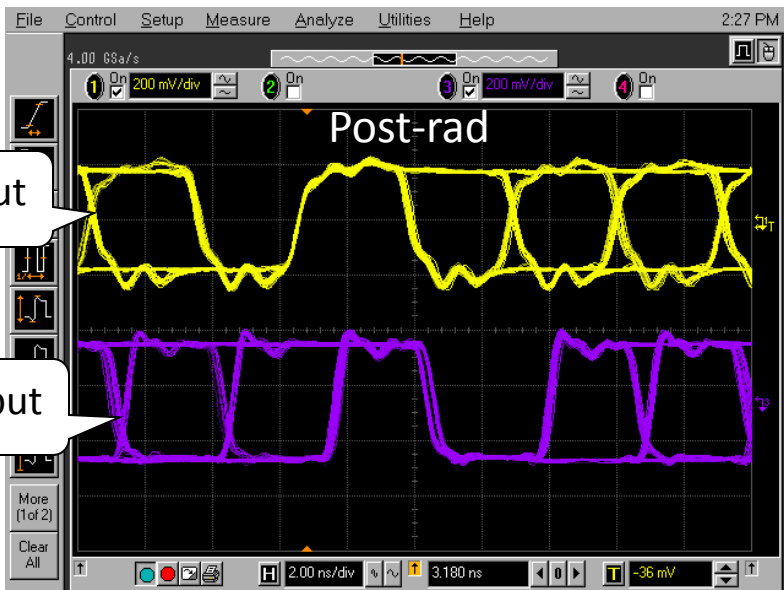
The GBT - SerDes

**The GBT – SerDes is a demonstrator for:**

- The Serializer/De-serializer critical circuits:
  - Phase-Locked Loops
  - Frequency dividres
  - Line driver/receiver
  - Constant-latency barrel shifter
  - Phase shifter
- The circuit operates at 4.8 Gb/s
- The chip was packaged in a custom flip-chip BGA package

Engineers:

- Ozgur Cobanoglu - CERN, Switzerland
- Federico Faccio - CERN, Switzerland
- Rui Francisco – CERN, Switzerland
- Ping Gui – SMU, USA
- Alessandro Marchioro - CERN, Switzerland
- Paulo Moreira - CERN, Switzerland
- Christian Paillard - CERN, Switzerland
- Ken Wyllie - CERN, Switzerland

Status:

- Chip is currently under testing
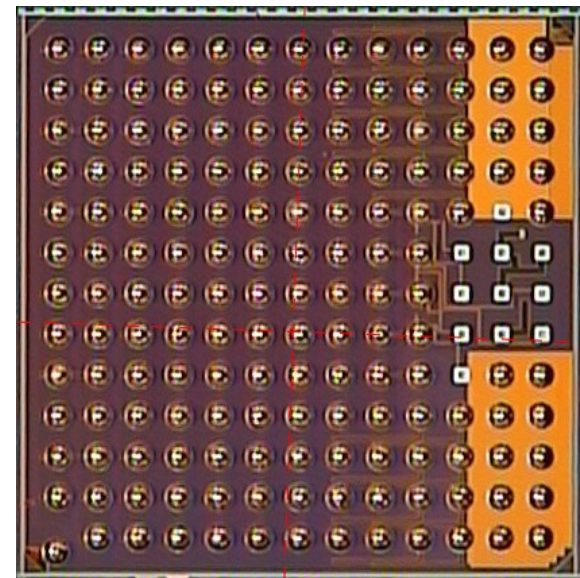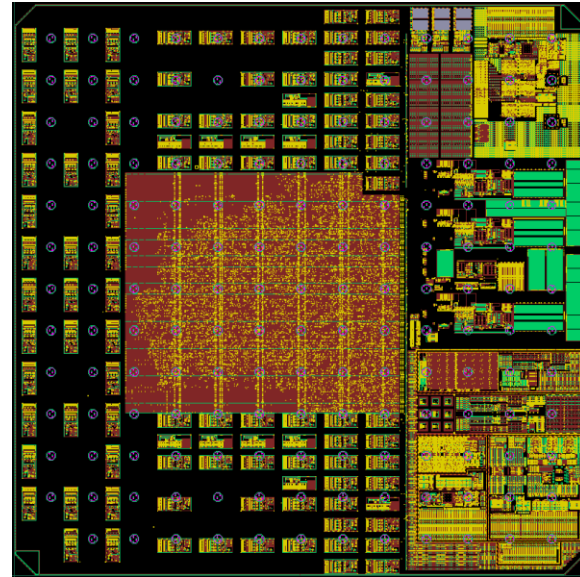
The GBT – SerDes Architecture
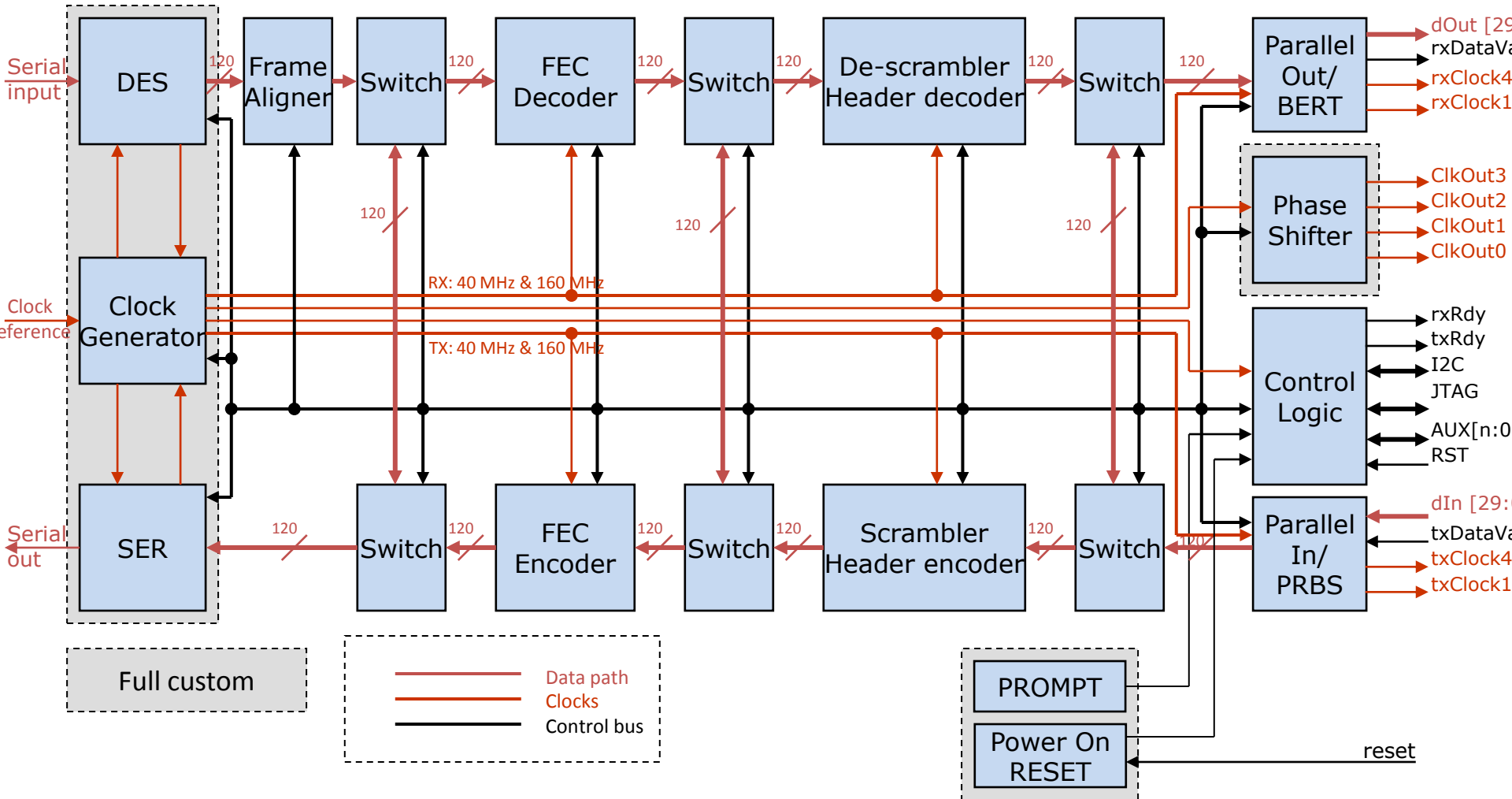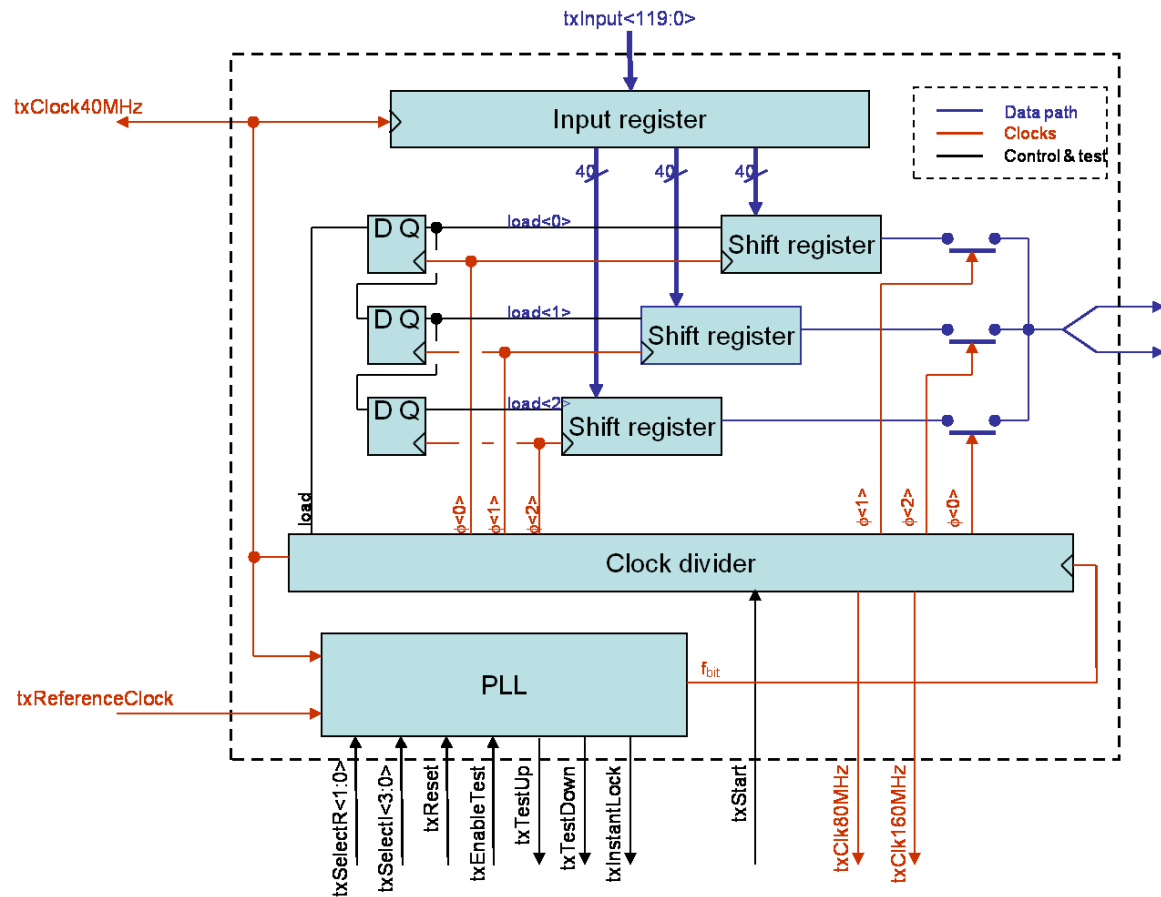
Serializer

Serializer:

- 4.8 Gb/s
- 120-bit shift register
  - 3 × 40-bit shift register (f=1.6 GHz)
  - 3-to-1 fast multiplexer (f=4.8 GHz)
- Data path:
  - No SEU protection
  - SEUs handled by the Reed-Solo... CODEC
- Clock divider:
  - Divide by 120
  - f = 4.8 GHz
  - Triple voted for SEU robustness
- PLL:
  - SEU hardened VCO

Engineers:

- Ozgur Cobanoglu - CERN, Swit...
- Federico Faccio - CERN, Switzer...
- Paulo Moreira - CERN, Switzerla...
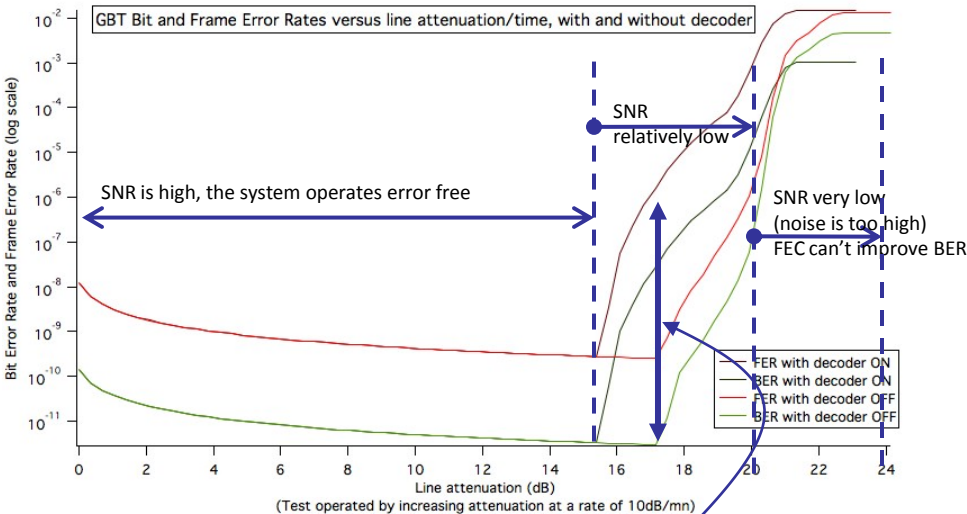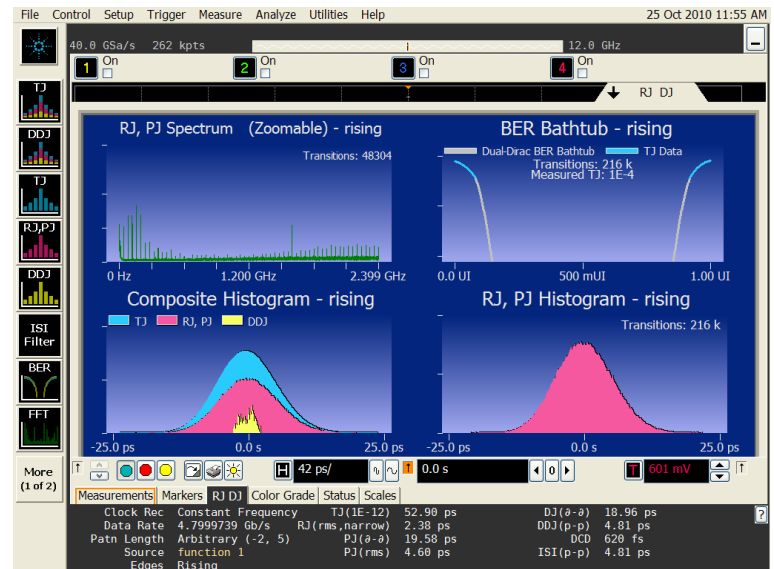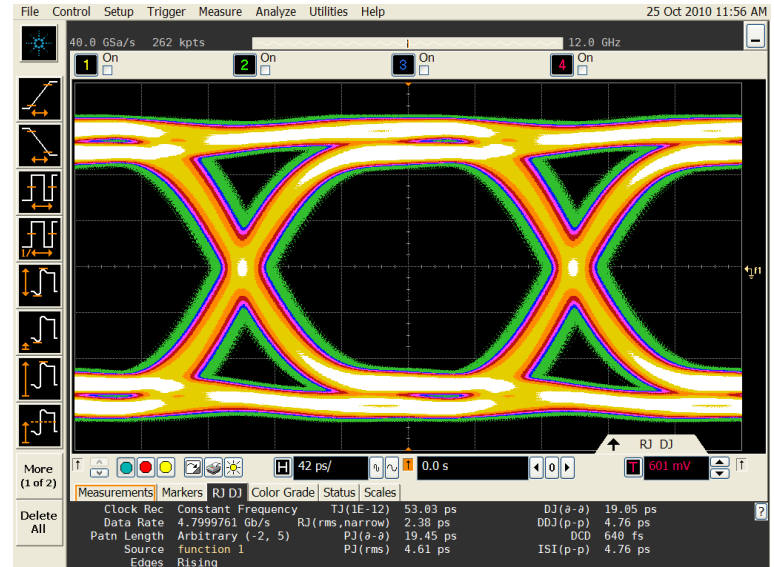
Status:

- Fully functional
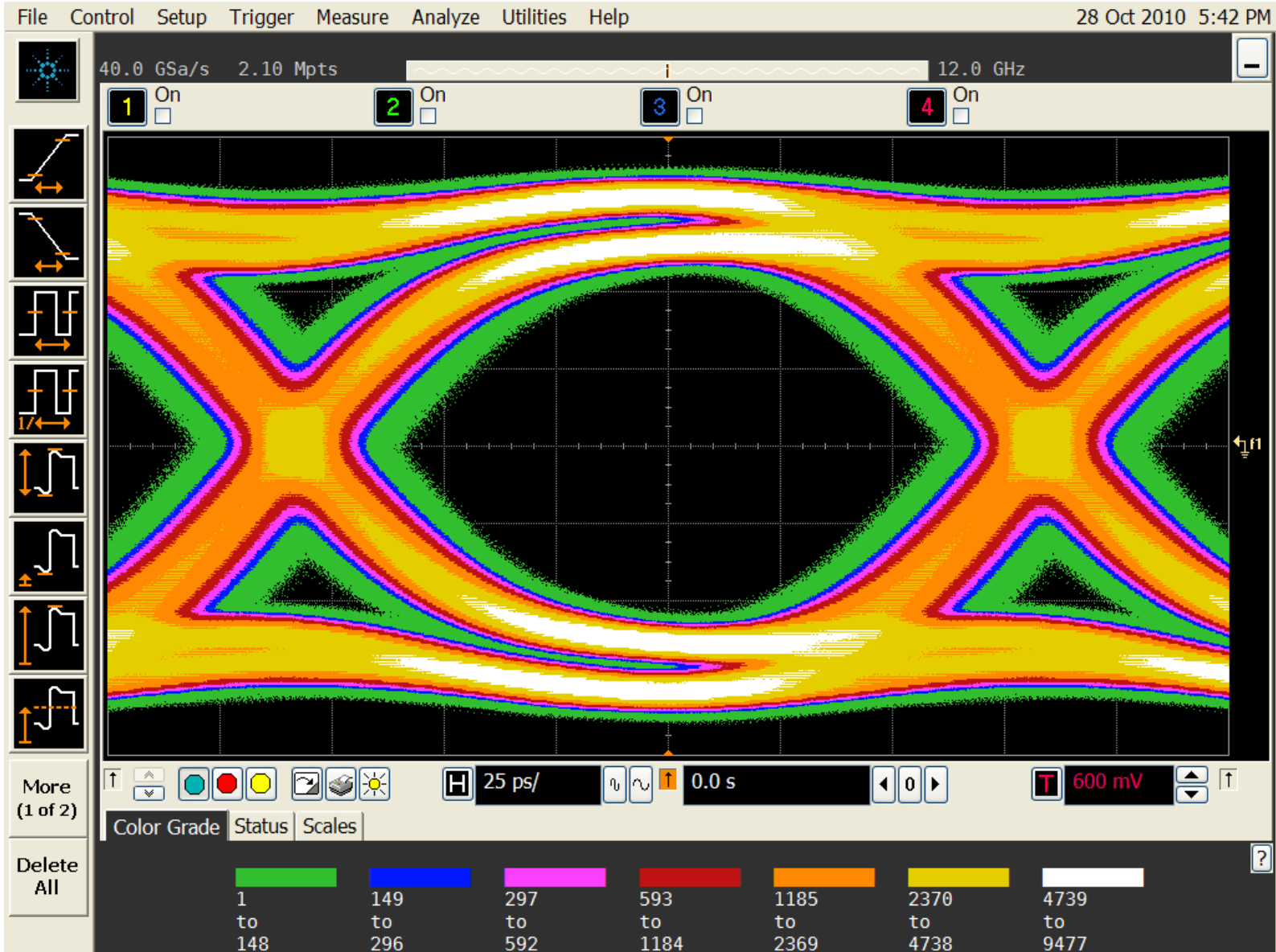
Serializer Measurements: 4.8 Gb/s

- **Tx Jitter:**
  - Total jitter $(1e^{-12})$: 53 ps
  - Random jitter: 2.4 ps (rms)
  - Deterministic jitter: 19 ps
    - Data dependent: 4.8 ps
    - Periodic:
      - RMS: 4.6 ps
      - PP: 19.6 ps
    - Duty-cycle-distortion: 0.6 ps
    - Inter-symbol interference: 4.8 ps

GBT Bit and Frame Error Rates versus line attenuation/time, with and without decoder

SNR relatively low

SNR is high, the system operates error free

SNR very low (noise is too high) FEC can't improve BER

FER with decoder ON
BER with decoder ON
FER with decoder OFF
BER with decoder OFF

Bit Error Rate and Frame Error Rate (log scale)

Line attenuation (dB)
(Test operated by increasing attenuation at a rate of 10dB/mn)

More than 3 orders of magnitude improvement due to the FEC

Serializer Measurements: 6 Gb/s
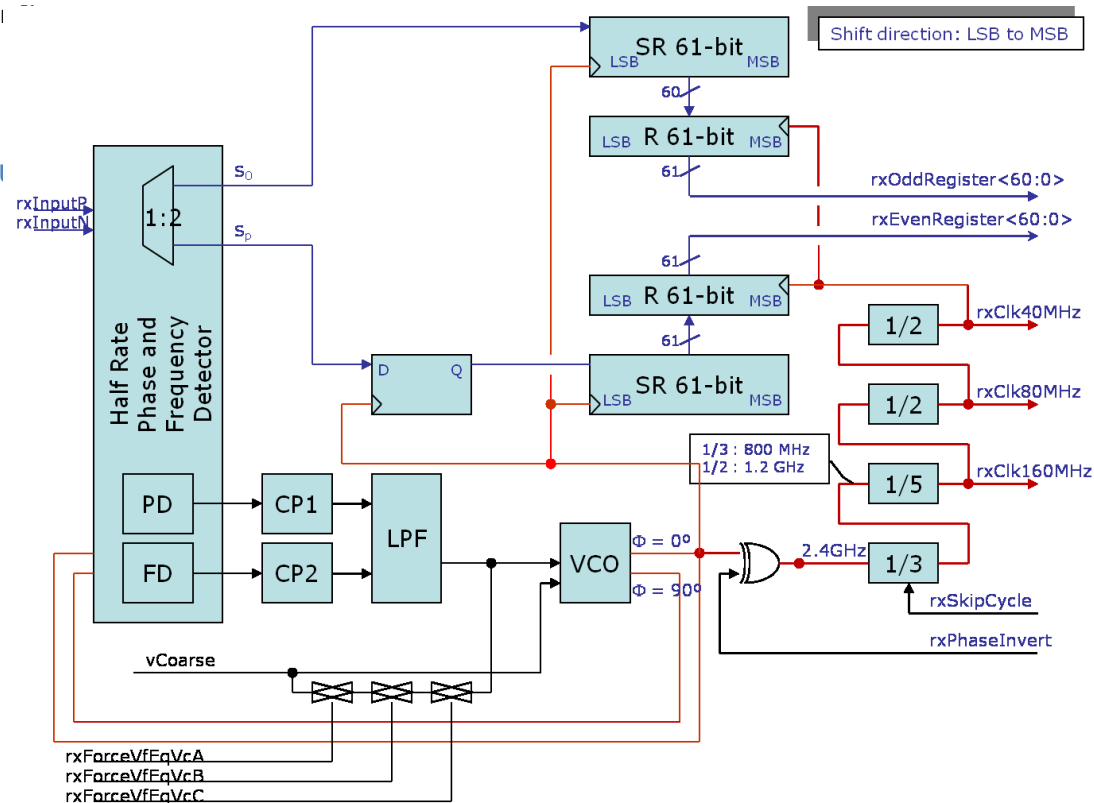
De-serializer

De-Serializer:

- Dual PLL CDR Loop:
  - 1st Loop: Frequency centering PLL
  - 2nd Loop: CDR
  - Allows to reduce the CDR VCO gain for lower
- Half-Rate:
  - Phase-detector
  - Frequency-detector
- Constant latency frame alignment circu
- As for the serializer:
  - Unprotected data path
  - TMR clock divider
  - SEU hardened VCO

Engineers:

- Ozgur Cobanoglu - CERN, Switzerland
- Federico Faccio - CERN, Switzerland
- Rui Francisco – CERN, Switzerland
- Paulo Moreira - CERN, Switzerland

Status:

- The receiver is fully functional
- Clock recovery operates up to 6 Gb/s
- However it only operates error free up 3.0 Gb/s
  - This seems to be caused by the (so far unexplained) bad quality of the eye-diagram at the input of the receiver (see later in this presentation)
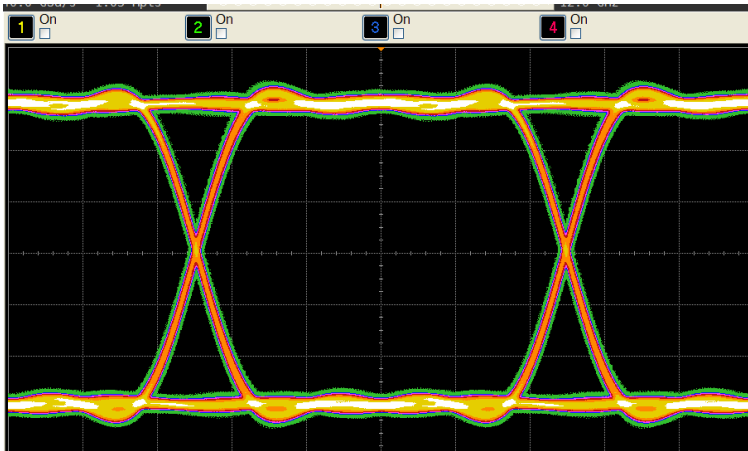
CDR: Measurements

- *40 MHz recovered clock clock PRBS @ 4.8 Gb/s:*
  - Total jitter (1e^{-12}): 63 ps
  - Random jitter: 4.9 ps (rms)
  - Deterministic jitter: 24 ps (pp)
    - Periodic:
      - RMS: 2 ps
      - PP: 5 ps
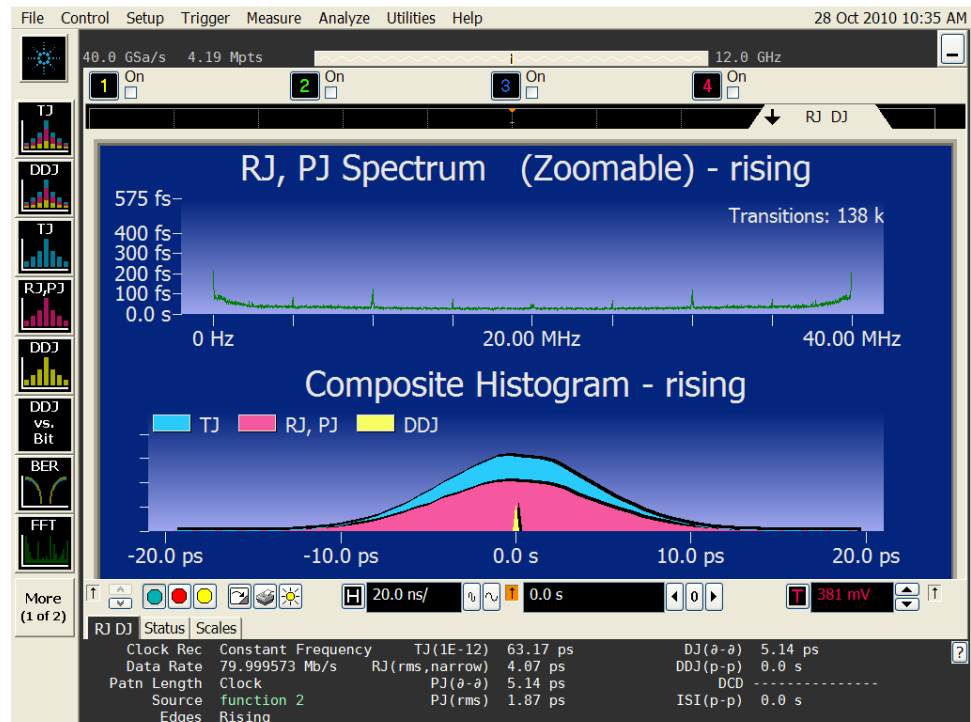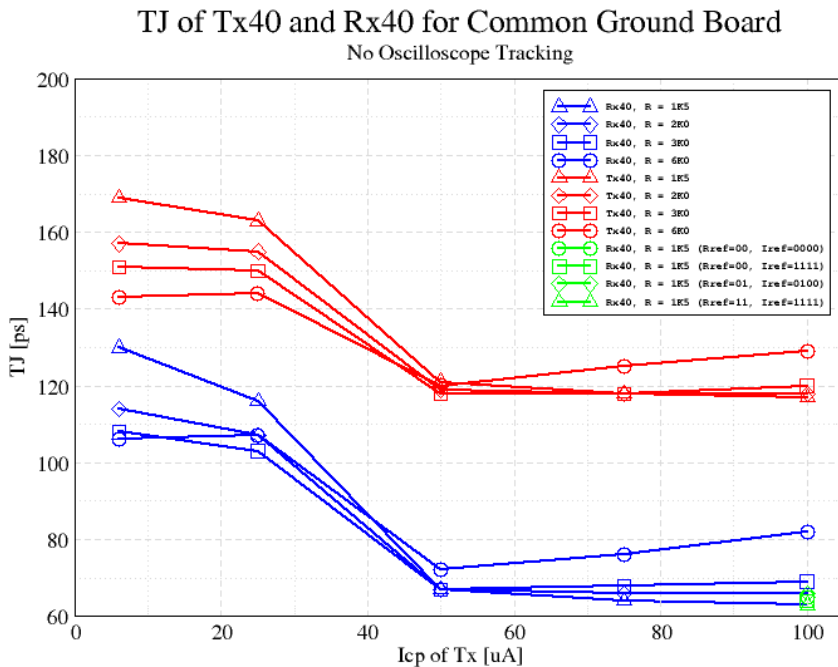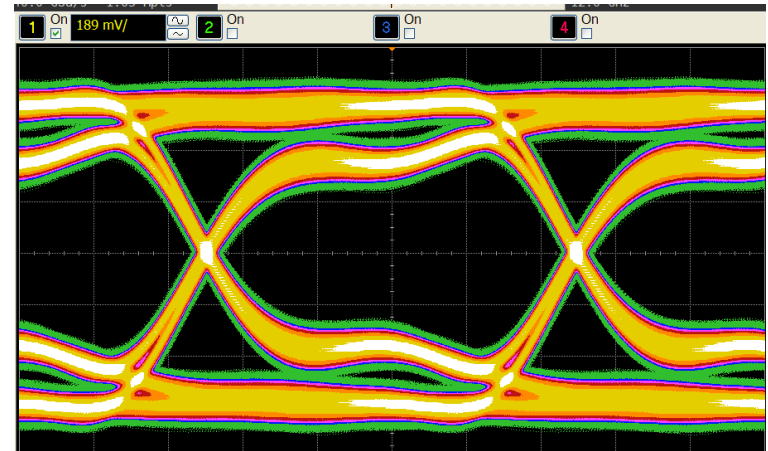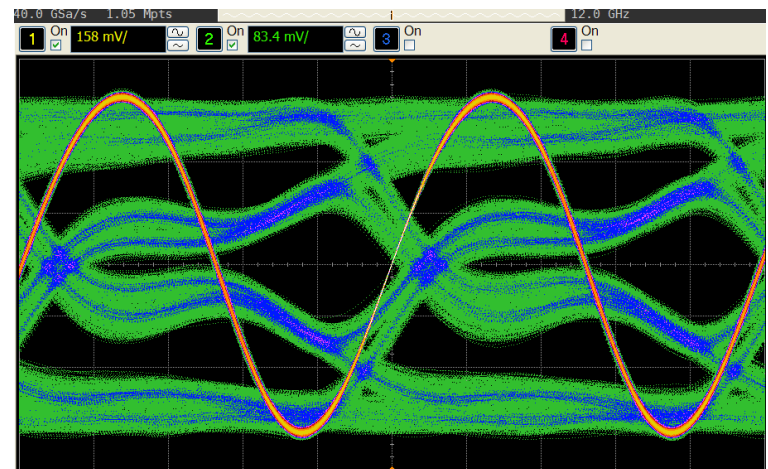
De-serializer: Input eye-diagram

Signal generator eye-diagram (straight to the scope)

Empty board with a connector and a 100 Ω termination (differential active probe)

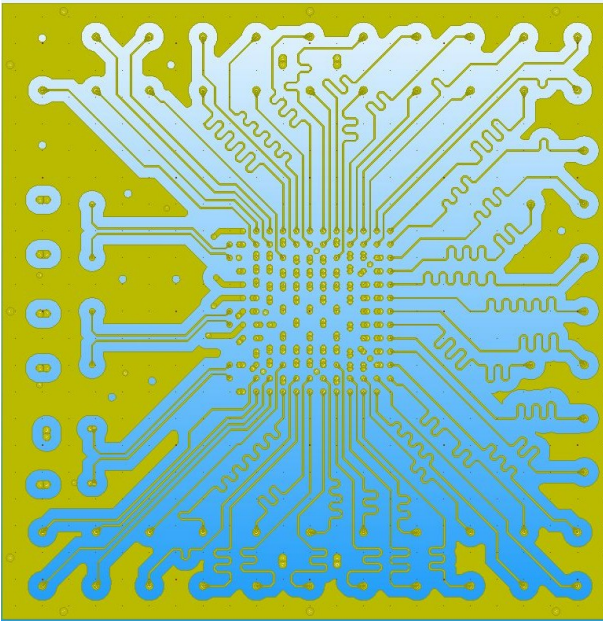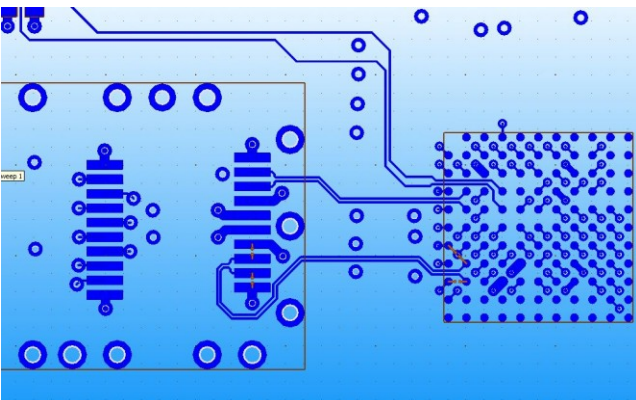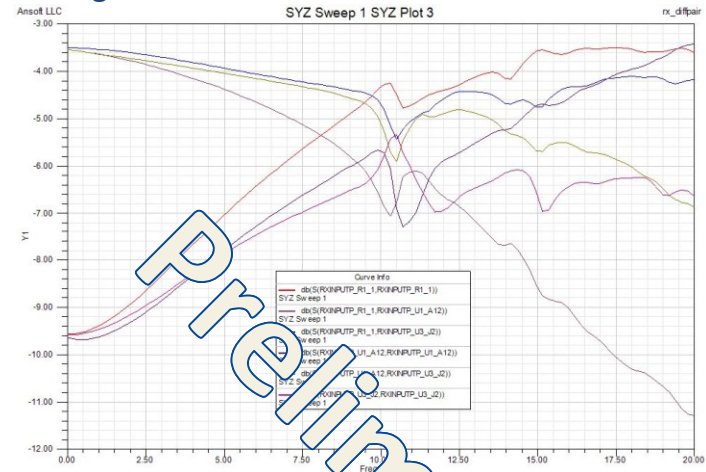Populated board

PCB − Package Modelling (2½ D)

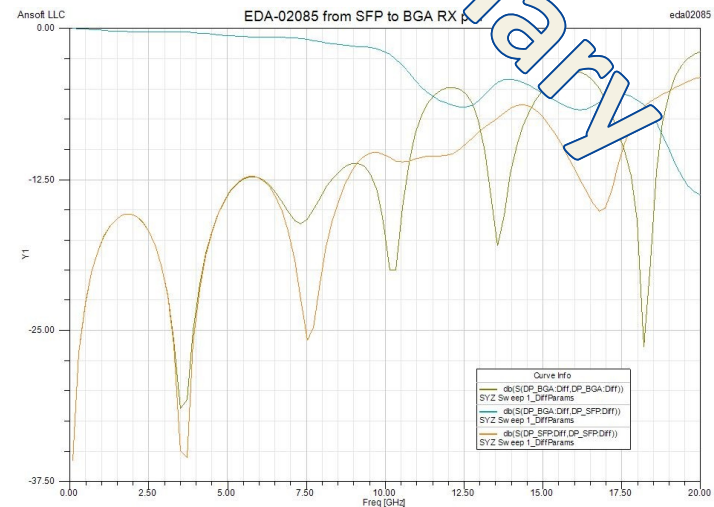**Package (one interconnect layer)**

PCB: SFP to GBT transmission lines

Package S-Parameters

Package + PCB S-Parameters

Phase – Shifter

Phase-Shifter:

- Main features:
- 8 – channels (3 in the GBT-SERDES prototype)
- 1 PLL + Counter generates the three frequencies: 40 / 80 and 160 MHz
- 1 DLL per channel
- Mixed digital/analogue phase shifting technique:
- Coarse de-skewing – Digital
- Fine de-skewing – Analogue
- Power consumption:
  - PLL: 42 mW (measured)
  - Channel: 16 mW/channel (measured)
- Differential non-linearity: <6.7% LSB
- Integral non-linearity: INL<6.5% LSB

Engineers :

- Ping Gui – SMU, USA
- Tim Fedorov – SMU, USA
- Paul Hartin – SMU, USA
- Nataly Pico – SMU, USA
- Bryan Yu – SMU, USA

Status:

- Fully functional
- Fully meets the specs
  - One channel with timing clearly identified with tri

#	specification	min	typ	max	unit	note
	Number of outputs	8				
	Frequencies	40, 80 and 160			MHz	individually programmable per output, set by control word Freq[1:0]
	Phase resolution	50			ps	Set by Delay[8:0]
	DNL			20%	LSB (50ps)	
	INL			30%	LSB (50ps)	
	Jitter RMS			5	ps	
	Jitter P-P			30	ps	
	Temperature coefficient			5	ps/deg	
	Supply coefficient			50	ps/V	
	Logic levels					Programmable: CMOS/LVDS
	Synchronized with the 40Mhz main clock					

Phase – Shifter: Measurements

- **Resolution:** Δt = 48.83 ps
- **Differential Non-Linearity**:
  - σ = 4.7 ps (9.6% of Δt)
  - pp = 21.5 ps (44% of Δt)

- **Period Jitter:** σ = 4.8 ps (pp = 29 ps)
- **Integral Non-Linearity**:
  - σ = 4.3 ps (8.7% of Δt)
  - pp = 21.9 ps (48.7% of Δt)
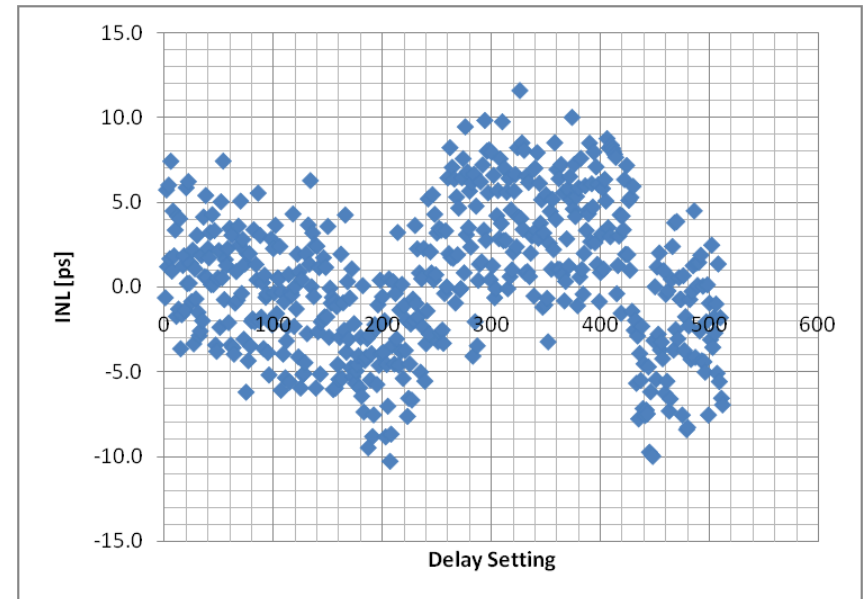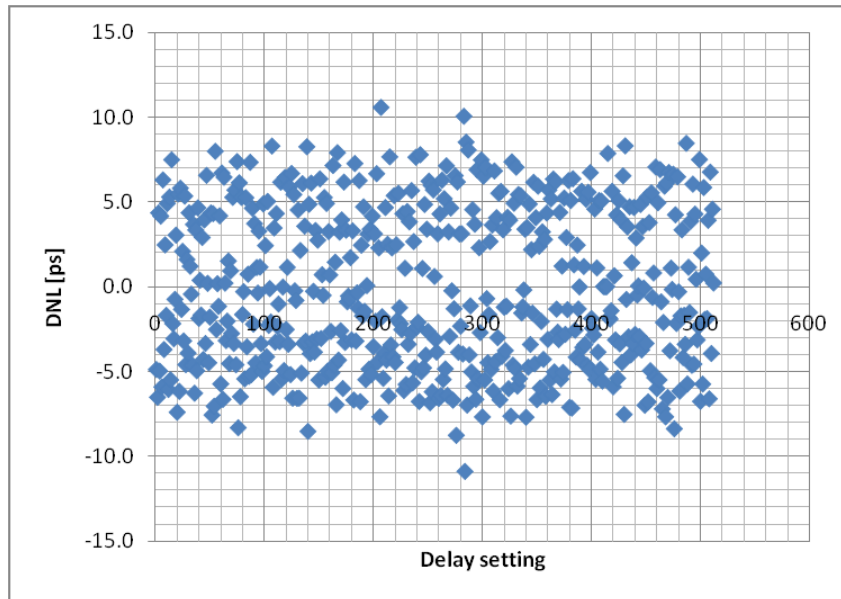
Phase – Shifter: Measurements
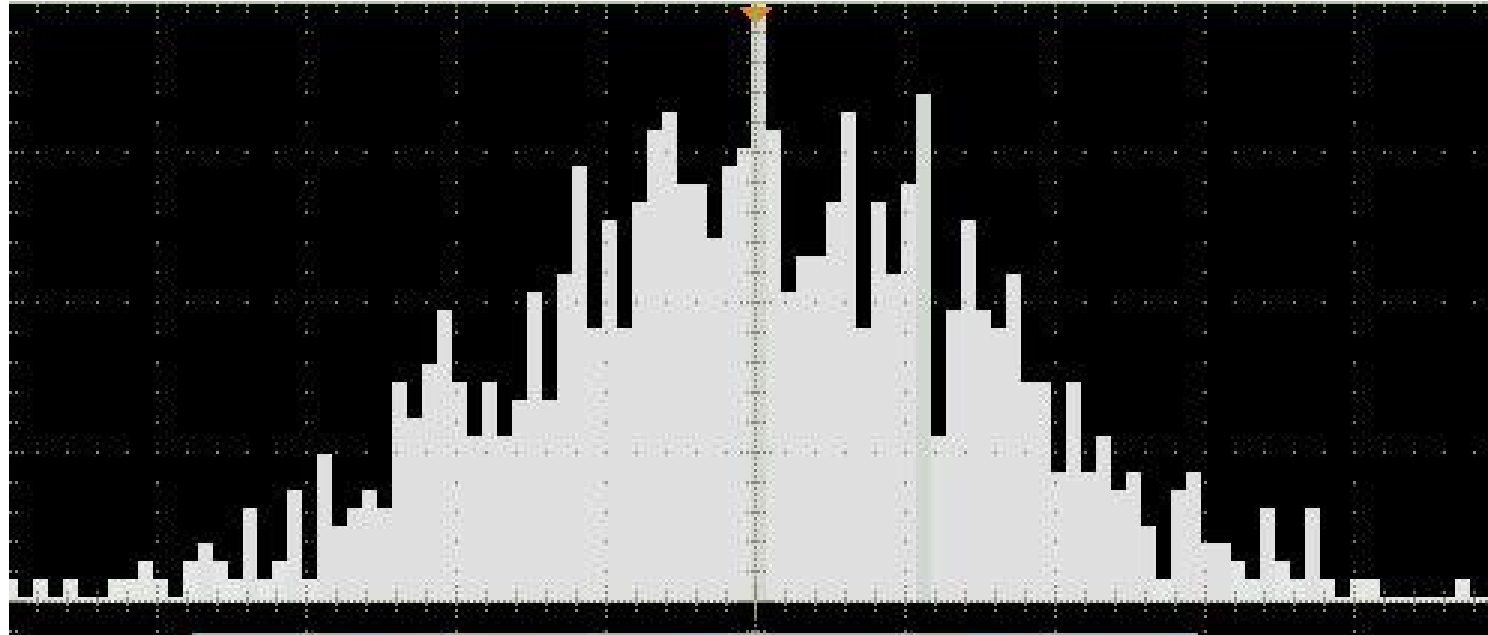
Clock Period	
Mean	25.000ns
Max	25.013ns
Min	24.984ns
Pk-Pk	28.760ps
Std Dev	4.7967ps
Population	656

Clock TIE	
Mean	0.00s
Max	13.771ps
Min	-12.916ps
Pk-Pk	26.687ps
Std Dev	3.2663ps
Population	959
Est Freq	39.999MHz

Digital Functions

Digital Functions:

- Parallel I/O interface MUX
- Scrambler De-Scrambler
- Encoder decoder
- Frame aligner logic
- Frequency calibration logic
- I2C interface

Engineers:

- Alessandro Marchioro - CERN, Switzerland
- Paulo Moreira - CERN, Switzerland
- Christian Paillard - CERN, Switzerland
- Ken Wyllie - CERN, Switzerland

Status:

- Fully functional
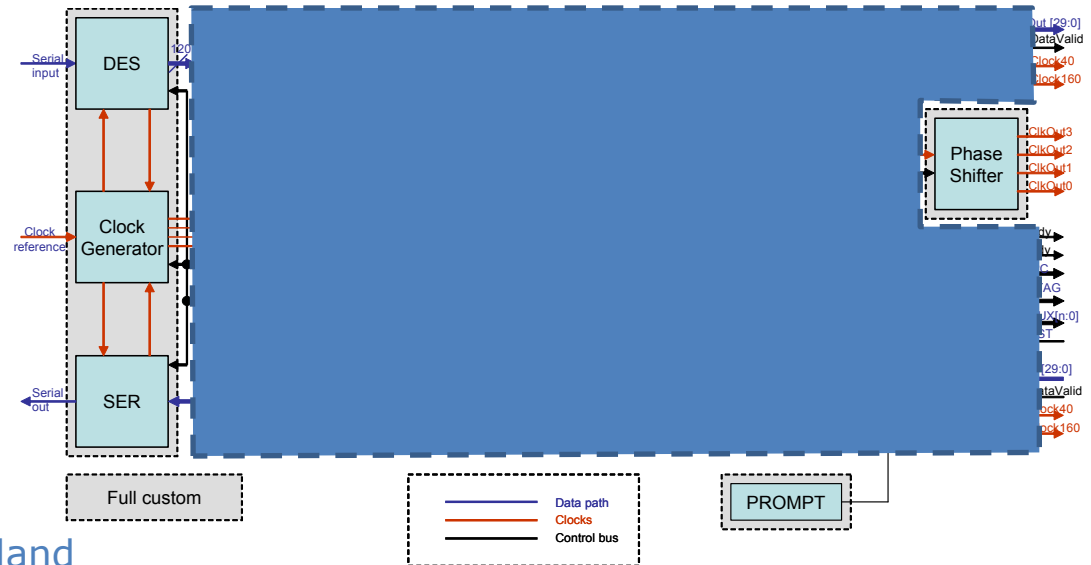
GBT – SerDes Power Consumption

Circuit	Power [mW]
CDR	456
Serializer	330
3 ch Phase-Shifter (+ 2 diff. drivers = 10 mW)	94 (≈ 16 mW/Ch + PLL: 42 mW)
I/O	75
Digital Core	27
Total	980

GBTX Block Diagram
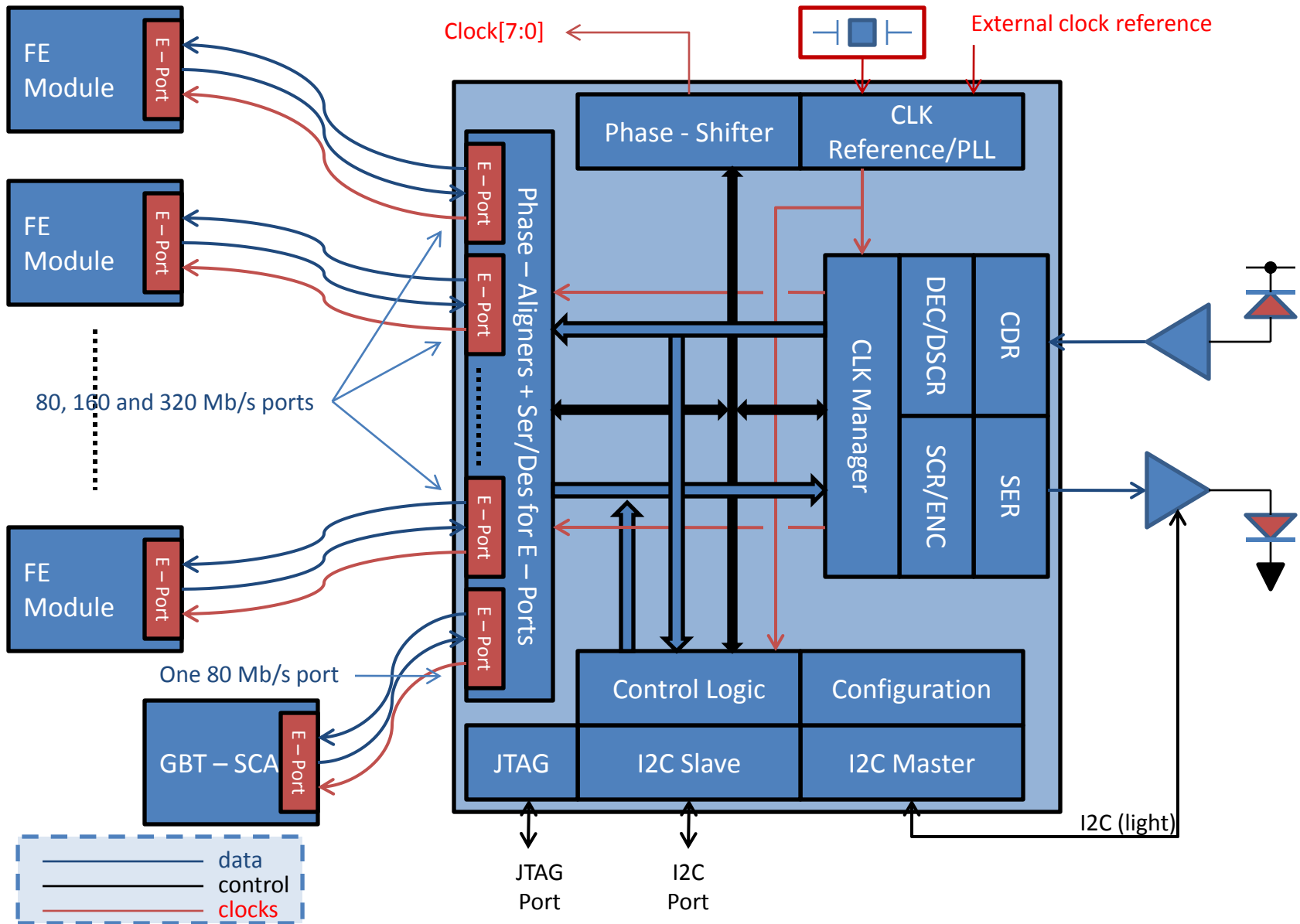
GBT Link Bandwidth

- Bandwidth:
  - User: 3.36 Gb/s
  - Line: 4.8 Gb/s
- Generic data field:
  - 3.2 Gb/s (80-bits)
- Dedicated channels:
  - Link control: 80 Mb/s (2-bits)
  - Slow control channel: 80 Mb/s (2-bits)
- DC balance:
  - Scrambler
  - No bandwidth penalty
- Link is bidirectional
- Link is symmetrical
- Down-link highly flexible:
  - Can convey unique data to each frontend device that it is serving
  - "Soft" architecture managed at the control room level

- Frame Synchronization:
  - Redundant header
- Forward Error Correction:
  - Interleaved Reed-Solomon double error correction
 - 4-bit symbols (RS(15,11))
  - Interleaving: 2
  - Error correction capability:
    - $2_{\text{Interleaving}} \times 2_{\text{RS}} = 4 \text{ symbols} \cong 16\text{-bits}$
  - Code efficiency: 88/120 = 73%
- Transmission protocol easily implemented in modern FPGAs

User field (84 bits, 3.36 Gb/s)

H	IC	EC	D	FEC
4	2	2	80	32

SC

Frame: 1 SLHC Clock Cycle (120 bits, 4.8 Gb/s)

GBTX – to – Frontend Communication

Mode	Type	Data Rate	Notes
OFF	Power off	-	
P-Bus	parallel	80 MW/s	One 40-bit word (DDR)
B-Bus	parallel	80 MB/s	Up to 5 Bytes (DDR)
N-Bus	parallel	160 MN/s	Up to 5 Nibbles (DDR)
2 ×	serial	80 Mb/s	Up to 40 serial links
4 ×	serial	160 Mb/s	Up to 20 serial links
8 ×	serial	320 Mb/s	Up to 10 serial links
8 ×	lanes	> 320 Mb/s	See "Lanes"

JEDEC standard, JESD8-13
Scalable Low-Voltage Signalling for 400 mV (SLVS-400)
http://www.jedec.org/download/search/JESD8-13.pdf

- GBTX – to – Frontend interface:
  - Electrical links (e-link)
  - Bidirectional
  - Operate in:
    - Serial and Parallel Modes
  - Up to 40 active links
- E-Link:
  - Three pairs:
    - D_{OUT}: GBTX –to – Frontend
    - D_{IN}: Frontend – to – GBTX
    - CLK: GBTX –to – Frontend
- Programmable data rate:
  - Independently for up/down links
  - Independently in five groups (of up to 8 links each)
  - 80, 160 and 320 Mb/s
- Lanes:
  - To achieve > 320 Mb/s
  - Two or more e-links can be grouped forming a "lane"
- Slow data rate channel:
  - Fixed data rate: 80 Mb/s
  - General purpose data transmission
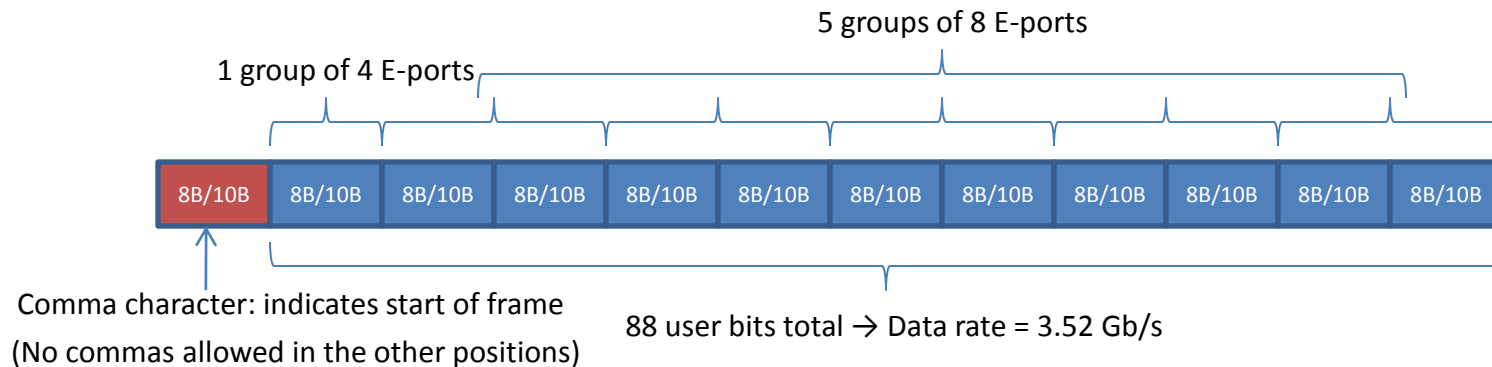 - Compatible with GBT – SCA
- Electrical standard:
  - SLVS electrical levels:
    - 100 Ω termination
    - 400 mV differential
    - 200 mV common mode
    - I_{LOAD} = ±2 mA

GBTX 8B/10B Transmitter Mode

- In this mode:
  - 8B/10B encoding is used
  - No SEU protection
  - **Only available in the simplex transmitter mode**
- Motivation:
  - Simplicity of the FPGA receiver
  - Significant reduction of the resources used by the GBT receiver in the FPGAs
- Implementation:
  - A first special word is required for frame synchronization:
    - Comma character will be used
  - Idle/data frames:
    - Data frame (txDataValid = 1): One comma character followed by 11 8B/10B words
    - Idle frame (txDataValid = 0): To be specified!
  - The 12-word 8B/10B encoder will very likely require additional GBTX latency!
  - To reduce the package cost and the pin count some of the (normally) GBTX output ports will work as inputs
- Bandwidth:
  - User bits: 88 (82 in the GBT protocol)
  - User data rate: 3.52 Gb/s (3.28 Gb/s in the GBT protocol)
    - 3.52 Gb/s vs 3.28 Gb/s → 7.4% increase only!

5 groups of 8 E-ports

1 group of 4 E-ports

| 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B | 8B/10B |

Comma character: indicates start of frame
(No commas allowed in the other positions)

88 user bits total → Data rate = 3.52 Gb/s

GBTX Chip and Package Size

- Total pin count: 434

- Chip size: $5.5 \times 5.5 = 30.25$ mm^2

- Fits a 21×21 pin Package

- Approximate package size:
  - 1 mm pitch: 22×22 mm^2
  - 0.8 mm pitch: 18×18 mm^2

E-Ports (DIFF: IN/OUT/CLK)	264
E-Port SC (DIFF: IN/OUT/CLK)	6
Transmitter	12
Receiver	12
VCXO PLL	10
Phase-Shifter	16
I2C Slave	2
I2C Master	3
JTAG	5
E-Fuse Programming	4
Chip control	12
I/O Power	34
I/O Ground	34
Core Power	10
Core Ground	10
Total	434
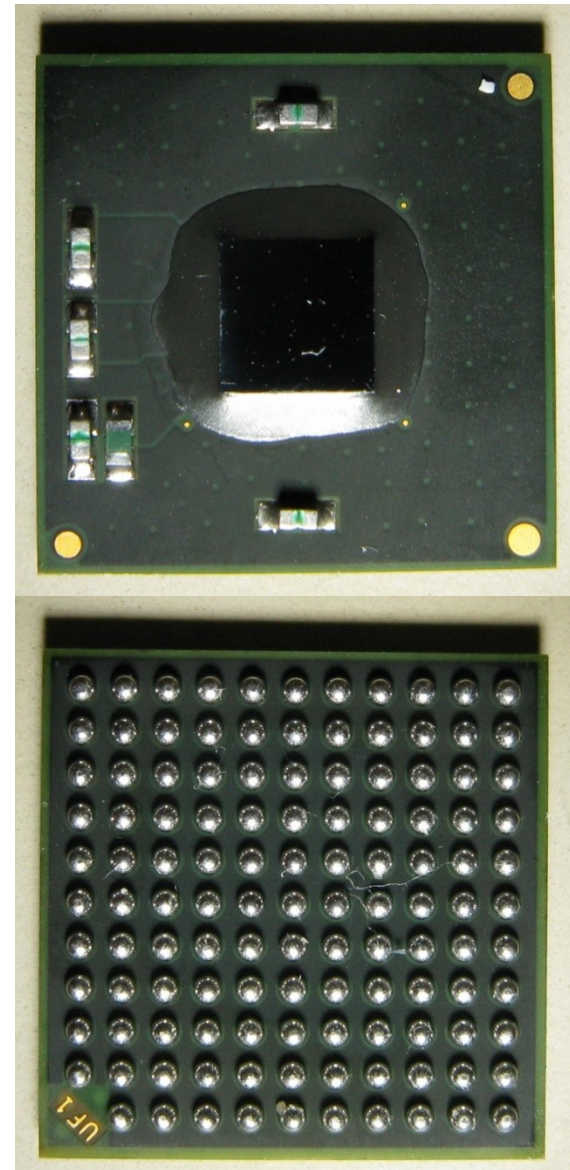
GBTX Power Consumption

GBTX Circuit	Vdd [V]	Idd [mA]	Power [mW]	Comments
CDR	1.5	304	456	Measurement
Serializer	1.5	220	330	Measurement
Phase-Shifter	1.5	167	251	Estimated for 8 channels based on a 3 channel measurement
E-link output data buffers (44)	1.5	88.0	132	Simulation (SLVS driver with maximum current settings)
E-link clock buffers (44)	1.5	88.0	132	Simulation (SLVS driver with maximum current settings)
Phase-Aligners (11)	1.5	27.7	42	Estimated
Digital core	1.5	23	35	Estimated based on current measurement and new functionality
Other I/O	1.5	10.0	15	Estimated
VXCO PLL	1.5	5	8	Estimated
E-Link input data buffers (44)	1.5	4.4	7	Simulation
E-link de-serializers (11)	1.5	2.5	4	Estimated
E-Link serializers (11)	1.5	2.5	4	Estimated
Clock Manager	1.5	1	2	Estimated
Total	1.5	943	1414	

- CDR
- Serializer
- Phase-Shifter
- E-link output data buffers (44)
- E-link clock buffers (44)
- Phase-Aligners (11)
- Digital core
- Other I/O
- VXCO PLL
- E-Link input data buffers (44)
- E-link de-serializers (11)
- E-Link serializers (11)
- Clock Manager
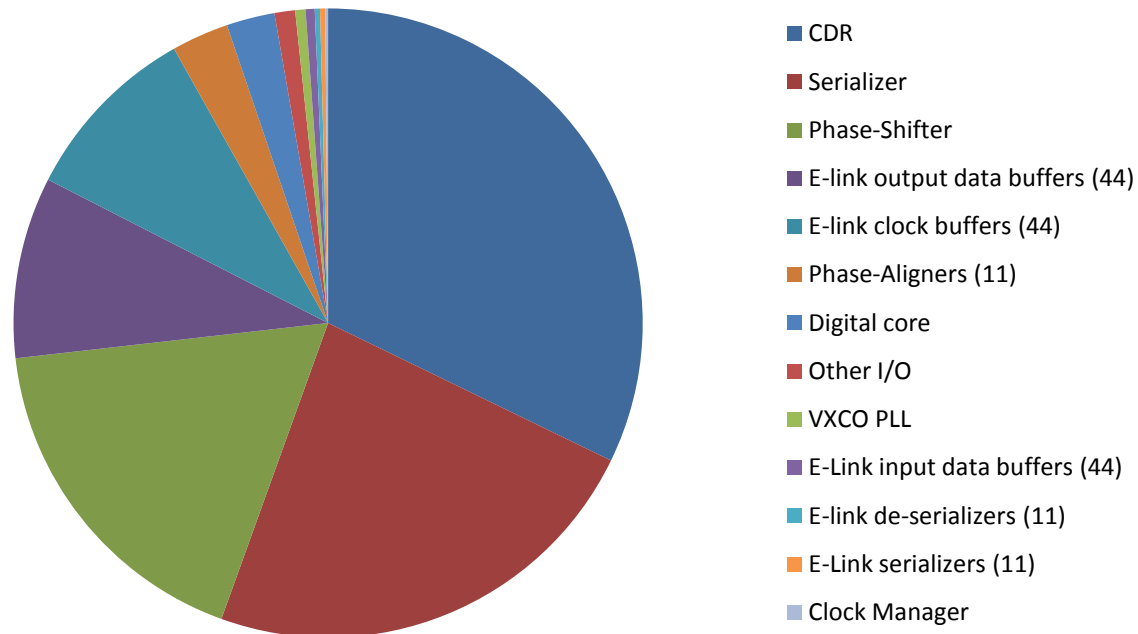
Project Schedule & Manpower

Tasks remaining:
- GBT – SerDes:
  - Understanding the receiver behaviour:
    - 3 Gb/s error free operation instead of 4.8 Gb/s
  - SEU tests
- GBTX:
  - Receiver rework (if needed)
  - Power down functions (SER/CDR)
  - TX 8B/10B mode
  - Clock Manager
  - VXCO based PLL
  - 8 channel Phase-Shifter (only 3 on GBT - SerDes)
  - Implement the 8B/10B transmitter mode
  - E – Links
    - Bi-directional C4 pad
    - Serializers
    - Phase-Aligners
  - E-Ports:
    - Implement a bidirectional C4 pad with switchable termination resistor
  - Control Logic:
    - Watchdog and start-up state machines
    - IC channel logic
    - I2C master
  - Configuration logic:
    - Fuse bank
  - Chip assembly and verification
  - From industry:
    - BGA package (flip-chip)
    - 80 MHz crystal
  - Testing:
    - Test setup (should we use the IC tester?)
    - Early behavioral model needed for test development
    - Software
    - Firmware
- GBLD:
  - Change the input protection diodes, change I/O to 1.5V
- GBTIA
  - Change pad ring, add average power detector and add squelch circuit
 - Migration from the LM to the DM technologies flavor
  - 2.5V Supply

Project Schedule 2011
- 1st Q:
  - SEU tests on GBT – SerDes
  - GBLD submission
  - GBTIA submission
- 3/4th Q: GBTX submission

The Gigabit Link interface Board (GLIB)

- GLIB concept:
  - Evaluation platform
  - Easy entry point for users of high speed optical links
- Intended use:
  - Optical link evaluation in the laboratory
  - Control, triggering and data acquisition of remote modules in beam or irradiation tests
- Each GLIB card:
  - Can process data to/from four SFP+ transceiver modules
  - Each operating at bi-directional data rates of up to 6.5 Gbps.
- Matches comfortably the specifications of the GBT/Versatile Link:
  - Target data rate of 4.8 Gbps.
- Basic configuration:
  - One GLIB board interfaces with up to four GBT channels
- Physical implementation:
  - Double width Advanced Mezzanine Card (AMC)
  - Based on the XC6VLX130T FPGA of the Virtex-6 family
- Long lifetime:
  - Distribution and support of a small set of variants over several years
- Engineering contacts:
  - Sophie Baron
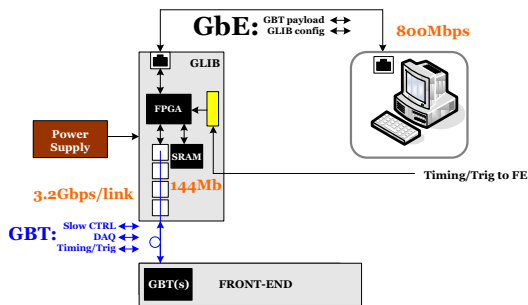 - Francois Vasey
  - Paschalis Vichoudis
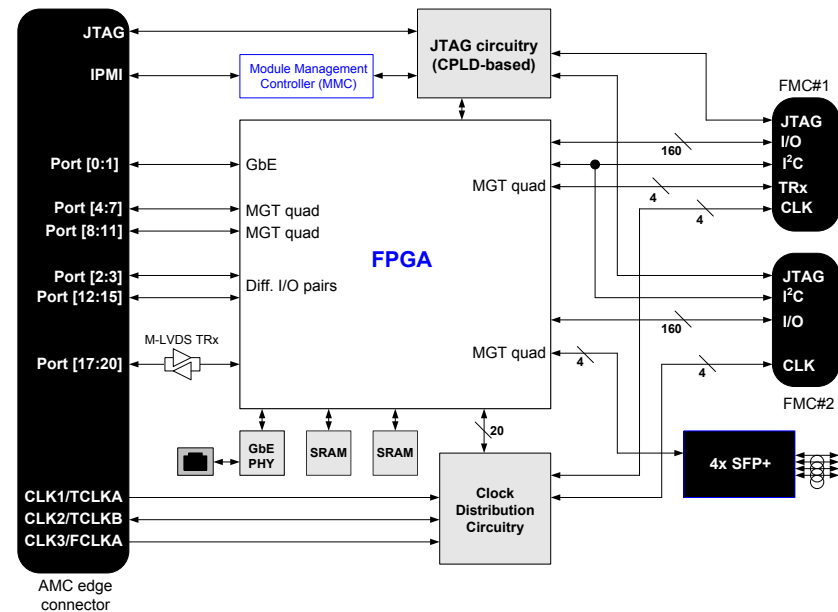
GLIB Deliverables

- The GLIB team envisages to deliver and support:
  - Software
  - Firmware
  - Hardware
- 3 Basic setups:
  - Bench-top beam test setup
  - Bench-top front-end module test setup
  - Crate system test setup
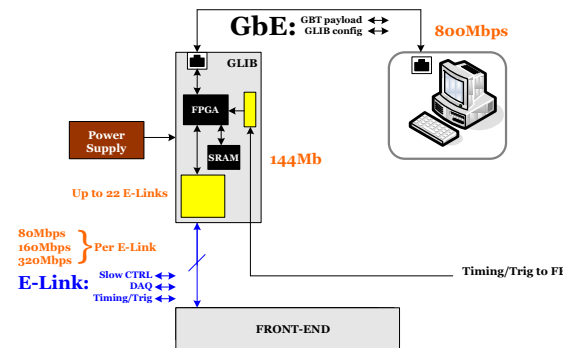- The required FMCs (TTC & E-Link) will also be delivered and supported.

Status:
- Specifications
  - V1.9 available.
- Design
  - Schematics: Ready.
  - Layout: Ready. Verification on-going
  - Fabrication: Prototype Feb 2011
- Testing:
  - Commercial solutions will be used
- Software/firmware:
  - Development will start in 2011

Bench-top beam test setup

Bench-top front-end module test setup

Crate system test setup