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FE electronics for Sci-Fi tracker for LHCb upgrade

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Abstract

For the LHCb upgrade leading to a complete readout at 40 MHz readout all electronics requires an important redesign. For the Inner Tracker we study the possibility of using a Scintillating Fibre Tracker Sci-Fi tracker instead of the current Si strip technology. The SiPM light detection device used for the Sci-Fi requires adapted FE electronics which is discussed in this document.

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1 Revision

Version 1.1, 25. November 2010
Includes some feedback from Ken. **Version 1.0, 18. November 2010**
Initial version

2 Introduction

With the current development for the Velo using a pixel detector makes the reuse of the Velo FE chip for the tracker impossible. The electronics for the tracker therefore needs to use a custom designed readout chip adapted to the SiPM in case of the use of Sci-Fi. The specification for a SiPM and Si strip detector FE chip can not be merged into one design - the very large signal of the SiPM is about 300 times larger than the one for Si strip detectors. In this document we try to collect the requirements for the FE electronics for a Sci-Fi detector in LHCb upgrade. The architecture that is shown in Fig. 1 splits the FE signal amplification and shaping, the digitization and the zero suppression into three separated blocks. The reason it is described in this way is to avoid the impression that only a single chip solution can be used for the tracker readout electronics. In the following we discuss different parameters that need to be considered for the electronics development.

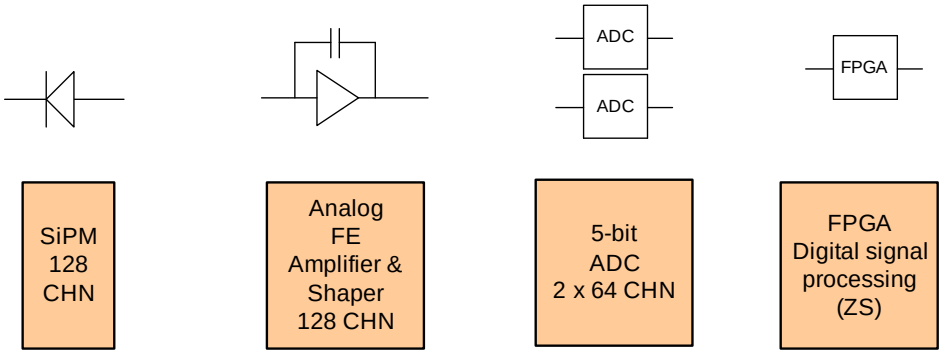

Figure 1: *Signal processing chain for the SiPM detector with analog FE, ADC and digital signal processing on the FPGA.*

3 Description

The electronics for the Sci-Fi tracker is considered to be located outside the acceptance of the LHCb experiment, possible locations are 3m above and below the inner tracker detector. The transport of the signal from the Sci fibres to the outside locations is assumed to be done with a clear fibres. The clear fibre interface is a layer of fibres with the same geometry as the detector but constructed with non scintillating fibres. The interface (transport of the light from the inner to the outer region of the detector) is imposed by two very strong arguments. First is the fact that the SiPM detectors used

to detect the optical signal are not sufficient radiation hard. The SiPM detectors need to be in a shielded box (plastic shield for thermalizing the neutrons) where the neutron flux is significantly reduced. Second the space constraints in terms of data processing, cooling and data transmission requires a very advanced readout chip if done at the detector itself. Only a fully integrated solution with analog preamplifier, shaper, ADC, ZS and data transmission can be envisaged with the space constraints present.
The radiation level for the electronics at this place (shielded) is supposed to be at least 10 times below the current LHCb radiation level) otherwise the SiPM can not be used.

3.1 Amplifier and shaper requirements

The FE amplifier and shaper can not be made to be usable for SiPM and silicon strip detectors. The dynamic range is very different for the two detectors and therefore in the following only the SiPM detector requirements are considered.

- The SiPM should be connected directly to the input of the pre-amplifier, any external resistors or capacitors should be avoided. Note that with one resister and one AC decoupling capacitor results in a total of 768 components on the hybrid with 3x128 channels. (VATA64 (Ideas) shows that this is possible). The input impedance is defined with the requirement of no external termination resistor.

- 128 channel is the size of the SiPM modules, it is naturally also the number of channels of the readout chip. (64 channels is also possible, two chips per SiPM module can be employed.)

- Each channel should have its (8-bit) DAC to adjust for gain variations. There is no thresholds for signal detections at this point since the signal is digitized in the next processing step.

- Sinking the dark current must be implemented. Small capacitance and small dark current, area is $A = 0.25mm^2$, detector terminal capacitance $C_t = 9pF$, dark current $I_{Dark} = 8nA$.

- The peaking time is smaller than 25ns imposed by the LHC bunch crossing rate.

- The dynamic range of the signal detection is 0 to 30 photons. Explanation: One MIP is expected to produce 15 photons in the $1.1mm$ scintillating fibre layer, this is reduced by probably 50% at the clear fibre interface. With a gain of $0.75 * 10^6$ e/photon the total dynamic range is 0 to 3.6pC. The dynamic range therefore is 0 to about 5 MIP as for the silicon strip detector used for IT in LHCb.

- The voltage level of the full range output must be defined with the specialist for the ADC. The dynamic range is very small and should not be a major problem, current output is maybe an option. We should mention here that also a time over threshold measurement could be envisaged instead of a real ADC. Specialists in this field can maybe comment. Note that the short shaping time and the fact that the next event arrives possibly only 25ns later can make the time over threshold measurement very difficult. The time over threshold measurement can maybe be combined with the FPGA capability to sample the output of the threshold signal and conversion into a digital value.

- Only with a linear response the center of cluster position can easily be calculated from the ADC values. Conversions for calibration should be avoided if possible.
- S/N ratio of 10 is required, this is not a major difficulty to obtain but leaves important margin in the noise suppression.
- Spill over, without DSP the spill over generates additional clusters in the next bunch crossing, so keeping this low allows certainly to avoid expensive processing. (30% was given in the Beetle for LHCb). Double pulse resolution at 25ns.
- Detector occupancy is expected to be about 5 to 6%. The SiPM is recovered immediately since only a small fraction of the pixels is discharged after a signal.
- Output is expected to be one analog signal per channel.
- Packaging the chip should be considered and is certainly preferred. Certainly (F)BGA, 128 input and 128 outputs are required, space constraints!

3.2 ADC

A second ASIC is required for the digitization of the analog signal. Since the channel to channel interpolation is required to obtain a resolution that is better than $250\mu\text{m}/\sqrt{12} = 72\mu\text{m}$ (see [**?**]). The alternative option is to use a time over threshold system which may make the ADC chip not necessary.

- ADC number of bits should be at least 5. The dynamic range of 0 to 30 photons and a low noise of 0.1 photons is guarantee that little noise clusters are produced.
- Input is the signal from the analog FE chip.
- The output should be a serialized bitstream where for example the 5 bits from one ADC are transmitted on one digital signal at a 5 times higher frequency $(5 * 40MHz = 200Mbit/s)$
- The number of channels doesn't necessary need to be the same as for the analog FE, two 64 channel chips could be combined to allow for reasonable power per chip.
- chip needs to be packaged, (F)BGA 64(128) input and 64(128) outputs are required, BGA has to be considered due to space constraints!

3.3 FPGA

Antifuse Actel FPGAs are required in the radiation area. Note that the location where the electronics is placed needs to have some radiation shielding for the SiPM detectors. The FPGA should be also housed behind this shield (30krad only is supported by this technology). The FPGA needs to perform zero suppression and interfacing to the GBT via electrical connections. Since the radiation protection is present for the SiPM this may allow even to use SRAM based FPGAs at this place. We need an estimation of the radiation environment at the electronics location.

References

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