Update of Development of ECS unit for Counting Room Electronics

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Topics

1. The Concept
2. The Design
3. The Development
   - The Hardware
   - CCPC Software
   - PCIe core ↔ I^{2}C
   - NIOS & JTag
4. The prototype
5. Conclusion and Remarks

The concept of the project

goal

Gen Purpose ECS unit for Config, Mon and Debug: access PVSS in control room (CR)

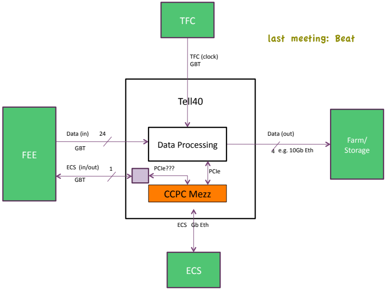
CR ↔ Ethernet ↔ embedded PC ↔ $\underbrace{\text{PCIE}}_{\text{high speed (HS)}}$, $\underbrace{\text{I}^2\text{C, JTAG, SPI}}_{\text{low speed (LS)}}$ ↔ board

focus on TELL40 board

TELL40 ECS Scenarios

dedicated Processor for TELL40

dedicated Processor for TELL40 ↔ FEE



last meeting: Beat

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focus on TELL40 board

Compactness

Unique Mezzanino & exploring FPGA in low speed line

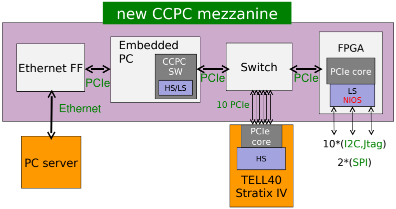
Schedule expectation

Prototype → Final HW & SW → Validation 2011-12

Mass Production → Installation (?)/16

The Design

- CCPC with 2 PCIe lanes:
  1Gbs LAN + Switch
- Switch drives:
  → 10 PCIe lines to TELL40
  HS block transfer
  → 1 PCIe lane to FPGA
  translation to LS protocols
- 10 outputs I^2C
- 10 outputs JTAG no chain
- 2 outputs SPI



The Design: main components

1. The embedded PC: **SMA 200 digital logic**

   SmartCore Atom Z530, 1GB, DDR2 RAM

   1.1 GHz, connector and heatspreader

   PCIe 1.0: 2 lanes x1 (2.5Gbs)

2. The FPGA → LS line: **Cyclone *IV* GX**

   EP4CGX22: 22k LEs, 150 I/Os, 4 transceivers

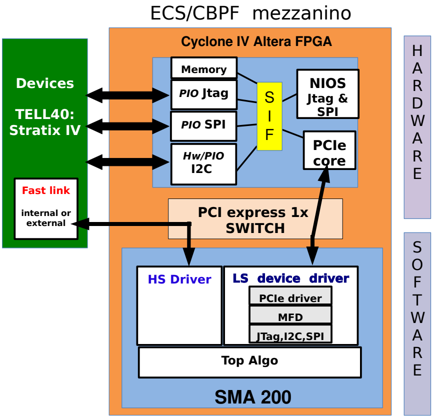
   or (to be studied) EP4CGX15: 14.4k LEs, 72 I/Os, 2 transceivers

3. The PCIe Switch → low latency, 1+10 ports: **PEX 8614**

4. The Ethernet: **Mini−PCIe Form Factor (Intel 82574L)**

   (at least for 1^0 prototype)

The ReDesign: HW & SW diagram



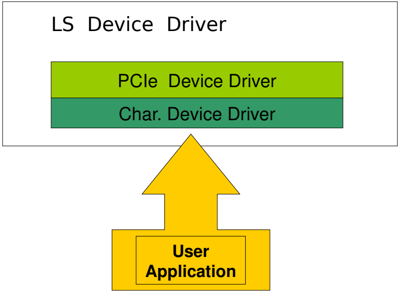
The Hardware

- **CBPF Setup** → SMA200 & Arria II kits
- **CERN Setup** → SMA200 (thanks Beat & Niko) & Cyclone IV (thanks Guido) kits
- next year ECS-CBPF proto $\triangleleft - \triangleright$ Validation board (test protocol + guideline for Collaboration concerning implementation of PCIe physical lines)

The CCPC Software: driver

The previous driver release:

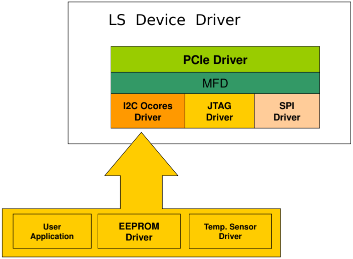
1. Probe and identify the device on PCI Bus
2. Allocate resources on PCI device for use in other drivers
3. Provide access for UserApp directly to PCIe device



The CCPC Software: driver

The new driver (phylosofy useful to SOPC builder)

1. The UserApp cannot access the PCI regs directly
2. Each controller have your own driver and the UserApp access from it



The CCPC Software: driver

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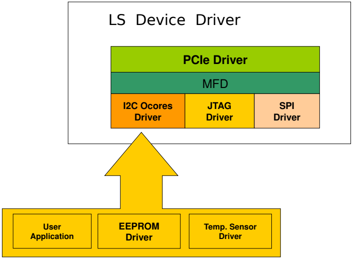
2. Each controller have your own driver and the UserApp access from it
3. PCIe Device Driver: inherited from first release and included an interrupt handler ⟶ working on it
4. Multi-Function Device Driver: Kernel Driver for devices with > 1 function; responsible for distribute the resources
5. I2C Ocores Driver: Abstract the control of the i2c controller ⟶ need to integrate with interrupt handler
6. JTAG and SPI Driver: soon



PCIe core ↔ I^{2}C

PCIe core: SOPC builder

1. fully featured PCI Express block component → only native endpoint
2. PCI Express Avalon-MM Bridge: translate messages across the busses, a built-in PCI Express Protocol Stack (Completer/Requester) and Interrupt controller

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I^{2}C OpenCore Controller

1. Compatible with Philips I^{2}C Standard
2. SW programmable clock frequency
3. Normal / Fast and High Speed Operation mode
4. Supports 7 and 10 bits addr mode
5. Adapted to use with Avalon-MM as slave
6. More than one controller can be used on system

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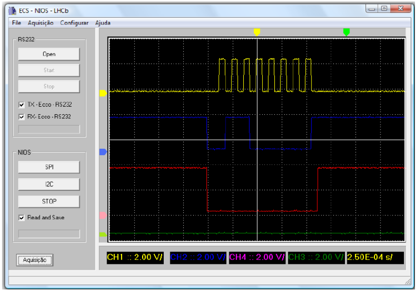
As soon as the interruption issue at driver level is finalized
(few weeks) the I^{2}C CHAIN will be ready for validation

NIOS & JTAG

- NIOS will be used to hold LS protocols but I^{2}C
- We have finished an interface to Test NIOS performance
  - **SPI** of ECS is done
  - **I^{2}C** is done, for test purpose



☑ TX - Ecco - RS232
☑ RX- Ecco - RS232
☑ Read and Save

CH1 :: 2.00 V/ CH2 :: 2.00 V/ CH4 :: 2.00 V/ CH3 :: 2.00 V/ 2.50E-04 s/

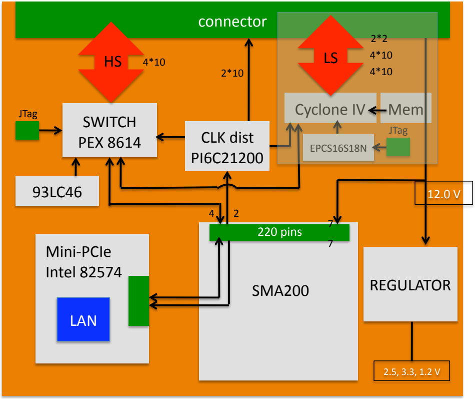
- JTAG SOLUTIONS $\left\{ \begin{array}{l} \text{C code Player NIOS: } \textbf{Compiled} \rightarrow \textbf{ready for testing} \\ \text{comercial IC on NIOS output: just start} \\ \text{JTAG code running in SMA200: under investigation} \end{array} \right.$

The Geometry

- **Geometry:** The Collaboration has defined the utilization of 2 slots for TELL40 space limitation & air flux is not a concern for our mezzanino (remind the additional cards: SMA200 with heatspreader, Ethernet)

The Schematic

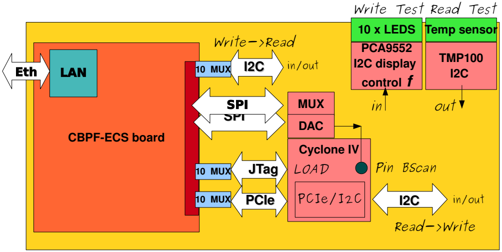
The Electrical schema is updated @Altium → HS line



Next step: Waiting the definition of Cyclone family to final PCB design & mount

The Validation board

- **Validation Board:** First approach → Test all 10 lines of JTAG (Load and Boundary Scan Test), I^{2}C and PCIe as well as the High Speed connectivity. Read (Temperature sensor) and Write (LED frequencies) Phases, to be applied to I^{2}C and PCIe↔I^{2}C lines **...** (thousand ideas: Read-Write on Memory, ... need to think on MUX/switch to drive the lines



Conclusion and Remarks

$$\text{We have redefined} \begin{cases} \text{HS} \rightarrow \text{10 PCIe lines} \\ \text{LS} \rightarrow \text{1 PCIe} \rightarrow \text{10 * [I}^2\text{C} + \text{JTAG]} + \text{2 * SPI]} \end{cases}$$

- **THE SETUPS:**

  new CERN Setup ready

  start design the Validation board

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- The Setups:

  new CERN Setup ready

  start design the Validation board

- The PCIe FPGA core & low level driver:

  - First Version of the PCIe using Memory Mapped in SOPC is ready
  - Second Version of the SCL driver using Memory Mapped under construction

  new phylosofy need to be validated and require some tricky treatment of interruptions

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- **THE OUTPUT COMMUNICATION:**

  SPI is ready in NIOS

  I^{2}C is ready outside (main solution) and inside (for test purpose) NIOS

  JTAG: three solutions are under investigation → C code player running NIOS (under test), running in SMA200 and the usage of a commercial device

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- THE PROTO PCB:

  The schematic of HS Line was updated

  As soon as we define the final archi → the FPGA family decision → schematic of LS Line

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- **The Schedule:**

  We are working parallely ... investigating different solutions

  The prototype will be ready first half of 2011