ITS Upgrade - WG4 Strip Upgrade

Outline |

- The present SSD
 - General description
 - Status & Performance
 - Possible improvements
- The strip upgrade
 - Layout options
 - Services
 - Performance goals

The present SSD — A starting point

The SSD detector

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overall dimensions: L x d ~ 1m x 1m A = (2.2 + 2.8) m²
Layer 5: radius = 38 cm ±z = 43.1 cm
Layer 6: radius = 43 cm ±z = 48.9 cm
acceptance coverage: |η| < 0.9</li>
#ladders (PS/DCS/DataTransfer unit): 144 (68+76)
#modules (readout unit): 1698 (748+950)
#FEchips (FE config unit): ~20k (12 chips/module)
#channels (signal treatment unit): ~2.6 millions
```

The sensor

- layout: doublesided 768 strip/side 95 μm pitch 35mrad stereo angle
- sensor area ~ 0.0028 m²
- achieved spatial resolution: 20 μm (rphi) 800 μm (z)

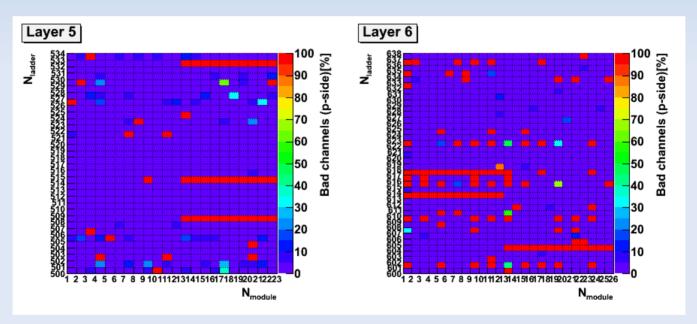
The front-end chip and electronics

- HAL25 mixed analogue digital ASIC designed; 0.25μ CMOS process
- 128 channels with preamplifier, shaper, storage capacitor
- ± 14 MIPs input dynamic range with good linearity
- 1.4 2.2 μs adjustable peaking time
- signal sampled by external Hold and read-out through analogue multiplexer
- serialized samples are then AC decoupled to multplx/buffer and driven to ADC

SSD status in 2010

• Overall efficiency

- Active modules: 1557/1698
- Active channels in active modules:
- Not operable half-ladders:
 - > single channels off: high noise, zero gain
 - modules/ladders off: electrical/configuration problems



Very good stability in Run 2010

- Max variation in active channels
- Presence in Physics Runs
- Good integration with central procedures
- Crucial role in tracking and PID

~ 90.3%

~ 91.7%

~ 98.5%

6/144

Present SSD - Possible improvements

New possible requirements from the upgrade studies concerning:

Acquisition rate

- Limited at ~3700Hz at present, due to a total dead time = 265 μs
- Sources of dead time:
 - 12x FEchip serial read-out time: ~ 160 μs +
 - endcap electronics "calm down" time $\sim 105~\mu s = 265~\mu s$

dE/dx capabilities

- nominal FEchip dynamic range: +/- 14 MIPs within 5% linearity
- confirmed by proton data analysis up to ~10 MIPs particles
- studies ongoing for highly ionizing particles/light nuclei
- possible asymmetric P/N charge collection (under investigation)

Signal optimization

- Intrinsic noise suppression: better control of env. conditions
- Common Mode noise suppression:
 - > better grounding of power lines
 - new algorithm implementation in the FEROM firmware

The strip upgrade - Layout

- Layout options (scenarios to be tuned according to the prompt WG2 outputs)
 - Replacement of present SDD with SSD-like modules
 - replace present SDD Inner layer: ~150 new modules
 - replace present SDD Outer layer: ~320 new modules
 - → ~500 SSD modules: to be scaled with the rapidity coverage, radius, no. of layers
 - new sensor production
 - same FEchips (6000xHAL25) possibly available
 - new production of microcables, front-end electronics
 - new design for services and supports
 - Complete re-design of the detector to fit the new physics performance requirements and the new position of the detector (occupancy, radiation, ...)
- Supports & Services (see WG5)
 - Integration with present SSD layers (if kept)
 - Integration with the rest of ITS upgrade
 - New cooling system, ...

The strip upgrade — Performance goals

- Performance goals (to be tuned according to WG1/2 outputs):
 - Acquisition rate: extend beyond 3700Hz (up to ?)
 - with present chip HAL25: different signal serialization
 - new endcap/bus
 - new chip
 - new read-out modules
 - dE/dx: extension of the dynamic range by redesign of electronics
 - Maximum occupancy handled: depending on radius, LHC beam energy
 - new sensor design decreasing strip pitch/lenght
 - new micro-connection design (pitch, geometrical tolerance)
 - new power consumption, cooling requirements
 - Material budget
 - Radiation tolerance of sensor and electronics

Summary

- The strip upgrade studies should move toward different scenarios following the first WR1/2 outputs
- The present SSD is a good starting point for first discussions and plans on
 - geometry layouts
 - required performance
 - possible improvements of the present components
- New solutions and designs should be investigated for
 - front-end chip
 - sensor
 - off-detector electronics
 - services