



Frontend System for High Granularity Calorimeter (HGCAL) in the CMS experiment

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On behalf of CMS Collaboration

Overview

CMS HGCAL: 47 Layers sampling calorimeter ($1.5 < |\eta| < 3.0$) for Phase-2 upgrade (present detector cannot operate under HL-LHC conditions) with large number of readout channels (~6.24 Million) operated at -30°C with CO_2 cooling

Active Elements:

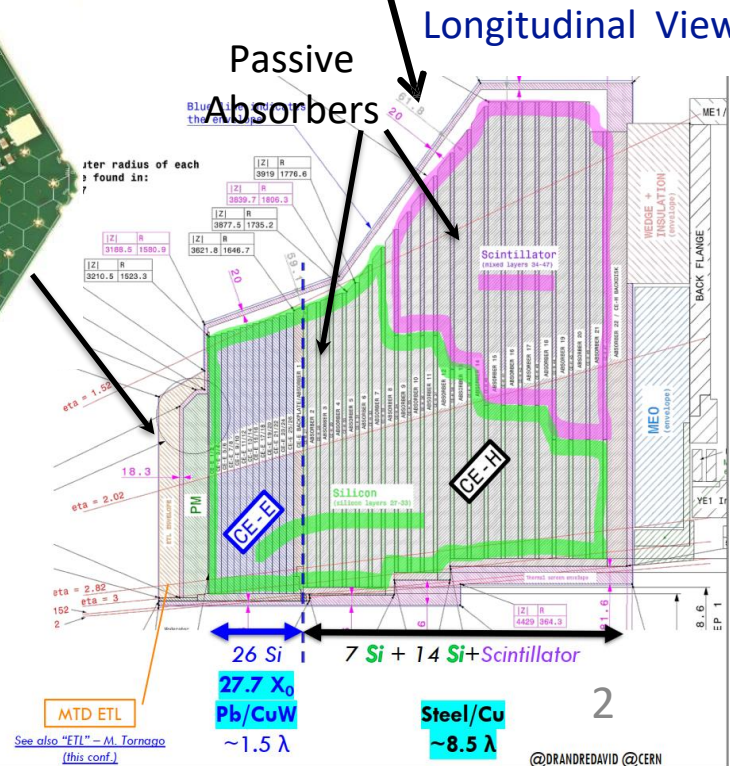
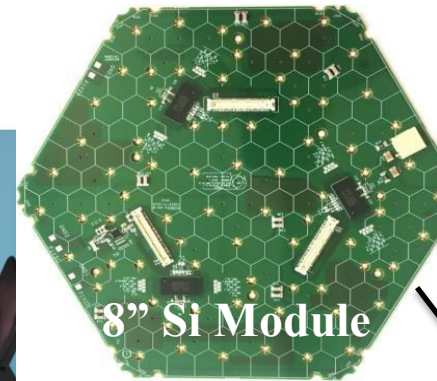
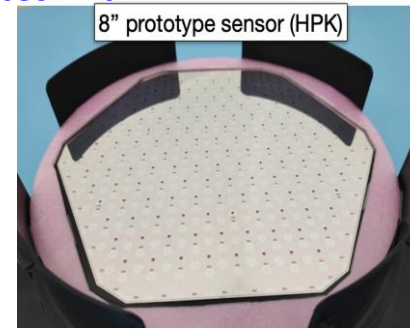
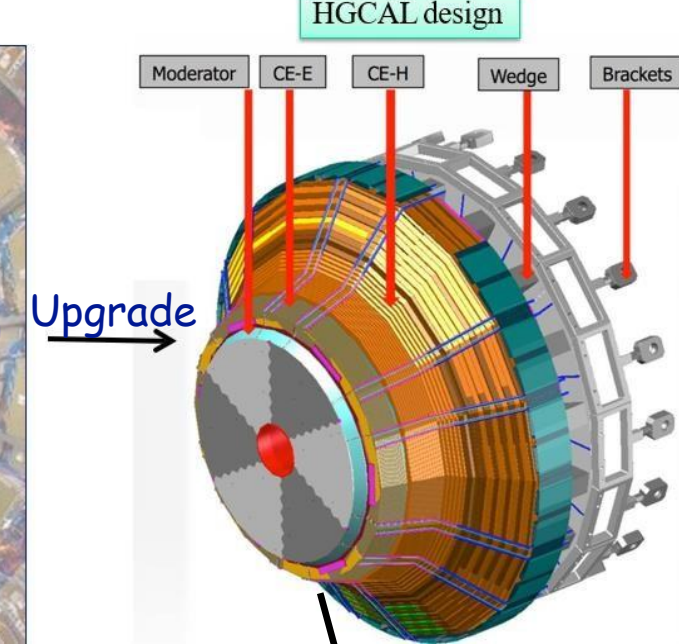
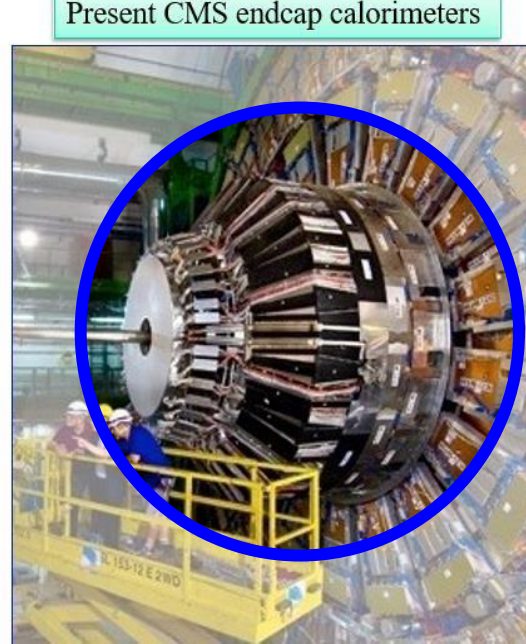
- 8" Hexagonal modules based on Silicon (Si) sensors in the electromagnetic (CE-E) and hadron (CE-H) calorimeter (~620 m², ~6 M Channels)
- Scintillating tiles with SiPM readout in relatively low-radiation regions of CE-H (~370 m², ~240 K Channels)
- **Cassettes:** Multiple modules mounted on cooling plates with electronics and absorbers

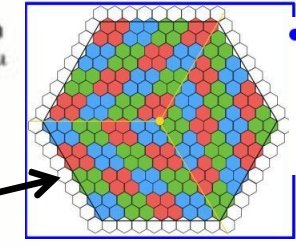
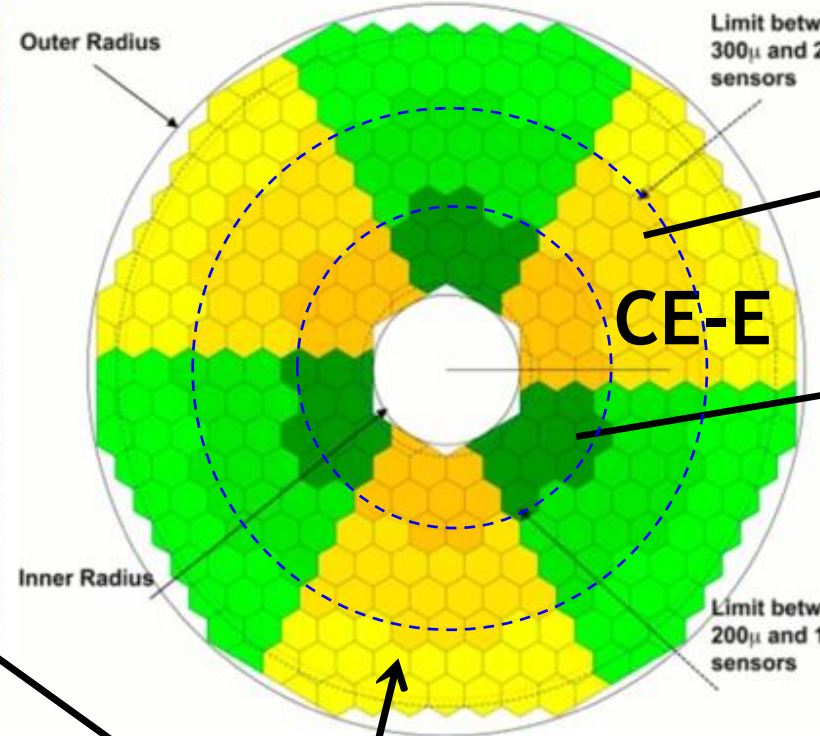
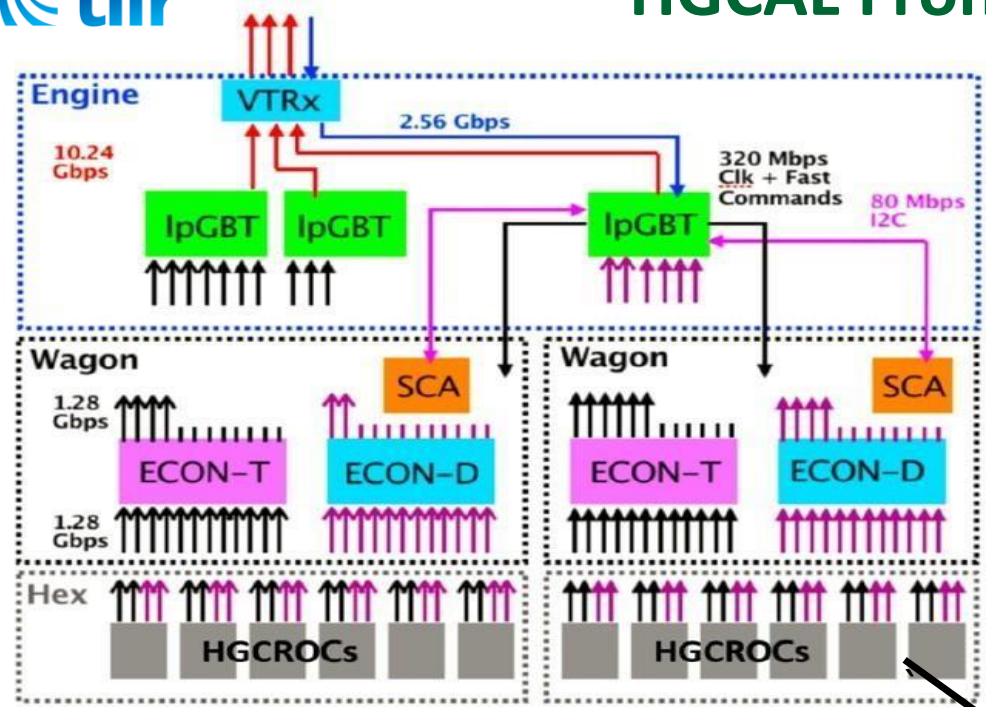
Absorber:

- Pb, CuW and Cu in CE-E (26 Layers)
- Stainless Steel and Cu in CE-H (21 Layers)

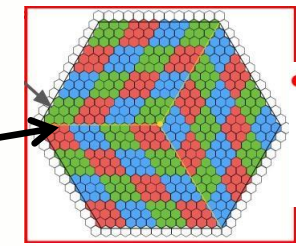
5D Imaging Calorimeter (x,y,z, ΔE, t):

- Highly granular spatial information (0.56 or 1.26 cm² for Si Cell, 4 to 30 cm² for Sc tiles)
- Large dynamic range for energy loss measurements
- Timing information to accuracy of ~30 picoseconds





- **Low density modules (LDM)**
 - 192 channels
 - cell size = 1.26cm²
 - Outer radii
 - 200µ, 300µ Si Modules



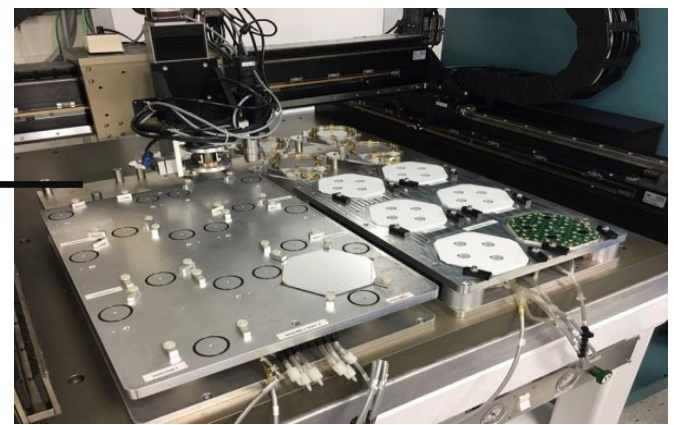
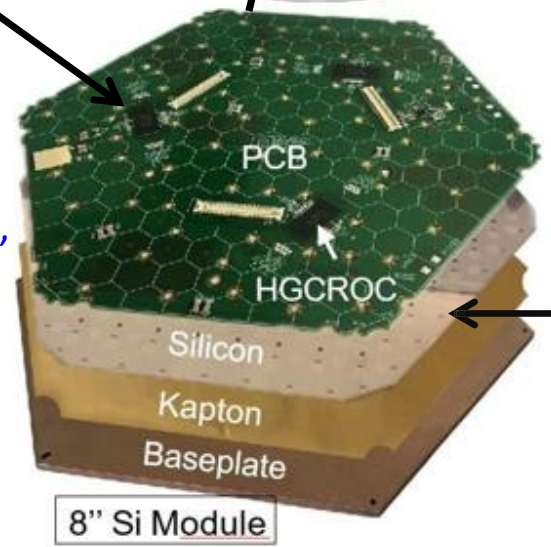
- **High Density Modules (HDM)**
 - 432 channels
 - Cell size = 1.056cm²
 - Inner radii
 - 120µ Si Modules

Si-Module:

- Glued assemblies, made with standardized Gantry, wire-bonders, encapsulation
- Sends bunch crossing synchronous data to concentrators
- ~31k Si Modules – 6 MACs

Concentrator ASICs:

- **ECON-T (trigger):** Frontend concentrator chip for trigger path, concentrates trigger channel data via one of 4 trigger algorithms before transmitting to the BE (Backend)
- **ECON-D (DAQ):** Frontend concentrator chip for DAQ path, performs channel alignment and zero suppression after L1Accept and sends to DAQ
- Trigger readout from alternate layers in CE-E and all layers in CE-H



Purpose:

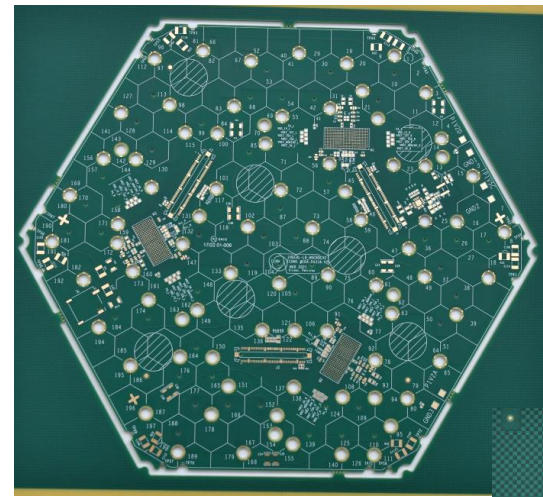
- Digitize (Hexaboard), Concentrate (ECON-T, ECON-D), and Transmit (low power Gigabit Transceiver (IpGBT) optical links) modules data to the TPG and data acquisition electronics
- Distribute clock and control signals (both “fast” and “slow”)
- Provide monitoring of e.g. temperature, currents, etc.

Requirements:

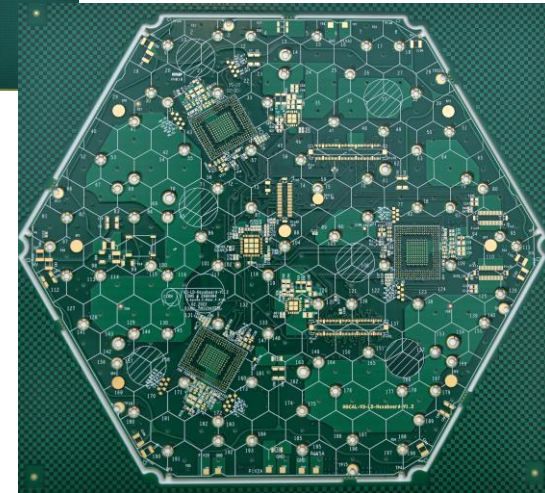
- Radiation tolerance up to 1.5×10^{16} neq/cm² in the inner detector region
- Fit in limited physical space
- Low power and support transfer of required data volume for good physical performance

TIFR Plans:

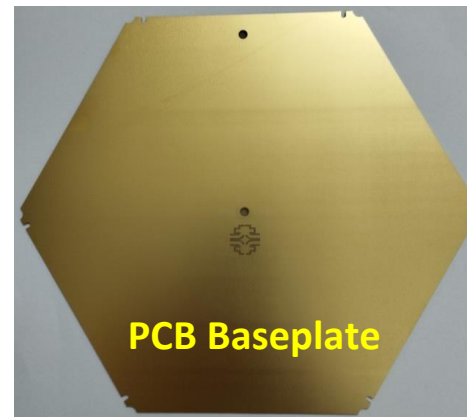
- Fabrication, Assembly and Testing of 8” Hexaboard PCBs, PCB based Baseplates and Cu/W based Baseplates



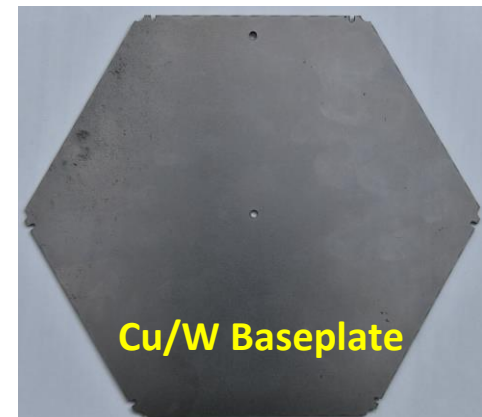
NSH Hexaboard



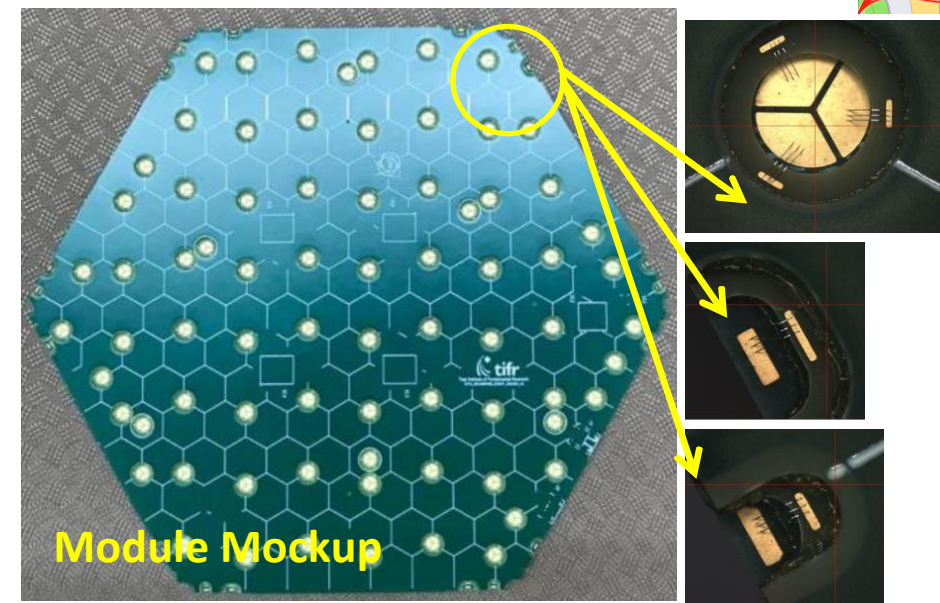
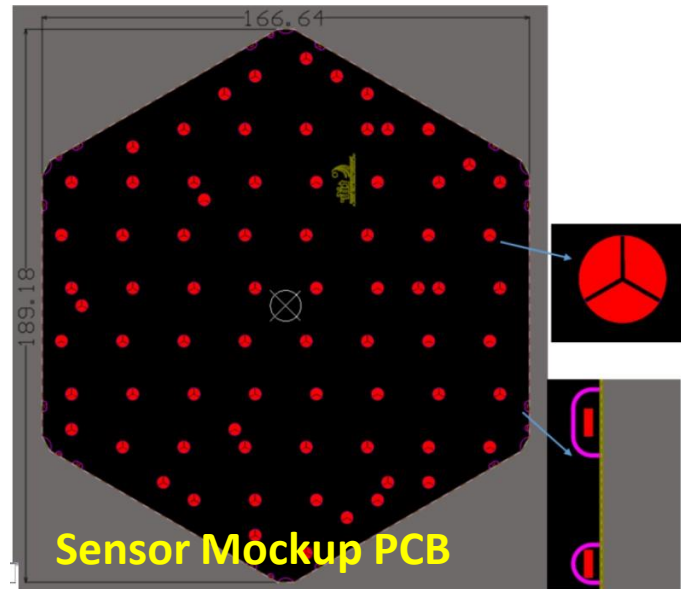
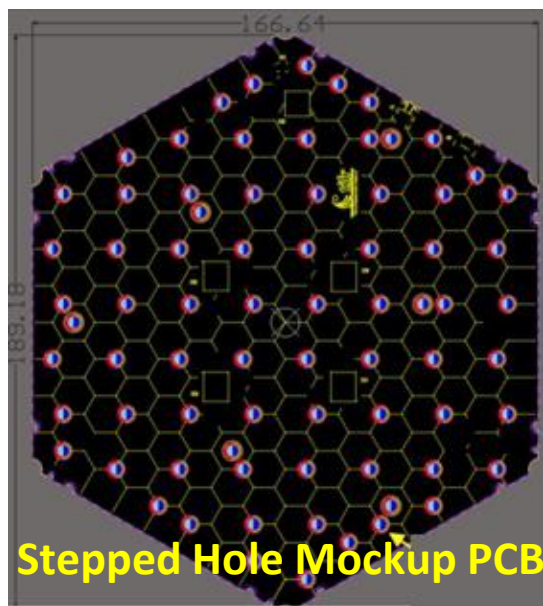
Stepped Hole Hexaboard



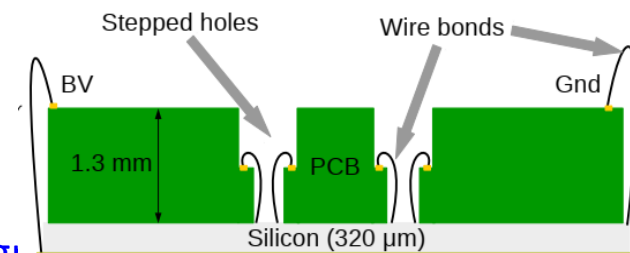
PCB Baseplate

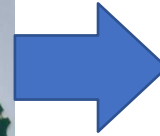
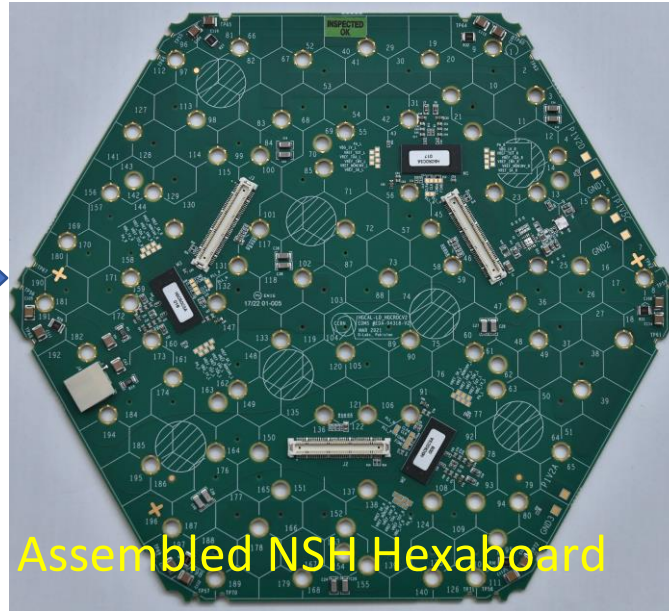
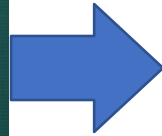
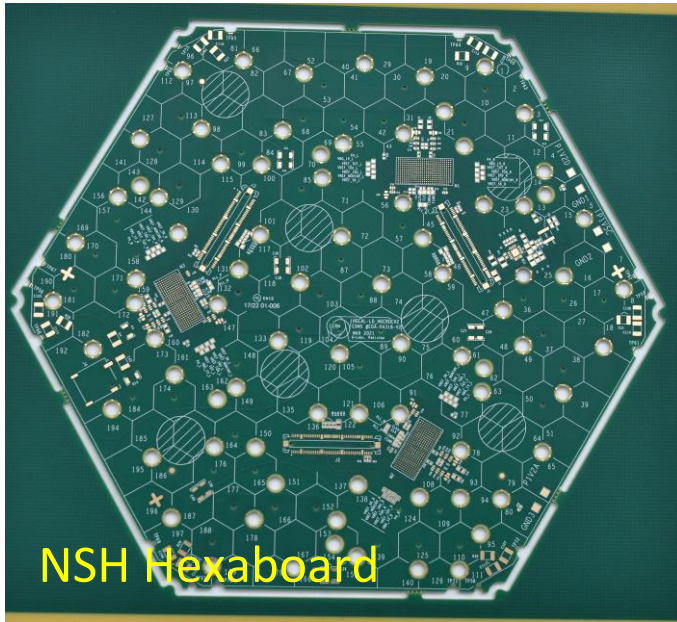


Cu/W Baseplate

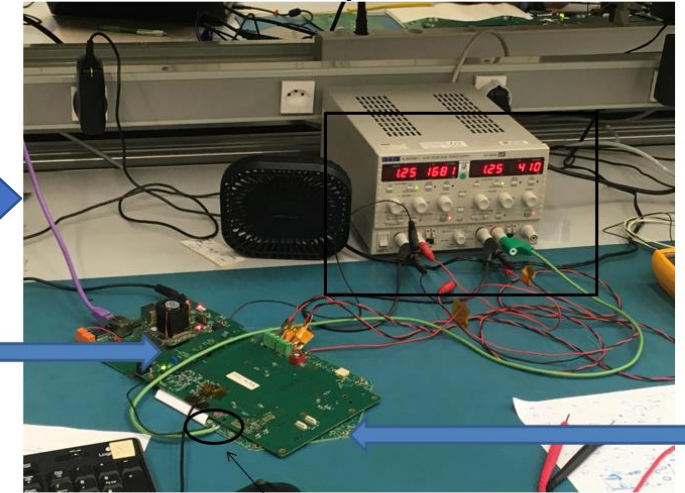


- Exercises of wire bonding and encapsulation carried out on dummy stepped hole Module matching with Silicon sensor pad geometry (No Circuits)
- Two PCB Concept: Stepped Hole design with bond pads at 120° + Sensor pad geometry design.
- Sandwich of two PCBs with a special glue with restricted flow
- Fabrication of Stepped Hole design is challenging, tricky and not a conventional job
- First version: Alignment offsets, glue dispersal issues
- Second version: offset issue resolved, spread of glue flow restricted
- Exercises: Wire bonding exercises and encapsulation





Test Setup at CERN

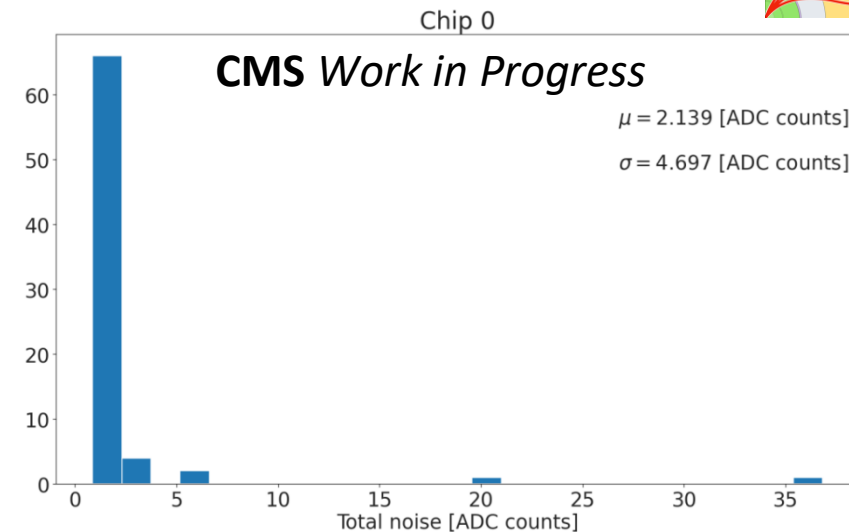
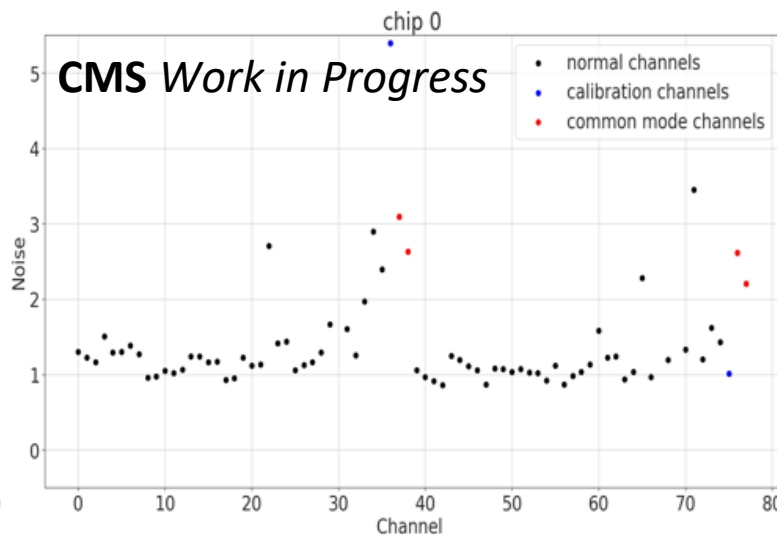
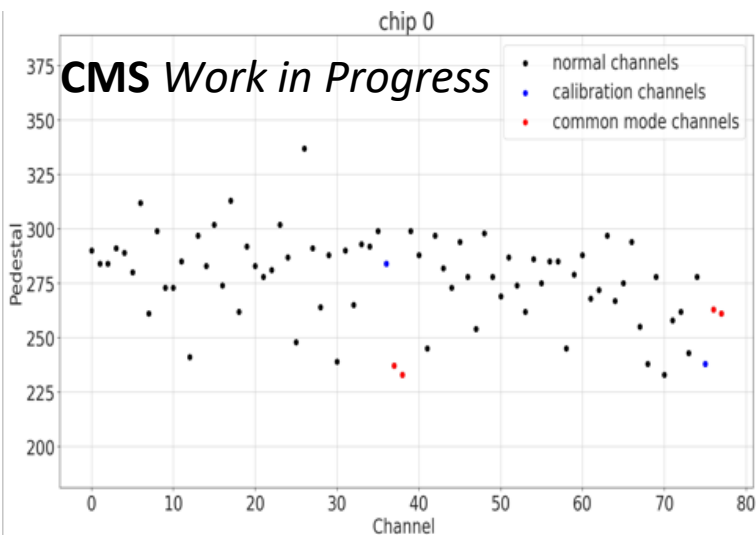


Test system

NSH hexaboard v2

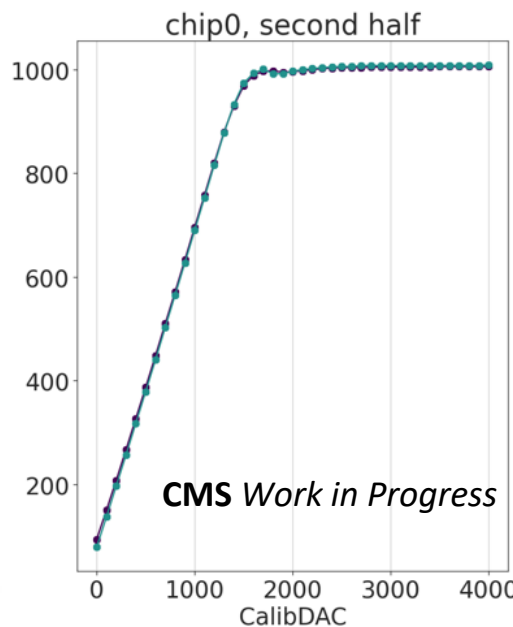
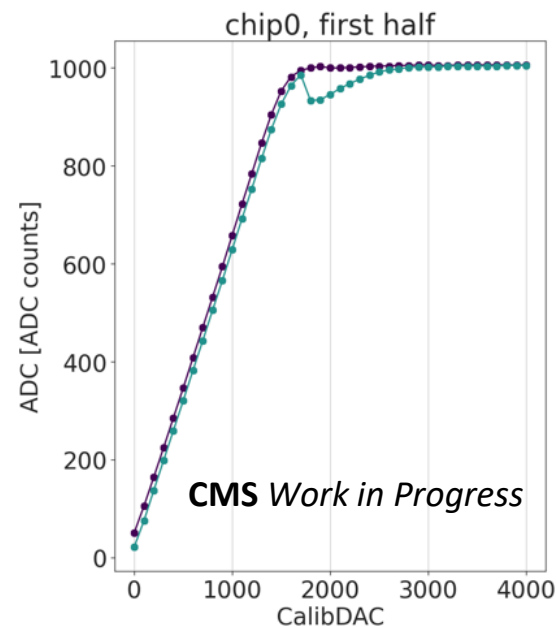
Missing the LDO. Test performed by directly supplying the requisite LV for the analog and digital requirements

- Design Concepts and Challenges
 - Class-3 symmetric stackup, 1.2 mm thick, 8 layers, Multiple micro-vias,
 - Differential track geometries, Tight Impedance levels, ~2400 Backdrills etc.
 - Twist < 0.4% (<0.8 mm over 200 mm)
- Litmus Test for the PCB Industry
- Two PCB companies have been identified
- Some of the NSH hexaboards fabricated and assembled in India (Flatness within Tolerance) were shipped to CERN for testing
 - It successfully went through all the electrical tests and it's performance was at par with other boards
- In process of setting up hexaboard testing station at TIFR



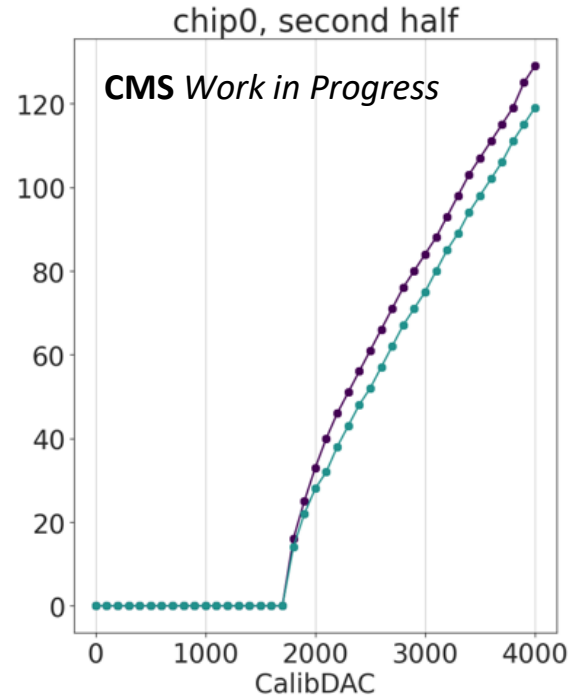
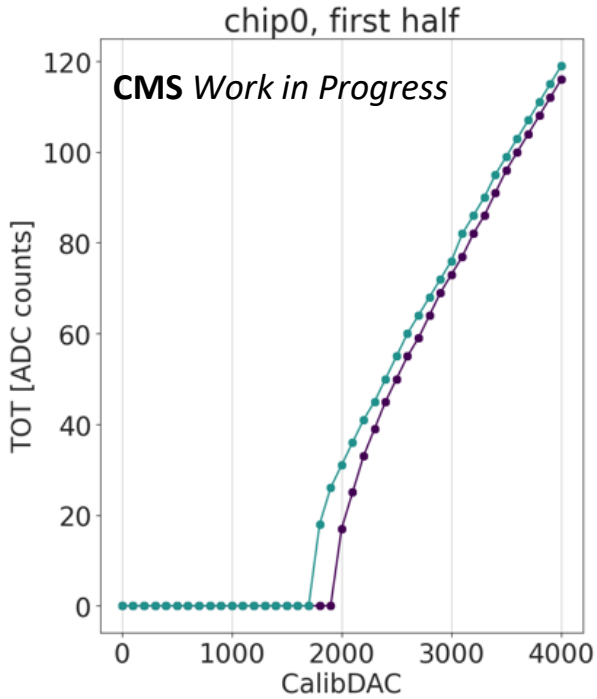
Pedestal and noise, Chip 0: Total noise around 1 ADC count

- NSH hexaboard was tested using the test system
- Pedestal run, including a scan to optimize the pedestal value to enhance the dynamic range, Charge injection (For all 3 chips)
- Results are as expected lines

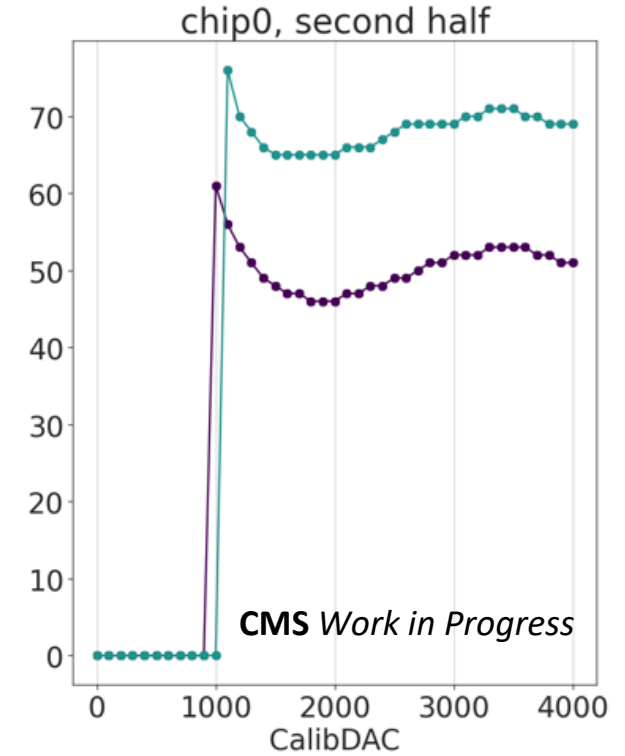
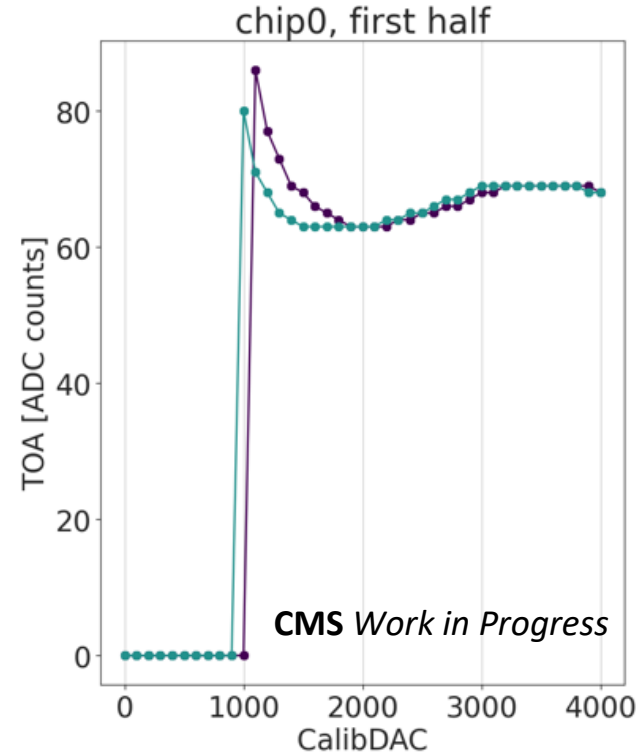


ADC vs charge injection, Chip 0: Two channels are plotted.

Bench test of NSH V2 Hexaboard



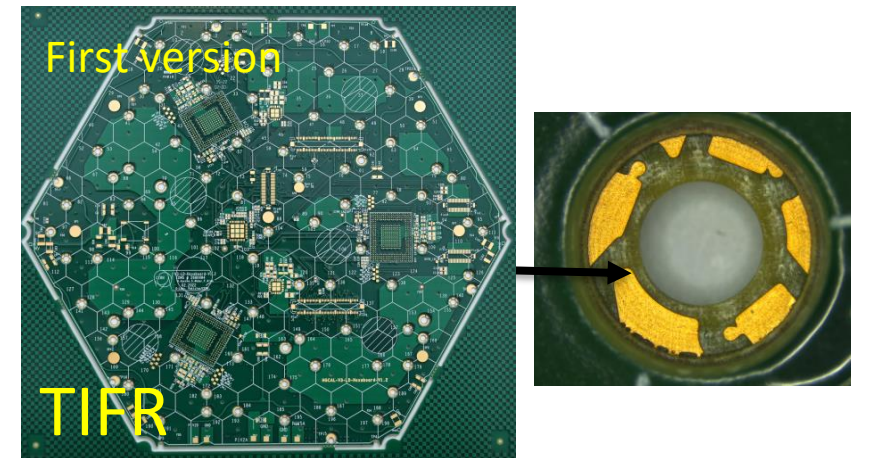
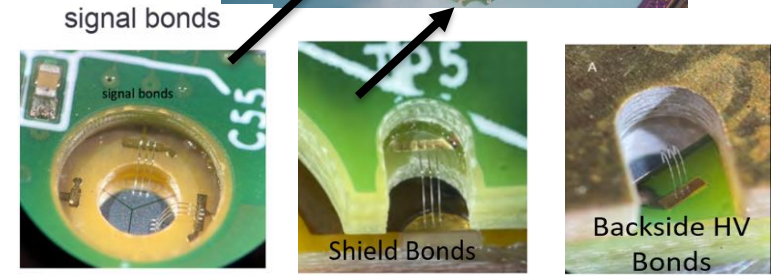
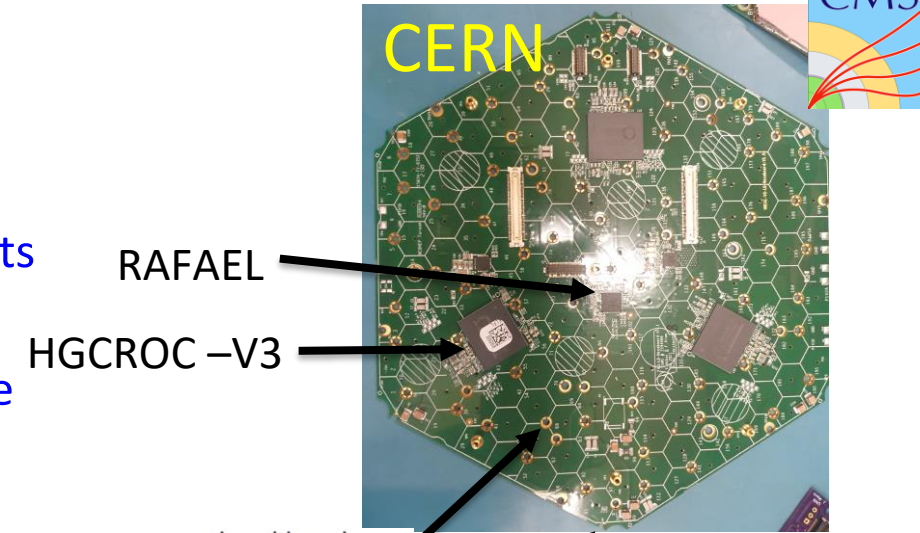
ToT vs charge injection, Chip 0: Two channels are plotted.



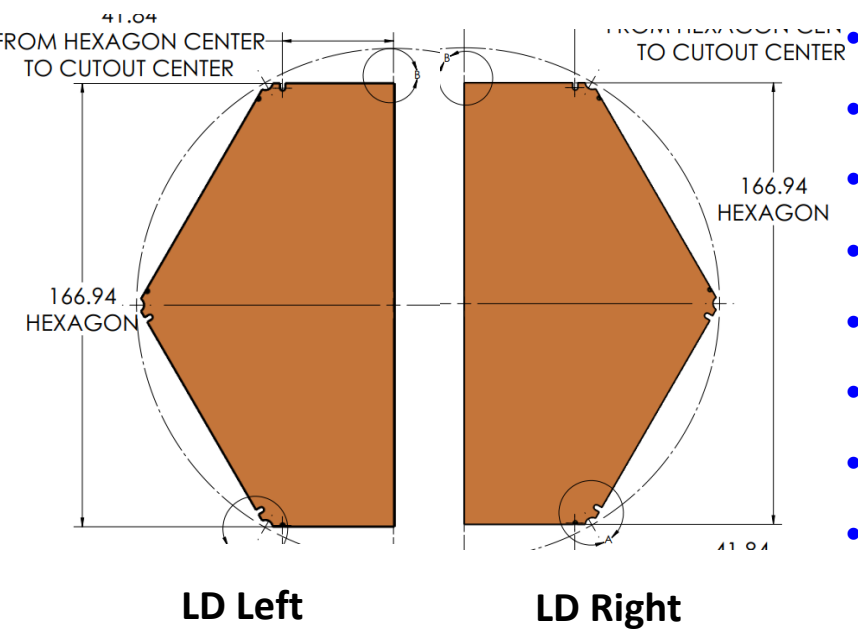
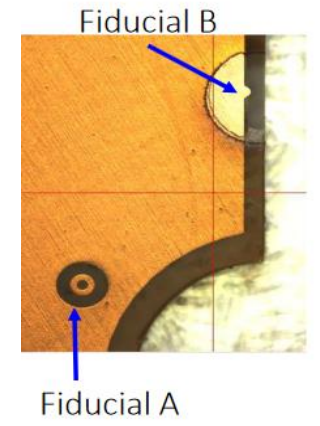
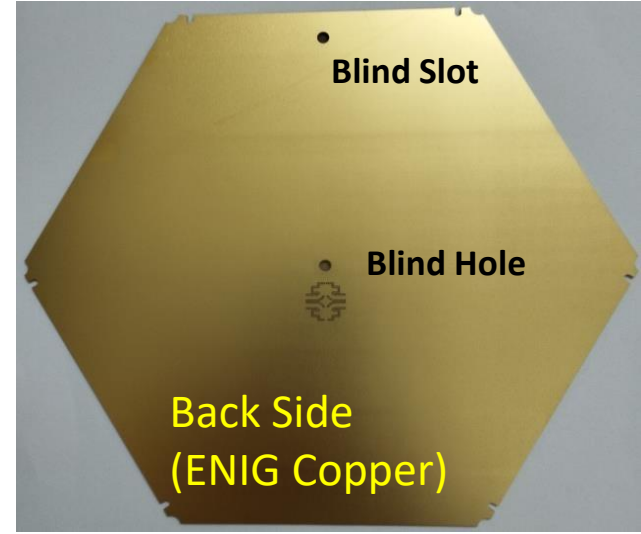
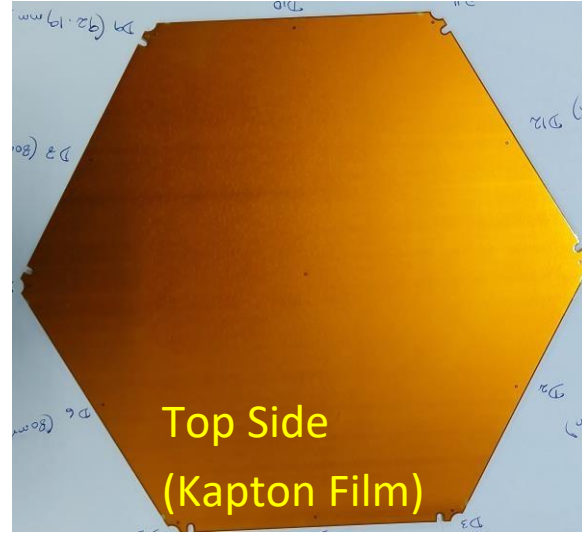
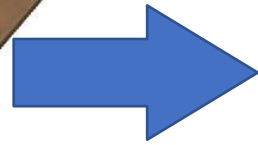
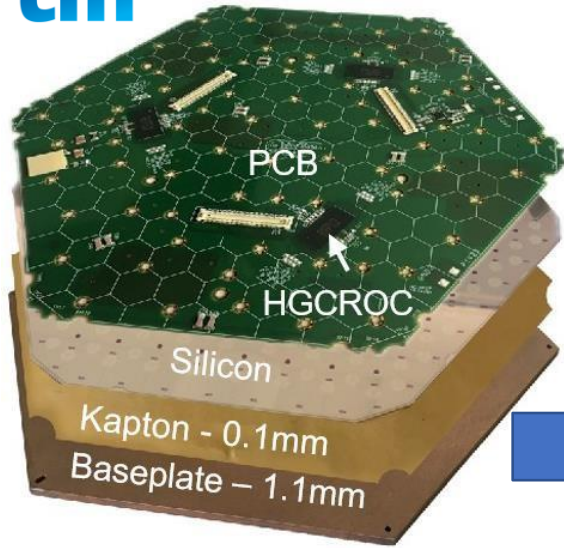
ToA vs charge injection, Chip 0: Two channels are plotted.

Hexaboard PCB: V3_LD_V1.2

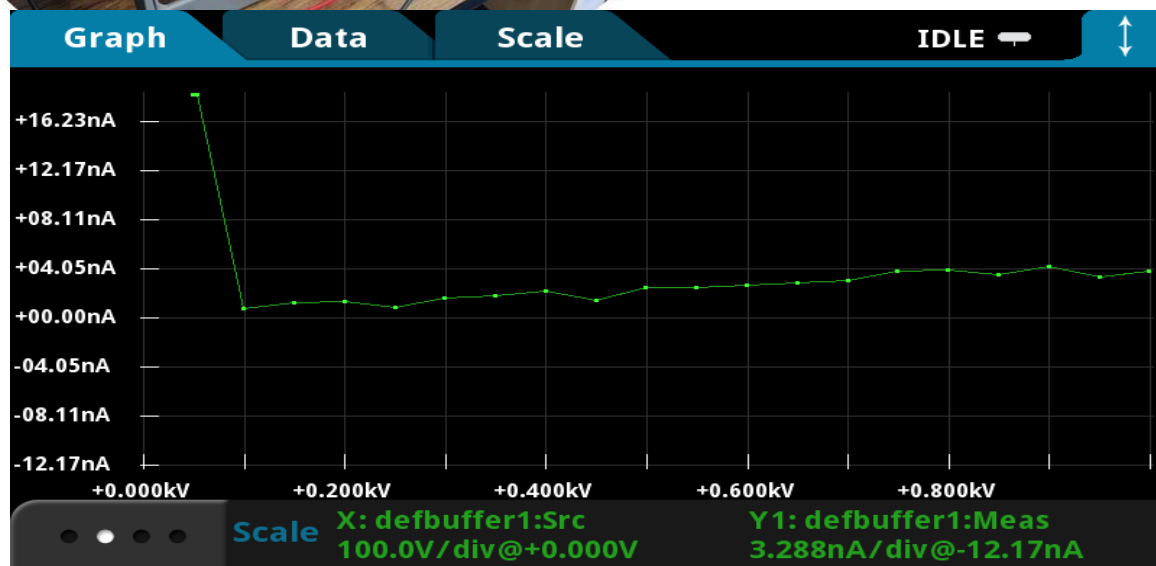
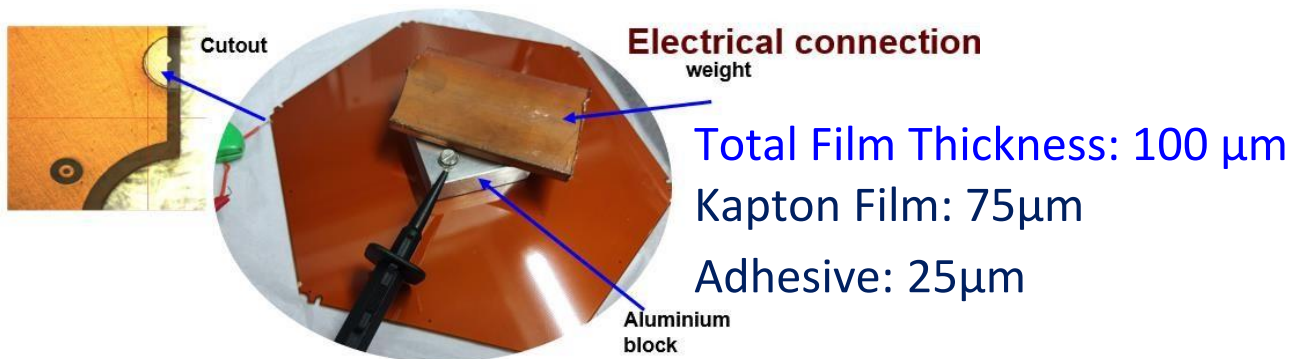
- 3(6) HGCROCs per Low Density (LD) (HD – High Density) hexaboard, inputs from Si sensor cells via wirebonds through stepped holes in the PCB
- RAFAEL ASIC to distribute control and precision clock signals, bias voltage for sensor brought in via backside wirebonds
- Similar stackup as NSH Hexaboard, But:
 - Includes the stepped holes (counterbore) geometry! (Tricky and challenging)
 - LD-packaged HGCROC-V3 design
 - Concept of making sandwich of two PCBs
 - R&D efforts with two leading Indian PCB companies ongoing
 - PCB stackup was suitably optimized after several iterations with fabricator
 - First version from Indian company delivered. Noted initial lapses in fabrication due to improper selection of the bonding material resulting in alignment offset, laser marks, glue seepage while making the sandwich
 - Awaiting few samples of next version from both the companies



PCB Baseplates (Full and Partial)

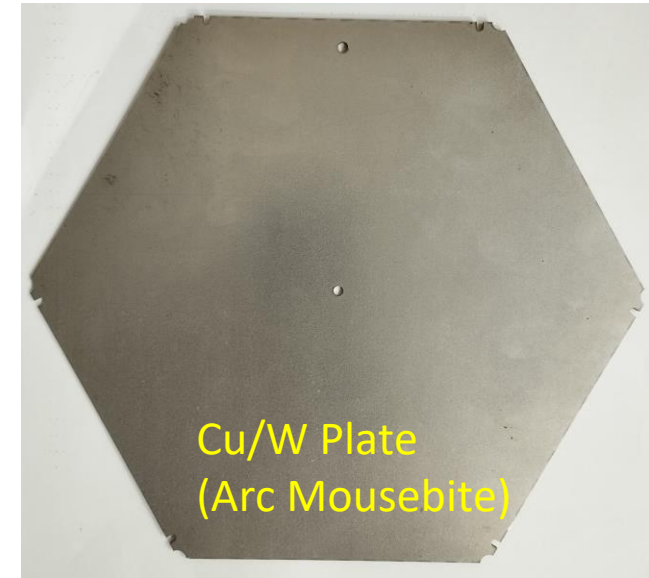


- First two components of Si Module (Baseplate(PCB) + Kapton Film) (1.2mm Thick)
- Full and Partial Modules with PCB Baseplates: Low Rad. of CE-E and CE-H
- Mounting platform for the Si sensor and Frond End PCB (Hexaboard) on Cassettes
- Blind Hole and Blind Slot features to mount on the Cassettes. Tight Tolerances.
- Kapton film for bias supply to sensor backplane and insulation
- Three types of Fiducials (Total 19) on Top to align and mount Sensor + PCB
- Working with vendors on fabrication for pre-series production (Few Hundreds)
- Our R&D efforts with these two PCB Industry leaders could register them to take participate in the Global Survey of HDI PCB fabrication (Frontend + Backend) for HGCAL



- One of the cutout was soldered with a wire to make connection to one side of the Kapton layer
- An Aluminum block was used to make connection on the other side of the Kapton layer.
- The weight on the aluminum block make sure a good connection between Aluminum and the Kapton layer
- Upper surface of the Aluminum is connected to the ground.
- Current readings were noted with Voltage variation from 50V to 1000V in steps of 50V
- Maximum leakage current noted was ~4 nA

- Provides Rigidity to Si Module, contributes to absorber material
- Costly material, contacted many local vendors for the procurement
- Procured few raw sheets of (200mm x 200mm)
- Good Flatness. Observed density (13.9 – 15 gm/cm³) variation ~7%
- Successfully established the process of Hexagonal profile cutting through wire EDM machine for single and stacked plates at TIFR
- QC measurements: All the dimensions measurements within $\pm 50\mu\text{m}$
- Identified a local industry and visited the factory for mass production of Cu/W sheets in India. Discussions and R&D are in progress.
- Latest design has flat mousebites with three layer shield for sensor isolation and supply biasing
- Fabrication in progress with three layer shield



- 60 full PCB Baseplates provided to one of the MACs and concerned group (Pre-series Production)
- Fabrication of another full PCB Baseplates (60 Nos.) in fabrication (Pre-series Production)
- Partial PCB Baseplates: LD left (20 Nos.) + LD Right (20 Nos.) will go in production soon
- 18 Cu/W Baseplates with three layer shields in production
- Awaiting next version of V3 stepped hole bare Hexaboard PCBs (To be assembled subsequently in Indian Companies)
- Look out for two posters on Quality Control (Mukund Shelake), QC Database Management (Prashant Shingade) of Baseplates and Talk on Development of Muon Tomography for the validation of HGICAL (Pruthvi Suryadevara)

- Status and Overview of the CMS HGICAL in CALOR by Zoltan Greece (Fermilab) on May 19, 2022

<https://indico.cern.ch/event/847884/contributions/4852514/attachments/2447638/4194247/2022Sep19CALOR2022ZoltanGecse.pdf>

- Performance of the CMS HGICAL for LHC Phase 2 by Andre David in ICHEP 2022

<https://agenda.infn.it/event/28874/contributions/169080/attachments/93797/128133/20220707%20ICHEP%20HGICAL%20performance.pdf>

- CMS High Granularity Calorimeter in EIC Calorimetry Workshop by Chia Ming Kuo on March 15, 2021

<https://indico.phy.ornl.gov/event/38/timetable/?view=standard>

Thank You