Position measurement in RPCs using timing difference at both ends of strips

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Contents

- 1. Resistive Plate Chambers (RPC)
- 2. Alternate Readout Concept
- 3. Experiment design
 - Source
 - Detector electronics
- 4. Measuring time with oscilloscope
- 5. FPGA based TDC
- 6. Frontend preamp design
- 7. Setup and Early Results
- 8. Future Works

References

1. Resistive Plate Chamber



RPC model (not to scale)





2mx2m fully assembled RPC at mini ICAL

- Gas mixture used: 95.2% R134a, 4.5% isobutane, 0.3%SF6
- Position resolution: ~6mm
- Timing resolution: ~0.6ns



2.1 Alternate Readout Concept



Traditional RPC readout



Proposed alternate RPC readout

 Traditional RPC readout scheme has two pickup panels with conducting strips, with the pickup panels kept orthogonal so that one gives the X-coordinate and the other gives the Ycoordinate.

 This work proposes an alternate readout system, where we have top and bottom strips kept aligned in one direction (let's say X). Readout electronics (differential) is kept at both the ends of the strip. From the difference in time of arrival (TOA) at both ends of the strip the position along the strip is reconstructed. The uncertainty in the development of avalanche will be cancelled out when taking the difference in TOA.

 Advantages: lower electronic noise (both due to differential readout as well as due to return current flowing symmetrically) better timing and position resolution, similar costs, (slightly) less dead space.

2.2 Existing work

	Contents lists available at SciVerse ScienceDirect Nuclear Instruments and Methods in Physics Research A	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
ELSEVIER	journal homepage: www.elsevier.com/locate/nima	
MRPC-PET: A position meas	new technique for high precision time and urements	
MRPC-PET: A position meas K. Doroud ^{a.*} , D. H	new technique for high precision time and urements atzifotiadou ^b , S. Li ^a , M.C.S. Williams ^b , A. Zichichi ^{c.d} , R. Zuyeuski ^a	

Improved-RPC for the CMS muon system upgrade for the		
HL-LHC	\mathbb{N}	
P. Kumari $l,1$ K.S. Lee ^s A. Gelmi ⁿ K. Shchablo ^j A. Samalan ^a M. Tytgat ^a N. Zaganidis ^a	\subset	
G.A. Alves, ^b F. Marujo, ^b F. Torres Da Silva De Araujo, ^c E.M. Da Costa, ^c D. De Jesus Damiao, ^c H. Nogima, ^c A. Santoro, ^c S. Fonseca De Souza, ^c A. Aleksandrov, ^d R. Hadjiiska, ^d P. laydjiev, ^d	[3]	

Double-end Readout Method Applied in RPC	
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	\sim
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[2] K Doroud et al, 2011. In multigap RPCs (MRPC): Results: 104ps/cm, 18.3ps (1.7mm)

Caveat: the rise time of signals in MRPC is intrinsically smaller, this is due to the electric field set. So in RPCs we may not get as good results.

[3] In CMS iRPC , 2020: Results: ~100ps/cm, ~160 ps (16mm)

[4] Q. Li et al, 2021:

Results: ~93ps/cm, 11 mm

[5] Yuexin Ding et al, RPC 2022: Reflection readout method

Results~93ps/cm ~5mm

 This work: Combine the benefits of differential readout and fast timing measurements

3.1 Experiment Design - Source

Muon Telescope

Accurate to ~2mm

Monte Carlo Aperture Simulation

• The measured distribution will be convolution of the aperture and the time difference distribution.









100

200

300

3.2 Experiment Design – Readout Electronics

Testing two different setups:

- 1. preamp-discriminator+TDC
- 2. Preamp+Oscilloscope/Digitizer

Expected sensitivity (i.e. 2/propagation_speed) is ~100ps/cm.

Expected performance:

- Preamp-discriminator (NINO: 15s jitter) + PICOTDC (7ps) / FPGA TDC (15ps) / HPTDC (35ps): 2.2mm-5mm
- Preamp (<10ps)+ oscilloscope(5-50ps depending on SNR): 1.5mm to 6mm.



Setup 1: preamp-discriminator + TDC



Setup 2: preamp + oscilloscope/digitizer

4. Time Measurement with Oscilloscope

Q – How precisely can we measure time differences with an oscilloscope?

We used Lecroy WavePro 725Zi oscilloscope:

- bandwidth of 2.5 GHz
- Maximum sampling rate of 40GSa/s (i.e. samples spaced 25ps apart)







Measurement setup: Timing resolution of oscilloscope

	Measured σ_t
No attenuation	3.5ps
1/10	~60ps
1/100	~100ps

5. FPGA TDC

 \odot FPGA TDCs have become a viable alternative to TDC ASICs

 \odot Cost, integrable into the FPGA DAQ

 Basic idea behind an FPGA TDC is to use inherent propagation delay of an electronic gate as the scale or clock period.

• Present day FPGAs have fast gates (~10ps) built in for computing carry logic.

• A simple architecture called "delay line TDC" conveys this idea.



5.1 Vernier FPGA TDC

Vernier FPGA TDC is another architecture, which uses two oscillators running with slightly different time period. The concept of vernier scale is used here, and the resolution is equal to the difference in the time periods.



Vernier TDC – block diagram





• We have implemented oscillators at different locations in ZYNQ7000, with two oscillators having time period difference of 17ps.

Basic ring oscillator

6. Frontend Electronics (Analog Preamp)

in THS4303.

Requirements

- Differential input impedance:
- Bandwidth: 350MHz assuming 1ns rise time signals

• SNR?



Circuit diagram (in LTSpice for simulation)



Board layout – 4 layer impedance controlled, power planes



3D view – front side (to be soldered to strips)



3D view – back side (supply and output connectors)

7. Setup and Results



At the position 25cm from one end of strips

The black paddles are scintillators which are connected to SiPMs. (The vertical paddle on the left is kept only for support)



At the one of strips



Connections soldered from strips to the frontend board.

7.1 Propagation speed measurement with RPC off



 Before turning the RPC high voltage on, signals were conductively coupled into second strip from the edge of the RPC at different locations along the strip. Sensitivity: 98ps/cm excluding the points at the edges.

• The signal is clearly riding on top of noise. The reflected signals are also seen, indicating that the termination on the frontend board (44ohms) is not matching the pickup panel transmission line.

7.2 Early Results...



• The aperture varies at different location – this effect is clearly seen in the symmetric distribution (484ps) at the centre and asymmetric distribution (with σ = 272ps) at -35cm for example.

The correction for the aperture has not been done yet, so no constraint yet set for the position resolution.
The sensitivity (2/propagation speed) except at the ends is 97ps/cm.

8. Future works

• Software noise removal.

- Faraday caging.
- $\ensuremath{\circ}$ Impedance matching.
- Front end preamp redesign: higher gain, lower noise, better connectors to the strips.
- Front end discriminator (NINO) redesign, experiment setup with discriminator + TDC.
- Calibration: The propagation speed may vary slightly along the strip. The propagation speed and resolution is expected to be dependent on the temperature also.

References

[1] J.M. John et al, 2022. *Improving Time and Position Resolution of RPC detectors using Time Over Threshold Information*. *JINST* **17** P04020

[2] K. Doroud et al, 2011. *MRPC-PET: A new technique for high precision time and position measurements*. Nuclear Instruments and Methods in Physics Research A, Volume 660, Issue 1, p. 73-76.

[3] P. Kumari et al, 2020 *Improved-RPC for the CMS muon system upgrade for the HL-LHC,* 2020 *JINST* **15** C11012

[4] Q. Li et al, Double-end Readout Method in RPC, JINST 16 P10036

[5] Y. Ding et al, *Reflection readout method*, RPC 2022

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Thank you 😳



FPGA_TDC_10Oct2022_i



Add on slides – Schematic Entry of the Frontend Board



Add on slides – Setup full view

Big reduction in noise if care is taken with the signal return

The signal is induced on the anode and cathode pickup pads - current flows from anode pad through amplifier and returns to cathode pad. The strip design allows the use of a transmission line (twisted pair cable) to connect this 'signal generator' to the amplifier - otherwise return path is via the outside grounding box (therefore sensitive to all the noise in the ground). In reality this is a key ingredient to substantially reducing the noise and improving the time resolution

If you want to get better than 50 ps time resolution – must use differential readout – must have access to anode and cathode readout pads

Add on slides – slide copied from Crispin Williams "the mrpc, a detector for excellent timing resolution", 2010/15



Add on slides – NINO Board rev0