



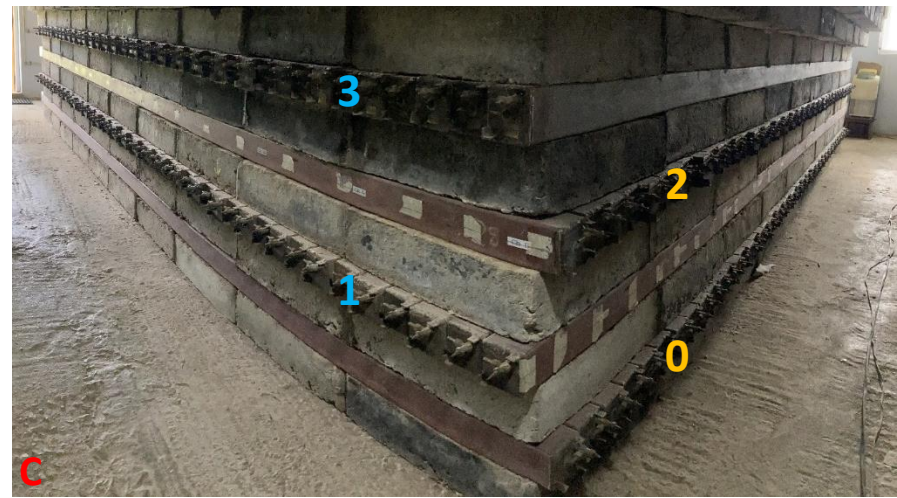
Trigger-less Muon Data Acquisition (TM-DAQ) system for the GRAPES-3 muon telescope

R SURESH KUMAR

On Behalf of GRAPES-3 Collaboration

CRL, TIFR, Ooty

The GRAPES-3 EXPERIMENT

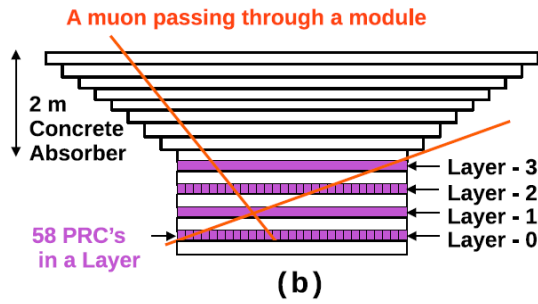
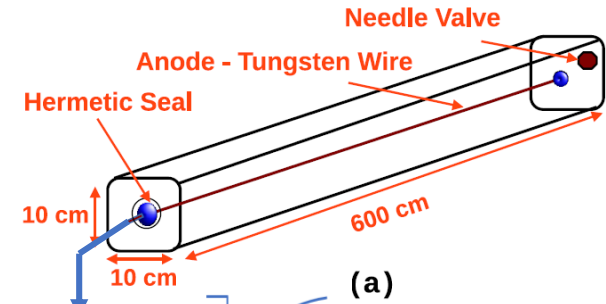




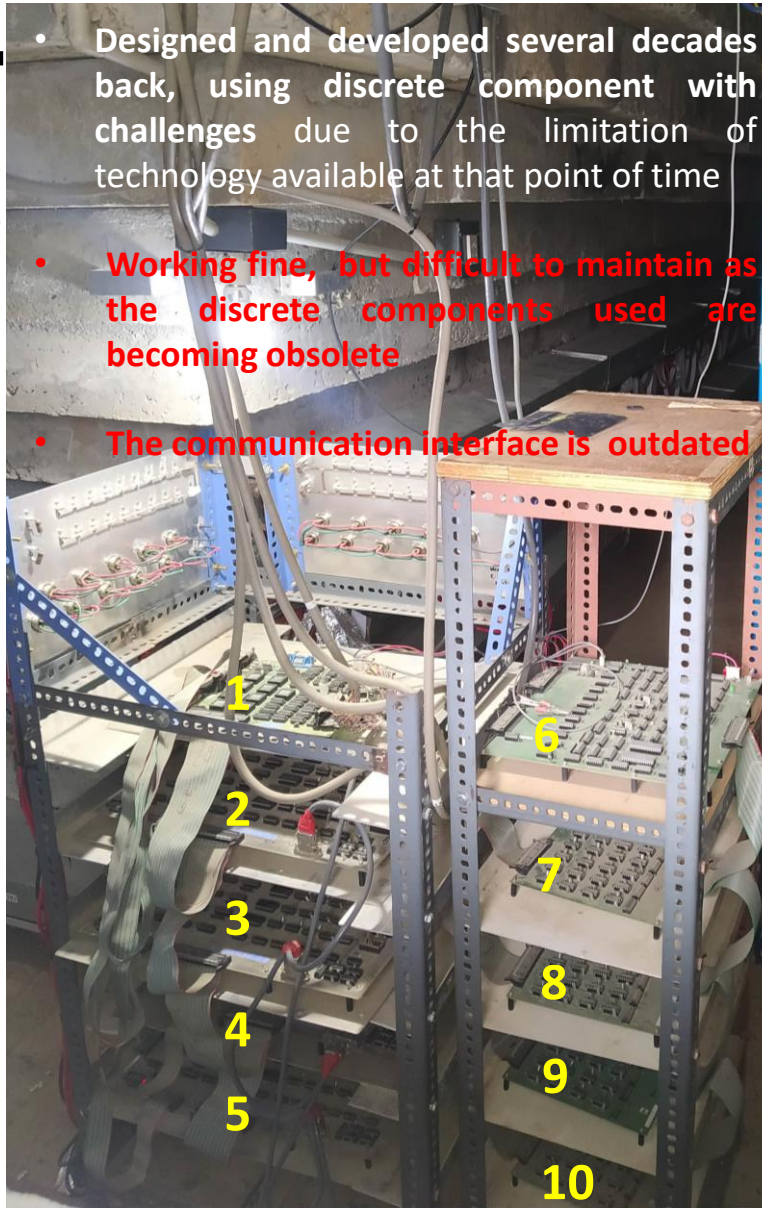
Existing Conventional DAQ for Muon Detector

Proportional Counter (PRC)

Muon Module



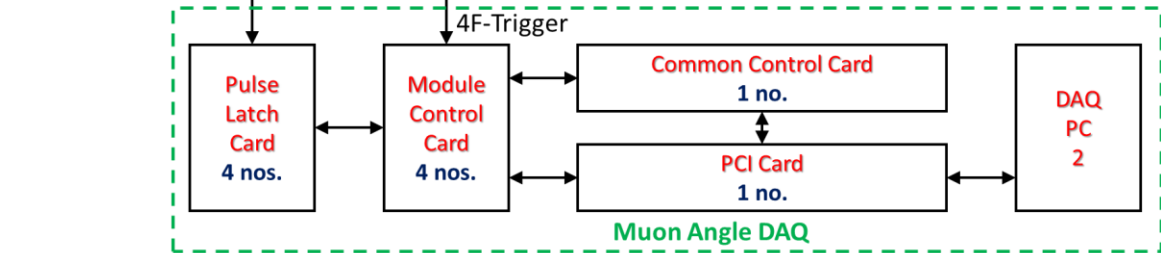
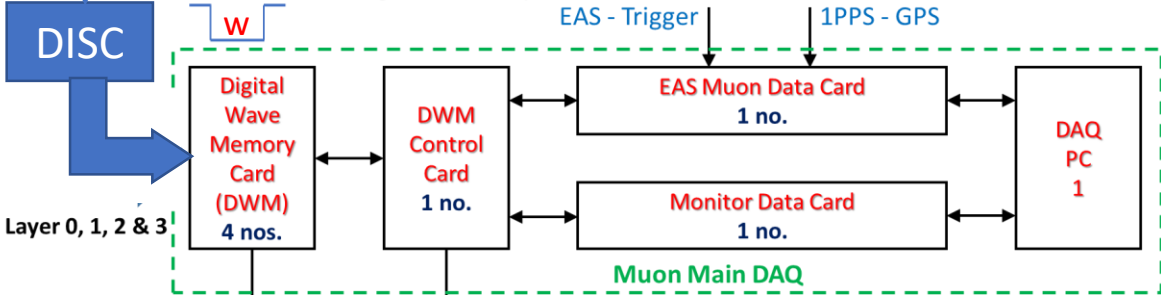
- Designed and developed several decades back, using discrete component with challenges due to the limitation of technology available at that point of time
- Working fine, but difficult to maintain as the discrete components used are becoming obsolete
- The communication interface is outdated



Challenges in Existing DAQ

- Two DAQ streams: Mu-Main and Mu-Angle
- Mu-Main: Width and Time of each PRC w.r.t. Air shower trigger
- Mu-Angle: 4- fold (whenever a Muon passes through all 4 layers of PRC's as show in picture b)
- It uses 10+ large area PCB per modules
- Large Dead time: 12 – 20 %
- Pulse Arrival Time: Not measured
- Pulse Width is measured for 1 channel (1000 sec) at a time in each layer time
- No direct CRM for PRC's
Only 4F and Any3F at every second
Other folds – time multiplexed
- Restricts the measurement of Muon angle up to Up to 45°

Muon Main DAQ records the data w.r.t air shower trigger generated by Scintillation Detector



Muon Angle DAQ records data w.r.t. 4-fold trigger (a Muon passing through all 4 layers of PRCs)



Triggerless Muon DAQ Concepts and Physics Horizon

- **Trigger less Muon Data**

- Records the arrival time and the pulse width for each and every hit from the proportional counter
- Record the hit rate of PRC, various triggers, temperature etc.
 - Pulse Width measurement is done with a resolution of 10 nano-second
 - Absolute pulse arrival time is measured with a resolution of 10 nano-second

- **Physics dependent reconstruction of raw data can be done in offline mode**

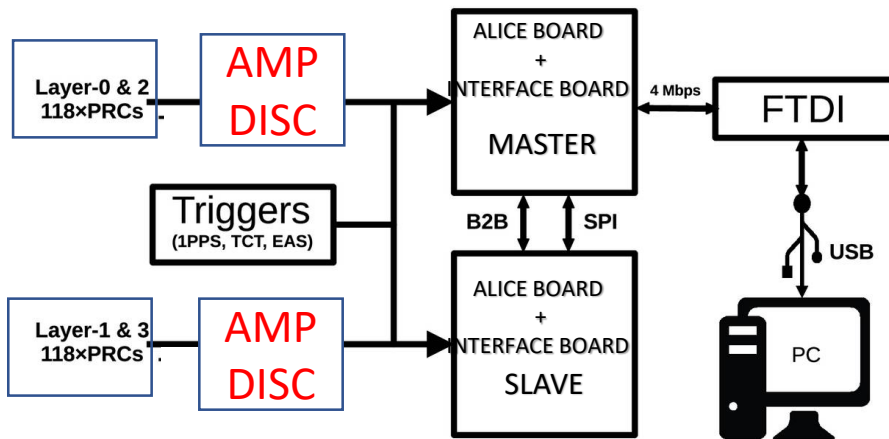
- Rigidity dependent study of Moon Shadow
- Transient Phenomenon
 - Thunderstorm Physics
 - Solar Physics
- Air Shower Physics
 - Air showers at large zenith angles, muon rich showers
- New Physics (This enables users to do Physics beyond standard model)
 - Search for tachyons, low beta particles (monopoles, WIMP etc.), serendipitous searches



Architecture of TM-DAQ System

- System requirement
 - A device with adequate I/O's to process all the PRC channel in parallel, better timing resolution, excellent signal processing capability and memory
- Solution: FPGA based embedded systems
- Received large number of ALICE Boards (~150 number) from ALCIE Collaboration as gratis
- Designed interface card to access the FPGA I/O's

Due to the limitation of I/O's, 2 No's Alice Board + interface Board combination is used to process 1 module



ALICE Board

Tyco Connectors

FPGA Chip

DDR Memories

Xilinx Virtex-4 FPGA (XC4VLX40)
 Clocks: 100 MHz & 50 MHz
 DDR SDRAM (EDD2516A)- 4 Physical chips Each with 32MB
 Tyco connector - 158 Usable I/O Pins
 Board Size : 17.4 X 10.6 CM

Interface Board

Communication Section

Designed by GRAPES Team

Tyco connector for ALICE Board

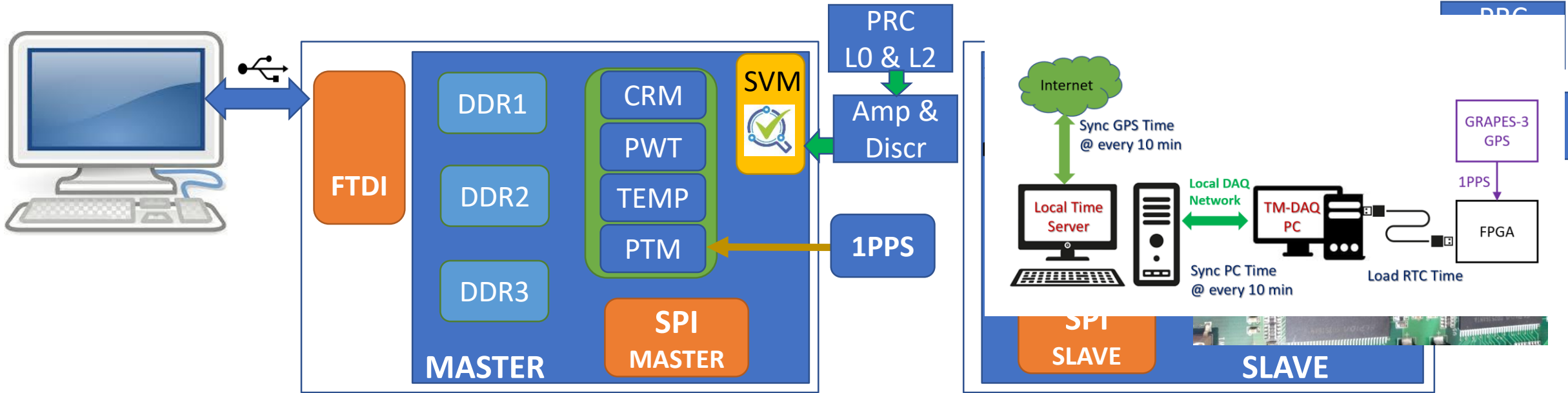
Power Section

PRC inputs

Designed interface card to access the FPGA I/O's

- Level translator section
- Power section (to the ALICE board)
- Communication section
- Size 36 X 34 Cm

FIRMWARE MODULES FOR TM-DAQ



Specialized Firmware Modules for Front Module

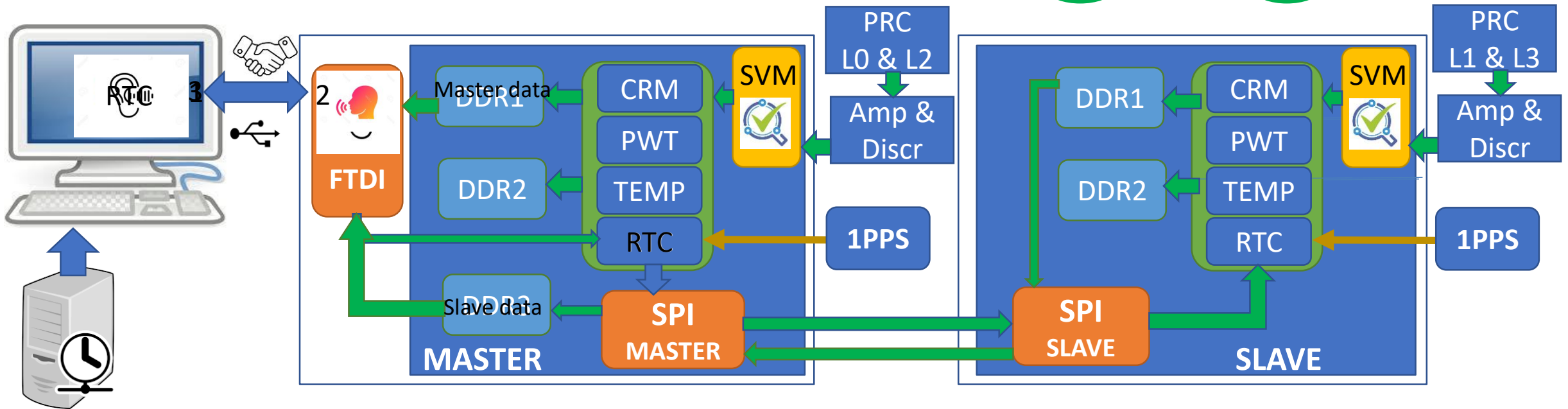
Since the ALICE card has only 158 accessible I/O's, we need to have 2 Alice boards to process one module. So we should have proper inter-board communication for which we have 8m long flat ribbon cable, which is susceptible to differential mode noise. To overcome this, we use differential signaling between crystals and oscillators.

1. SPI communication Module for Master and slave
2. DAQ Controller for 6Pb DDR (DDR BMM of Master) Digital Pulsed Accuracy 0.5% / Res. Resolution 0.0625°C
 - So the pulses are validated by checking the minimum pulse width
 - Real Time Clock (RTC) / Time Synchronization / Clock Counter / Time Calibration Trigger (TCT)
 - Complete time information ranging from year to nanosecond is managed inside FPGA by using smart algorithms
 - The temperature and the Counting rates of crystals are recorded as part of data
 - GPS synchronization ensures the accuracy of time
 - All raw data is recorded and any correction (e.g. w.r.t. temperature) can be done offline during analysis



TM-DAQ

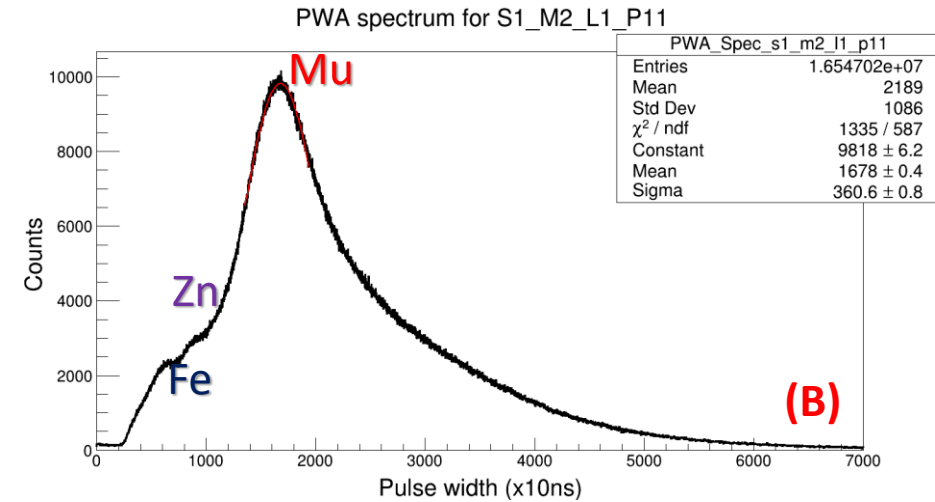
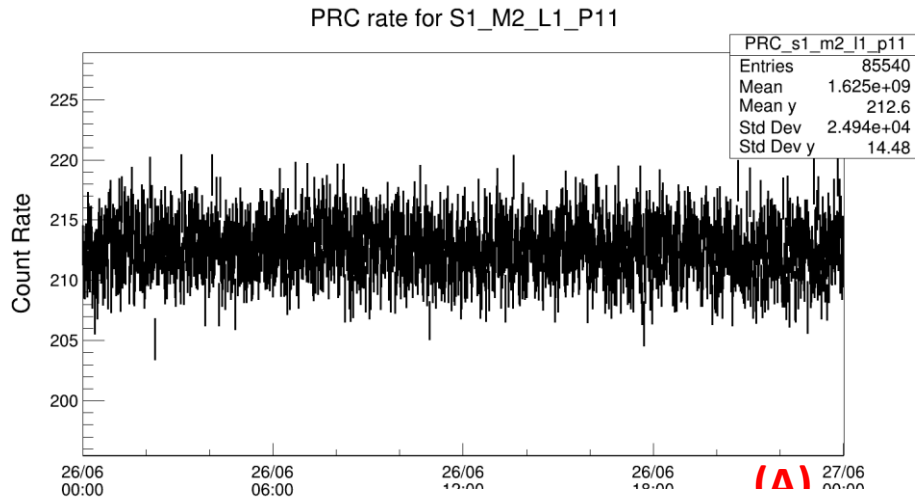
| | USB Protocol | SPI Protocol |
|--|---|---|
| Hardware Monitoring and Auto reset option | | |
| Max Theoretical Speed | 8 MBytes/Sec | ~1 MBytes/sec |
| <ul style="list-style-type: none"> All the critical signals are continuously monitored in the Master board and Slave board | | |
| Speed in TM-DAQ | The data transfer speed using USB protocol is ~1.5 MBytes/Sec | The data transfer speed using SPI protocol is ~500 KBytes/Sec |
| <ul style="list-style-type: none"> Any abnormality for more than 2 sec will initiate the Auto reset feature Auto reset will reset the DAQ and re-initialize all the parameters | | |
| | 600 KBytes/Sec | 300 KBytes/Sec |
| Data Volume in TM-DAQ | ~60 GBytes/Day/Module | ~30 GBytes/Day/Module |





Observation

- The stability and data quality of TM-DAQ seems to be very good and last several months we have not seen any failures (one module is continuously since 02nd Jan 2022 (~350days) without any break)



Station: 1 Module: 1

Muon Event Display

Topology : 1132

Trig. (HSE) : 110

Date: 2022-12-08

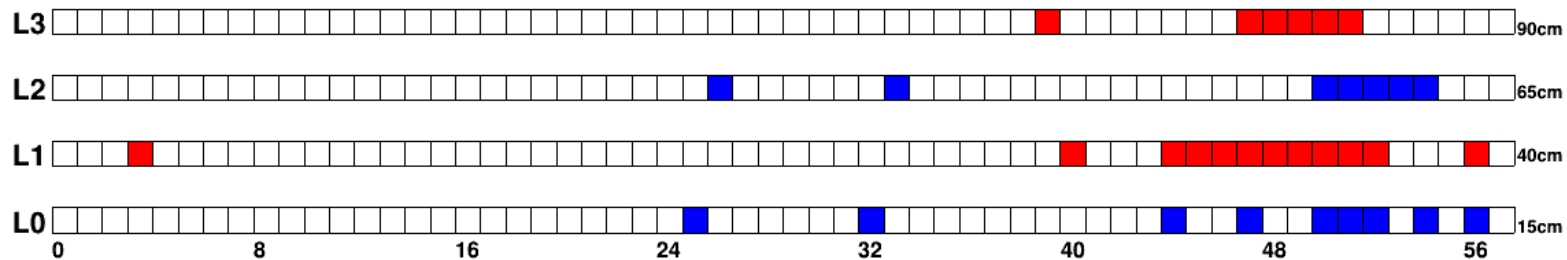
4F_Time: 10:00:15:259:858

EAS_Time: N/A

Event: 826

No. of Hits: 34

(C)



□ Good PRC

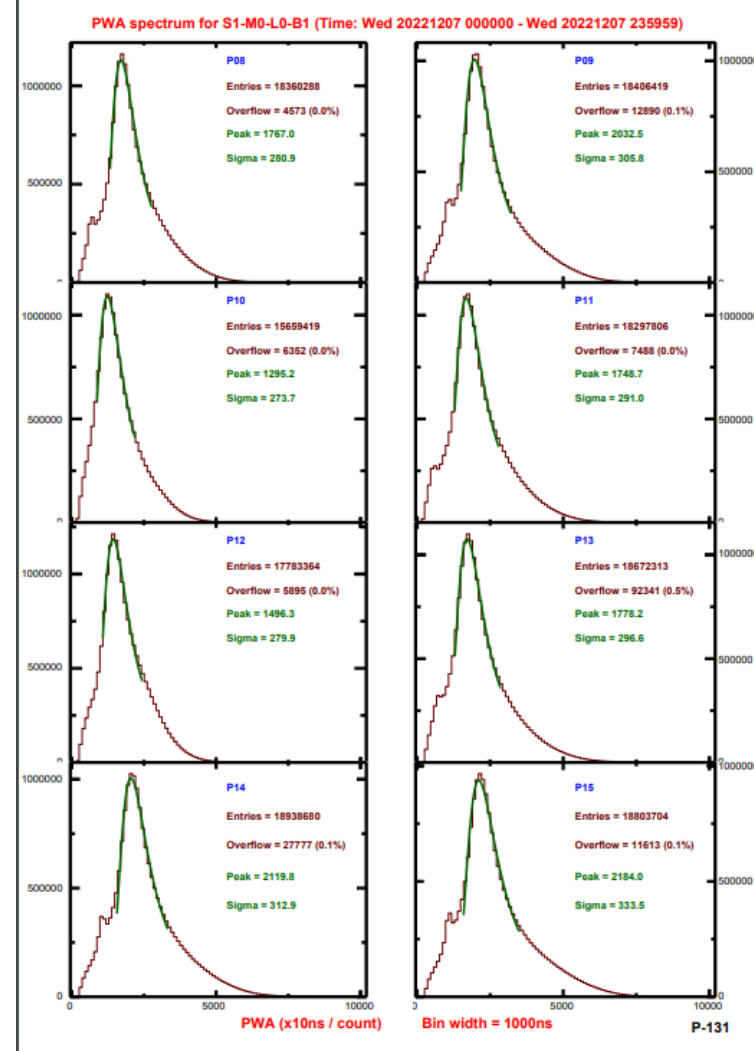
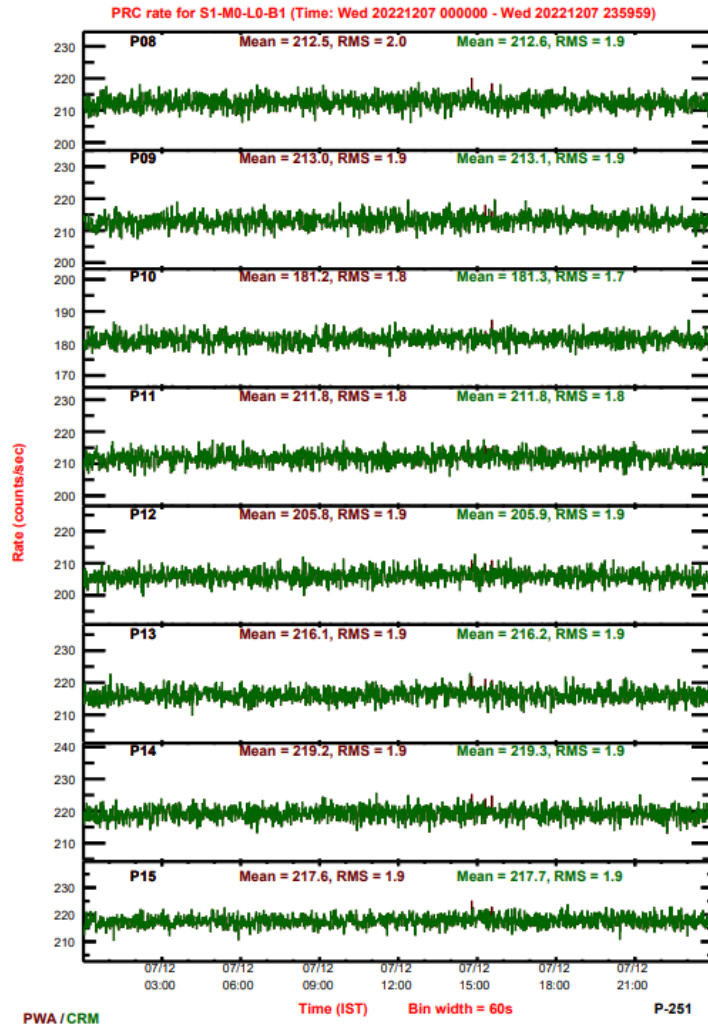
⊗ Dead PRC

■ PRC Hit - Even Layer

■ PRC Hit - Odd Layer

H : H/W Trig. S : S/W Trig. E : EAS Match

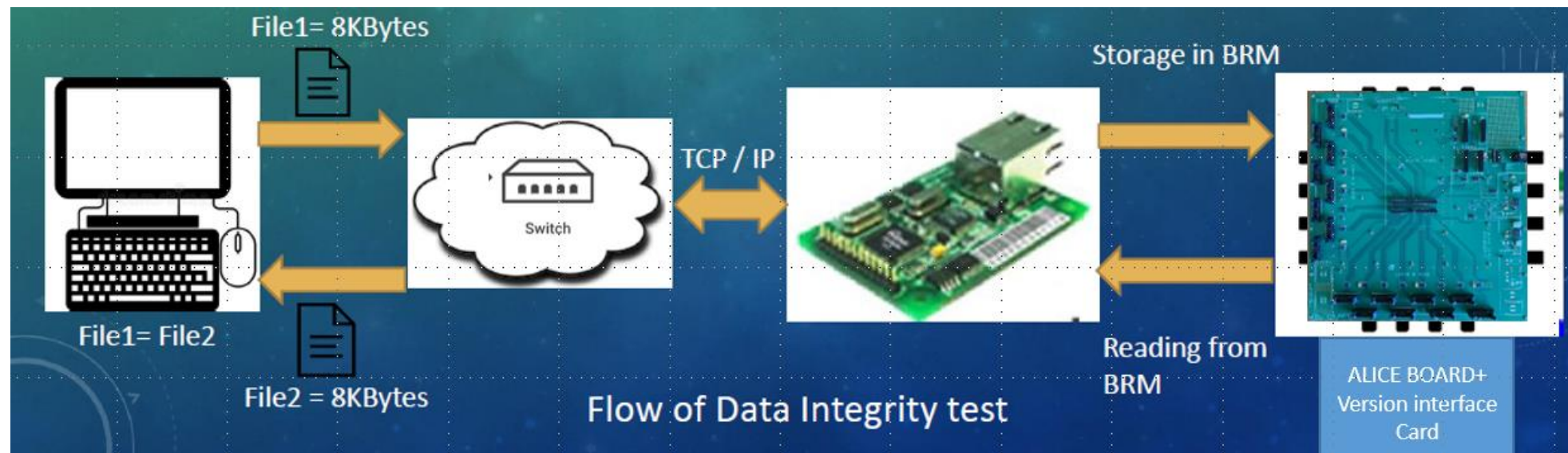
Daily Monitoring Plots





Ethernet Communication for TM-DAQ (Presently working on)

- The TM-DAQ in present version uses USB protocol for data recording ,Since we are using USB protocol for data recording, the Data taking PC has to be in close vicinity of the module thus we require one data taking PC per module.
- To avoid having one computer for each module, We are working on Ethernet protocol using WIZNET chip for transferring the data from the DAQ to the data taking computer.
 - ❖ Data integrity test completed
 - ❖ Bandwidth test completed (Speed = $\sim 5\text{Mbytes/sec}$)





Summary

- Installation completed in 8 Muon modules with USB communication (50% of the existing Muon modules)
- Ethernet testing is in advanced stage and expected to complete in Jan 2023
- Daily data quality monitoring programs are developed and commissioned
- Muon reconstruction algorithm is developed
- For more details <https://g3indico.tifr.res.in/event/858/contributions/2420/>
(Mini Workshop on Triggerless Muon DAQ System for GRAPES-3 Muon Detector-6 Dec 2021)



Thank You!!!