





# AEgIS upgrades and Phase 2 developments

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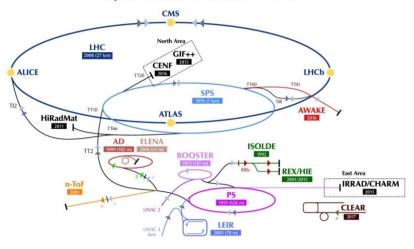


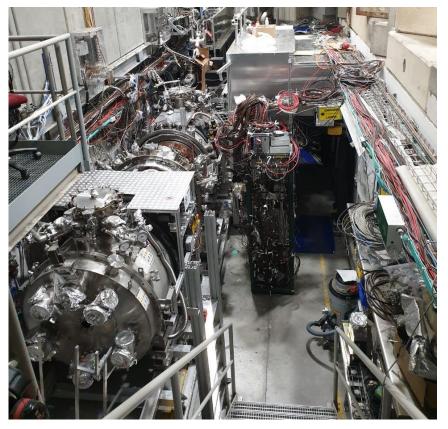


### Introduction to AEgIS

- Antimatter Experiment: gravity, Interferometry, Spectroscopy
- Located at CERN AD complex
- Aim of collaboration is to test Weak Equivalence Principle or the universality of free fall for antimatter containing neutral systems

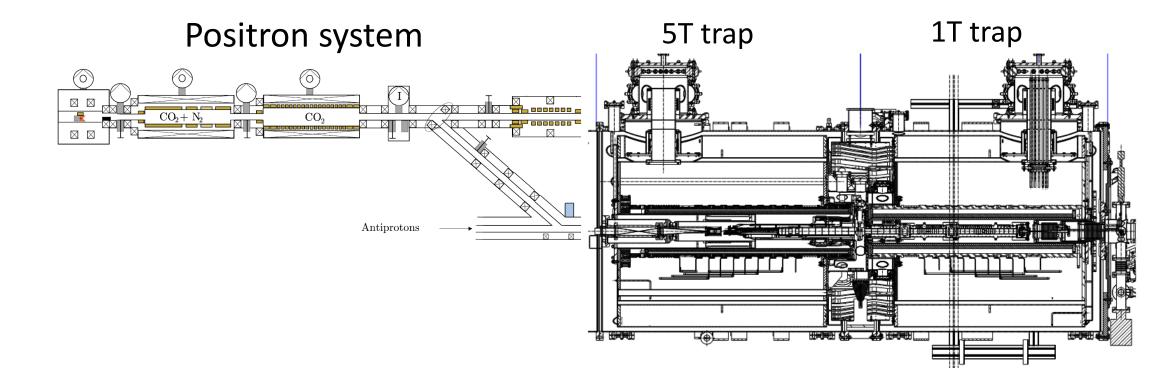
#### The CERN accelerator complex Complexe des accélérateurs du CERN





# The experiment

- Antiprotons are delivered from ELENA (previously from AD), then in AEgIS they are trapped and cooled
- Positrons are produced from <sup>22</sup>Na



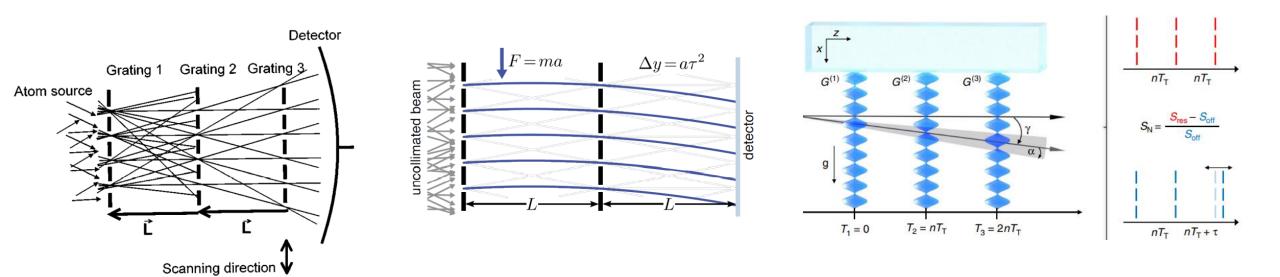
#### Antihydrogen production

- Charge exchange reaction of Rydberg positronium and antiproton
- Allows for pulsed formation

$$\mathrm{Ps}^* + \bar{\mathrm{p}} 
ightarrow \bar{\mathrm{H}}^* + \mathrm{e}^-$$

#### Free fall measurements

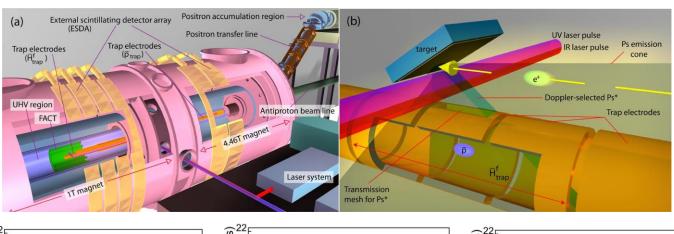
- Moire deflectometer
- Optical Talbot-Lau time domain interferometer

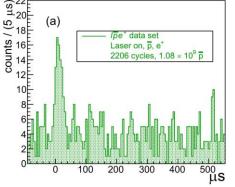


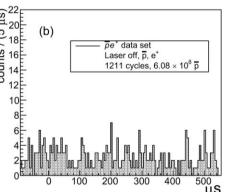
#### Phase 1

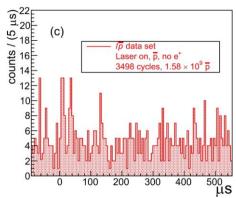
AEgIS Phase 1 was a feasibility study of a pulsed antihydrogen source.
 It ended in 2018 with the formation of cold antihydrogen atoms in the

trap.









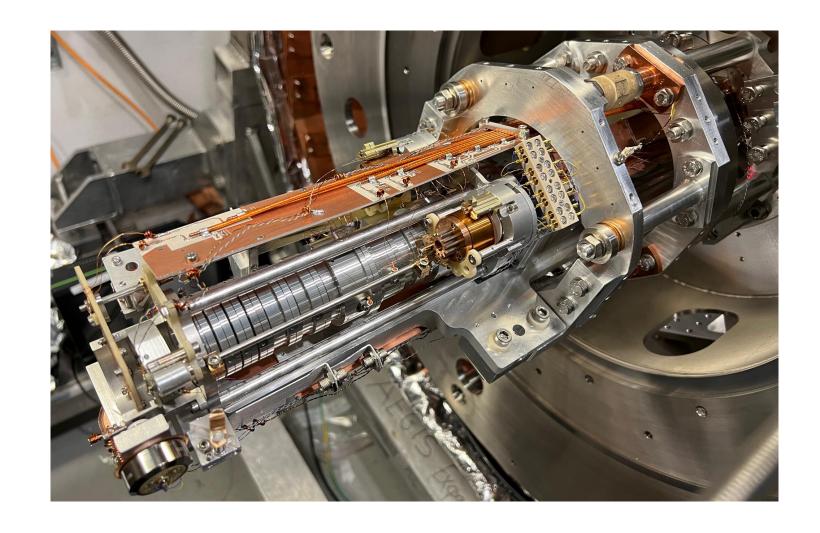
# Timeline

2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	
	LS1			AD Physics			LS2			ELENA Physics			
AEgIS Hbar Phase 1							AEgIS Hbar Phase 2						
	AF							EgIS Ps program					
									AEg	<b>IS</b> <del>p</del> − i	on prog	gram	

# Upgrades

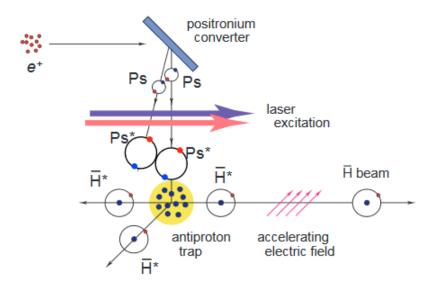
#### New trap

- Longer interaction with positronium
- Better diagnostics
- Positronium target baking during operation

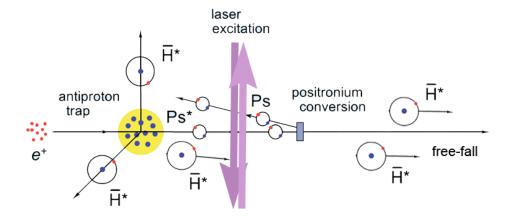


## Antihydrogen production improvement

Used in Phase 1



Used in Phase 2



# ARTIQ/Sinara control system

- Nanosecond precision over extended periods of time
- Based on Python

```
from artiq.experiment import *
from artiq.coredevice.kasli i2c import port mapping
class test_HV_amps_trigger(EnvExperiment):
   def build(self):
        self.setattr device("core")
        self.setattr device("fastino0")
        self.setattr_device("ttl_hvamp1_sw0")
        self.setattr device("ttl0")
        self.setattr device("dio mcx dir switch")
        self.setattr_device("i2c_switch0")
        self.dio_mmcx_i2c_port_1 = port_mapping["EEM0"]
   @kernel
        self.dio_mcx_dir_switch.set(0b00000101)
        self.core.break realtime()
        self.core.break realtime()
   @kernel
   def waitingtrigger(self):
        t gate = self.ttl0.gate rising(200*s)
        t_trig = self.ttl0.timestamp_mu(t_gate)
        if t trig != -1:
            at mu(t trig)
            self.core.break realtime()
            self.fastino0.set dac(8, self.voltage)
   @kernel
        self.ttl hvamp1 sw0.on()
        self.waitingtrigger()
```



#### **TALOS**

- Total Automation of Labview Operation for Science
- Allows 24/7 unsupervised data taking
- Founding pillars:
  - Distributed system
  - "Everything is a microservice"

#### Future plans

- Produce 1000 times more antiprotons than in 2018
- Formation of antihydrogen beam
- Free fall measurement for antihydrogen
- Antiprotonic atom program

