

# Characterization and Calibration of the RD53B CMS Chip

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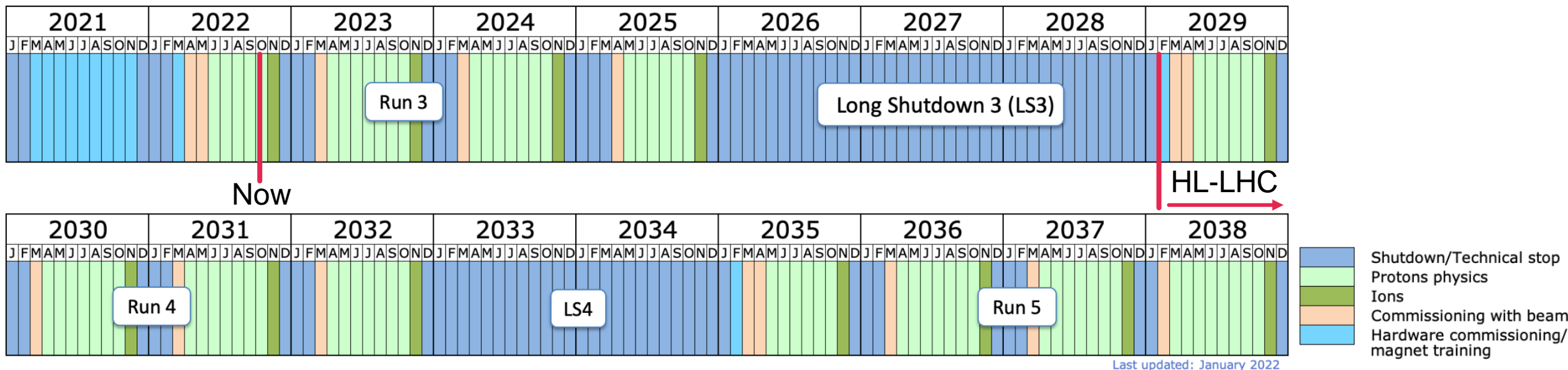


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2022-10-12

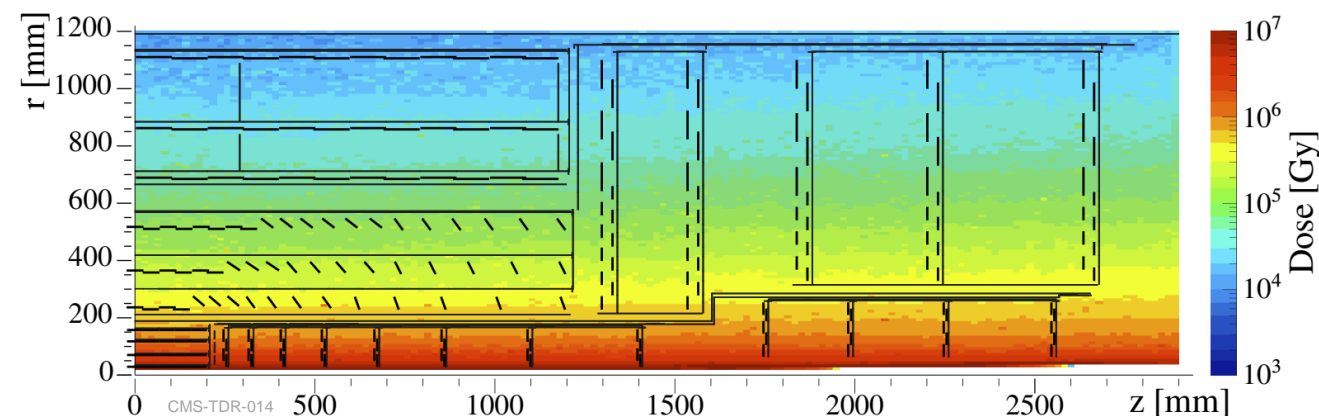
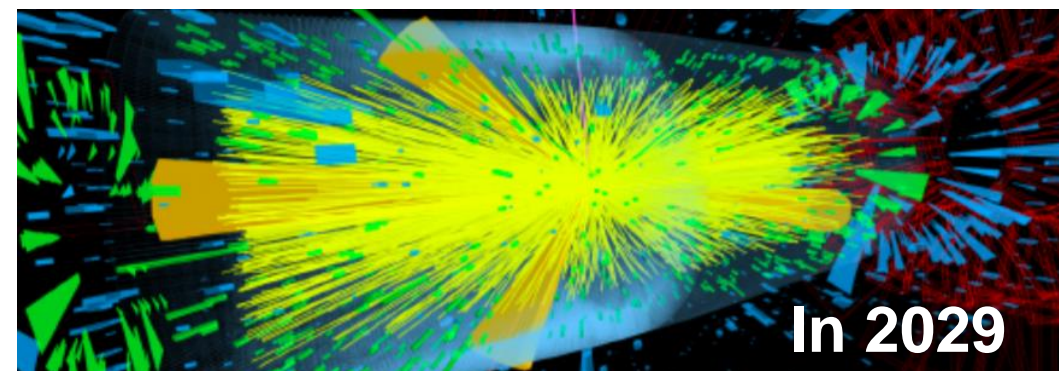
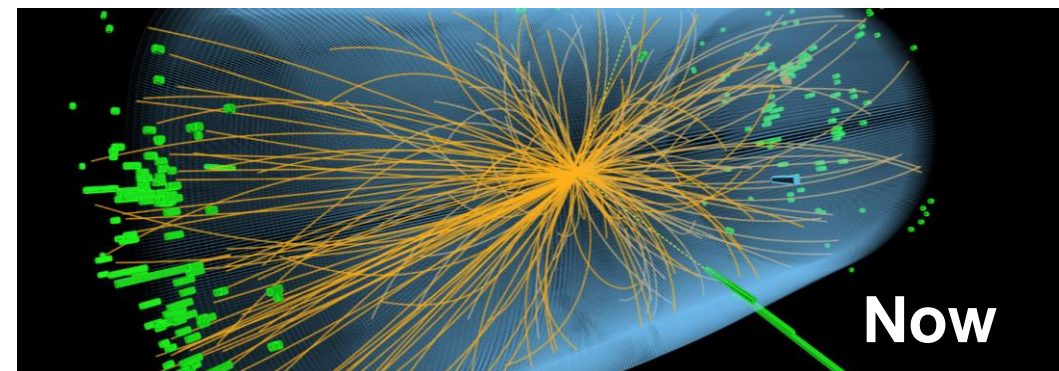
# HL-LHC upgrade schedule

- The High Luminosity LHC upgrade will take place during LS3
- This will result in:
  - pp collisions up to 14 TeV
  - Peak instantaneous luminosity: from LHC nominal  $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$   $\rightarrow$  to  $5\text{-}7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
  - Integrated luminosity: from nominal  $\sim 300 \text{ fb}^{-1}$   $\rightarrow$  to  $\sim 3000\text{-}4000 \text{ fb}^{-1}$
  - Average pile-up: from nominal **20-30**  $\rightarrow$  to **140-200**
  - $\sim 5$  times larger track multiplicity in the events than LHC nominal



# Detector requirements for Hi-Lumi

- 5x more collisions will greatly improve physics discovery potential, but there are also challenges:
  - More tracks → higher data rates, harder to separate tracks
  - More tracks → bigger radiation doses
- Therefore, the CMS tracker should satisfy the following requirements:
  - High granularity to efficiently separate tracks
  - High radiation tolerance to sustain efficiency up to  $3000 \text{ fb}^{-1}$
  - Contribution to level-1 trigger to ensure more efficient event selection at high luminosity
  - Extended acceptance range to improve the physics potential
  - Reduced material budget
- This makes the current CMS tracker not viable for operation after the HL-LHC upgrade





# (Current) CMS tracker

## CMS DETECTOR

Total weight : 14,000 tonnes  
Overall diameter : 15.0 m  
Overall length : 28.7 m  
Magnetic field : 3.8 T

STEEL RETURN YOKE  
12,500 tonnes

### SILICON TRACKERS

Pixel (100x150  $\mu\text{m}$ )  $\sim 1\text{m}^2 \sim 66\text{M}$  channels  
Microstrips (80x180  $\mu\text{m}$ )  $\sim 200\text{m}^2 \sim 9.6\text{M}$  channels

### SUPERCONDUCTING SOLENOID

Niobium titanium coil carrying  $\sim 18,000\text{A}$

### MUON CHAMBERS

Barrel: 250 Drift Tube, 480 Resistive Plate Chambers  
Endcaps: 540 Cathode Strip, 576 Resistive Plate Chambers

### PRESHOWER

Silicon strips  $\sim 16\text{m}^2 \sim 137,000$  channels

### FORWARD CALORIMETER

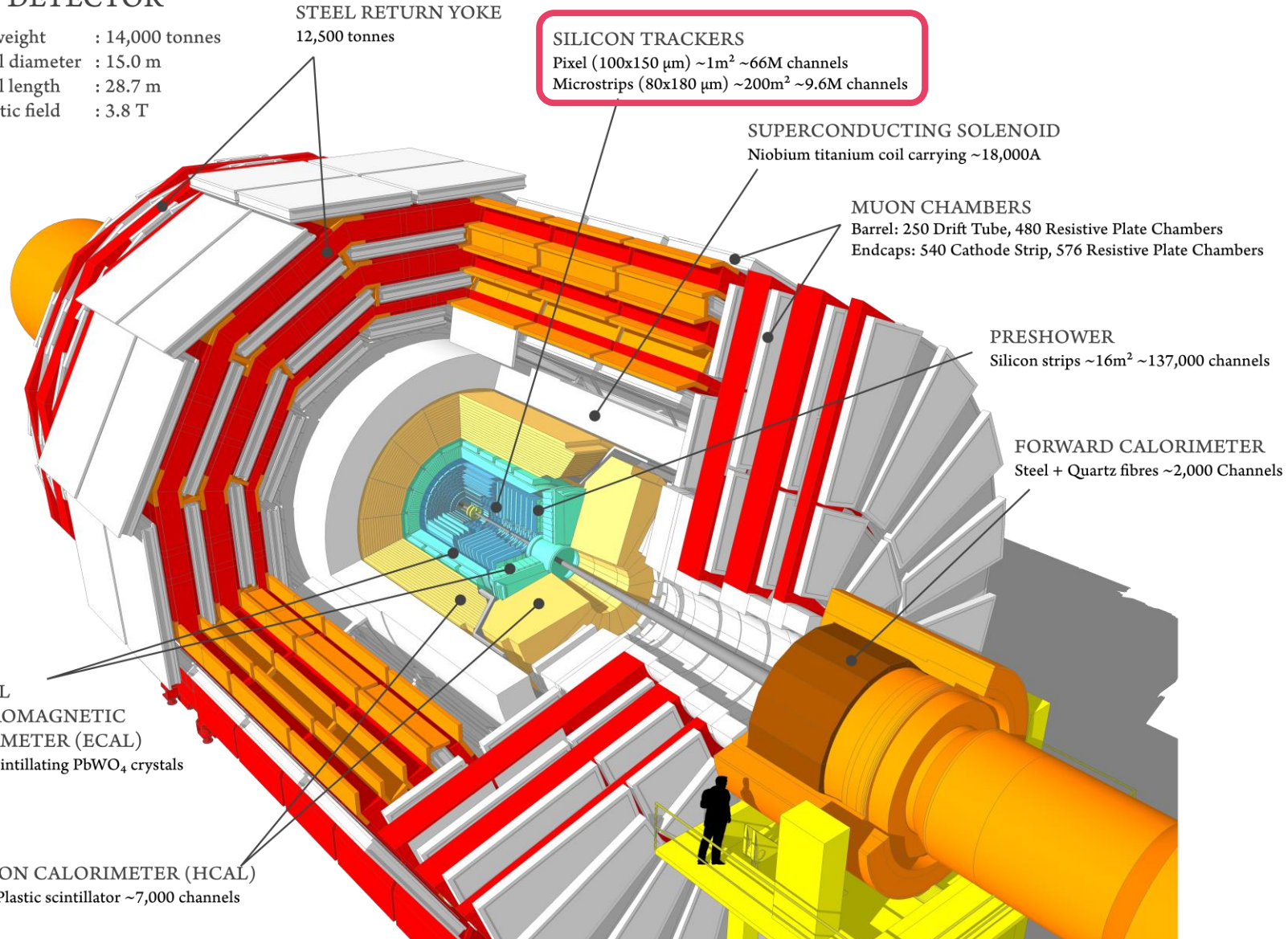
Steel + Quartz fibres  $\sim 2,000$  Channels

### CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)

$\sim 76,000$  scintillating  $\text{PbWO}_4$  crystals

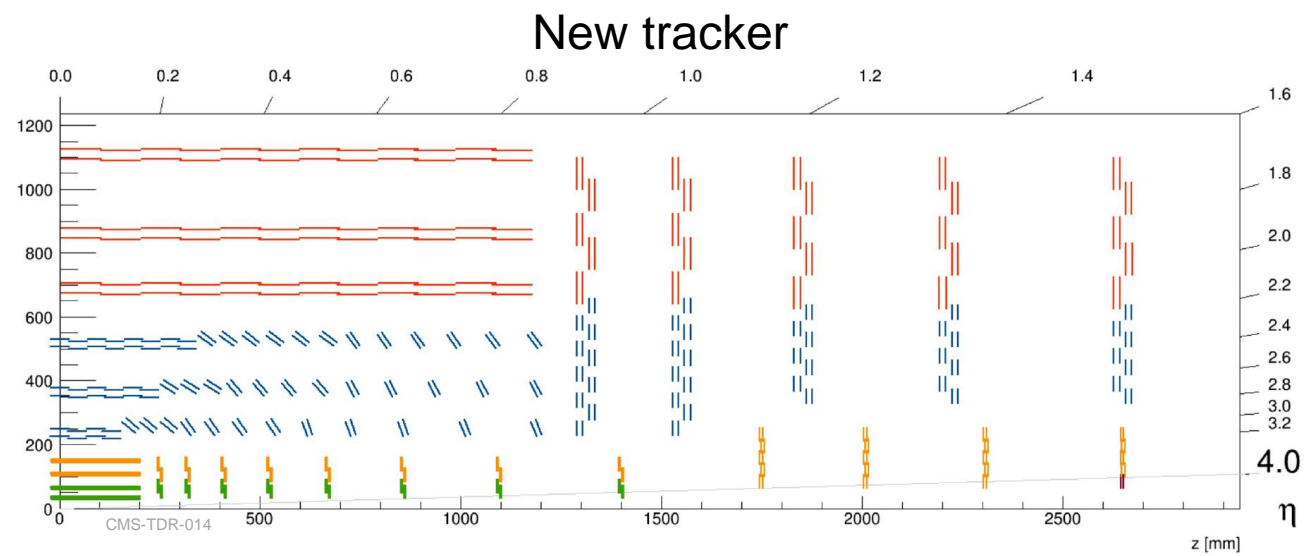
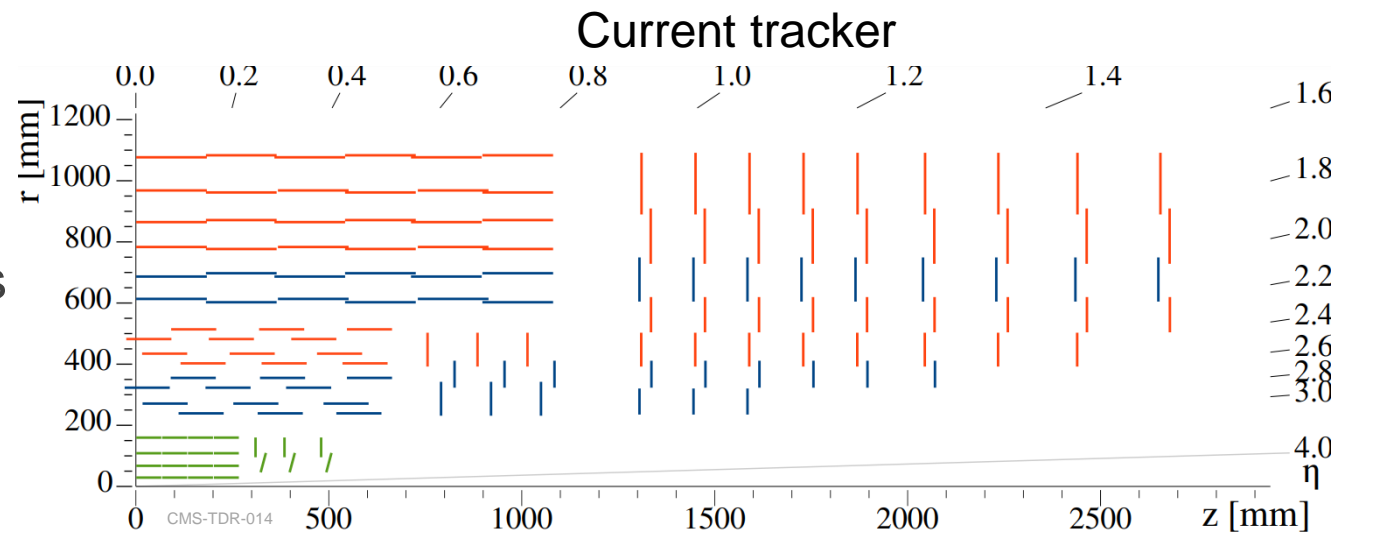
### HADRON CALORIMETER (HCAL)

Brass + Plastic scintillator  $\sim 7,000$  channels



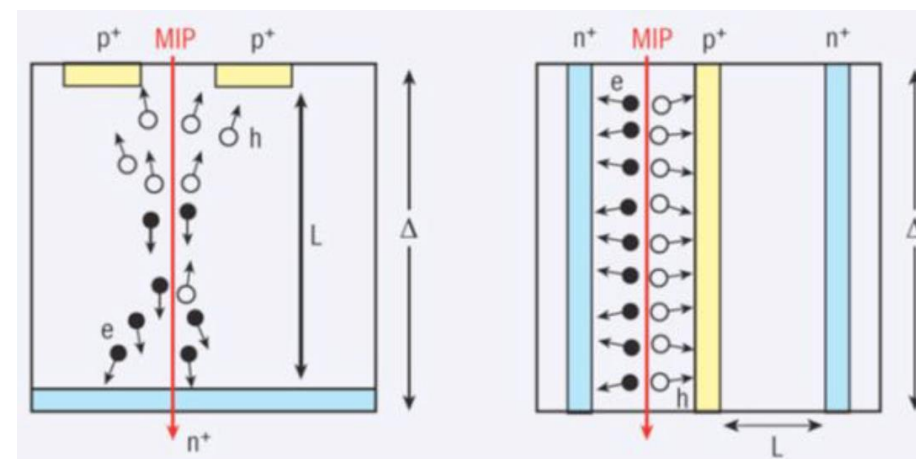
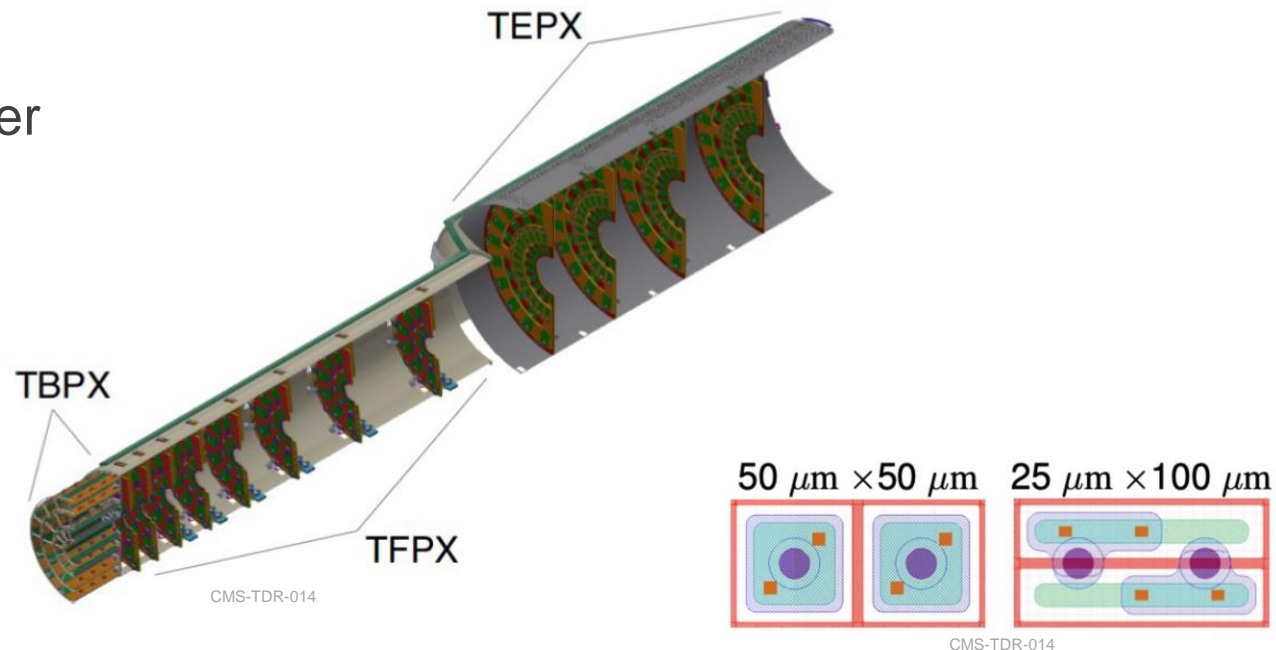
# Phase-2 CMS tracker upgrade

- Both CMS Inner and Outer Tracker systems will be completely replaced
- The Outer Tracker will have 6 barrel layers and 5 endcap disks per side and will feature micro-strip and macro-pixel silicon sensors
  - Outer Tracker will also contribute to the L1 trigger
- The inner tracker will have 4 barrel layers and 12 disks (instead of the current 3 disks)
  - This will greatly increase the tracking acceptance: up to  $|\eta| < 4.0$  instead of the current  $|\eta| < 3.0$



# The new Inner Tracker

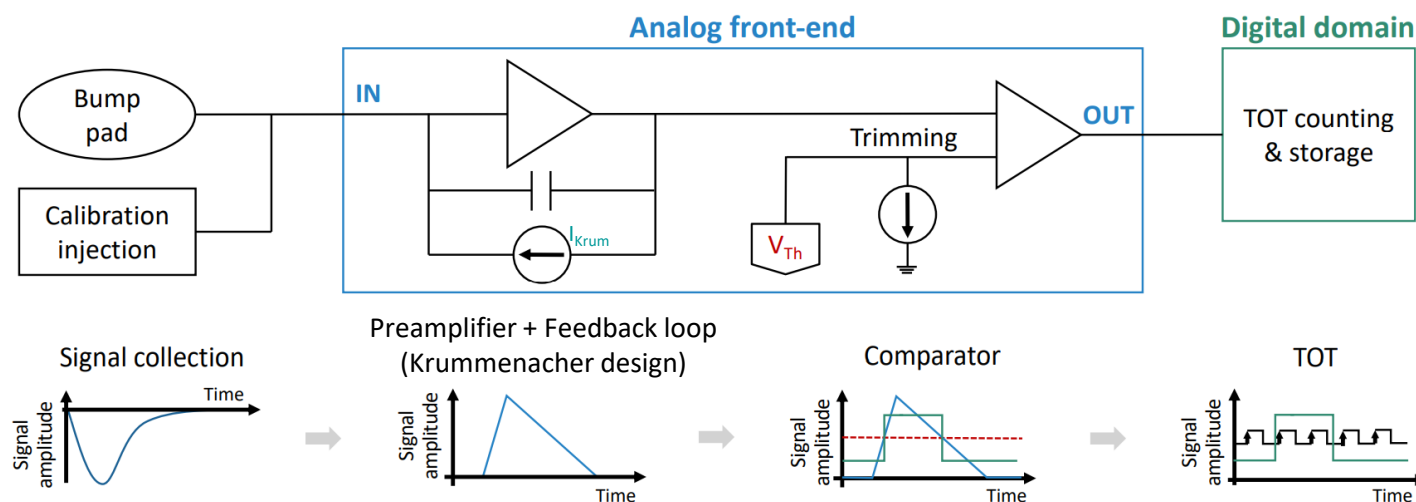
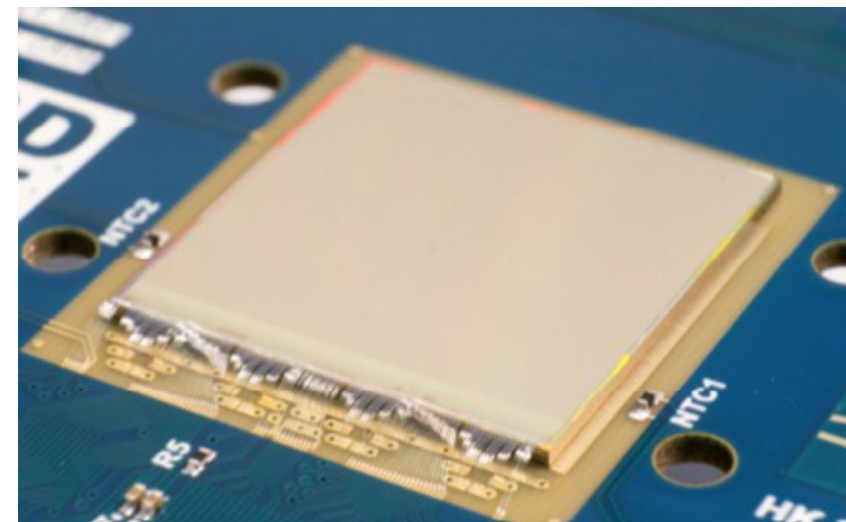
- The new Inner Tracker will feature ~6x smaller silicon pixels than the current one
  - $25 \times 100 \mu\text{m}^2$  or  $50 \times 50 \mu\text{m}^2$
  - $150 \mu\text{m}$  thickness
- Total active surface – around  $4.9 \text{ m}^2$
- Total pixel count – around 2 billion
- Two different pixel technologies will be used
  - 3D pixel sensors on barrel layer 1
  - n-in-p planar sensors everywhere else
- A readout chip based on 64 nm CMOS technology is developed by RD53 collaboration
  - RD53 is developing chips for both CMS and ATLAS with different features



<https://cerncourier.com/a/silicon-sensors-go-3d/>

# The CMS ReadOut Chip

- Features of the chip under development:
  - Able to withstand the radiation up to 1 Grad
  - Low power consumption of  $< 1 \text{ W/cm}^2$
  - Compatible with serial powering by using on-chip shunt-LDO regulators
- Second generation prototypes (RD53B) are undergoing tests
- The RD53B version for CMS is called CMS ReadOut Chip – CROC
  - 432×336 channels
  - Bump-bonded to the sensor
  - Wire-bonded to the readout
  - 4-bit digital readout for signal strength (ToT)

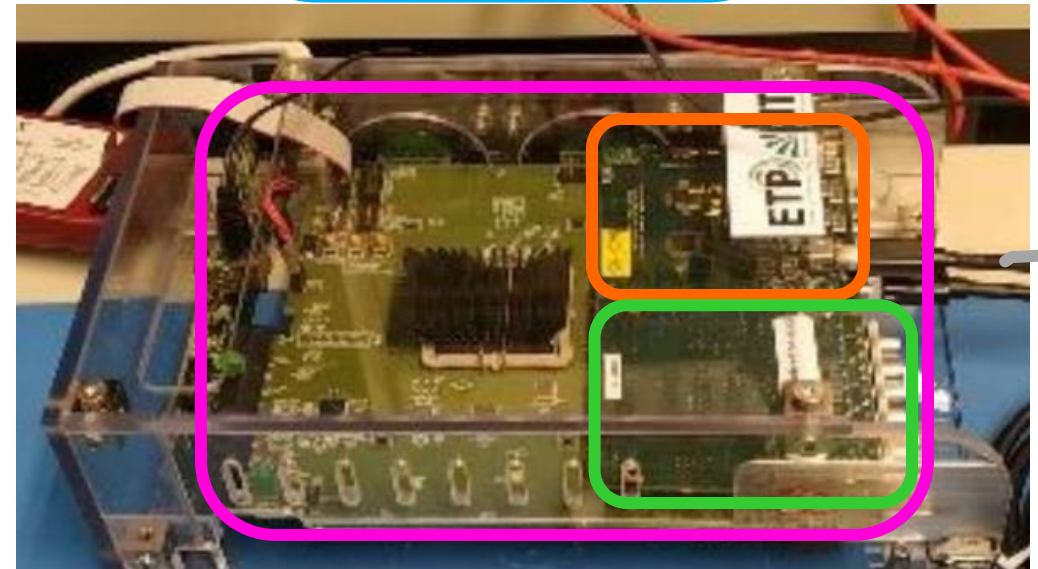
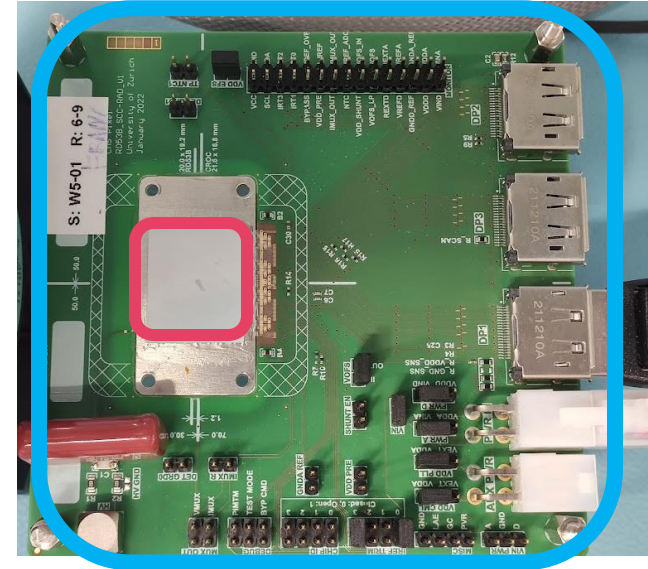


arXiv:2105.00070



Our test setup for CROC chips consists of:

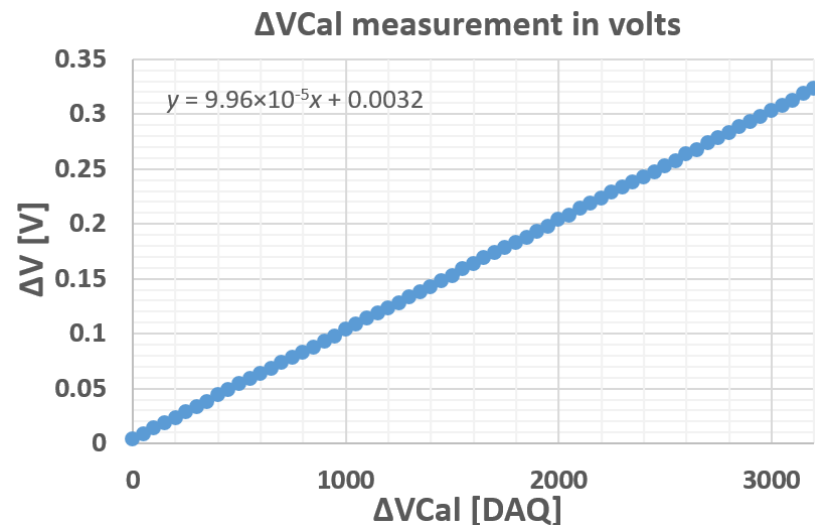
- Custom-made equipment:
  - A **CROC** chip mounted on a **Single Chip Card** (SCC)
  - Electrical readout **FMC board** connected to SCC via DP connection
  - **FC7 board** with FPGA and 2 FMC connectors
- Standard equipment:
  - **DIO5** FMC board (provides external trigger, clock, etc.)
  - Low and high voltage supply
  - Computer connected to the FC7 via IPbus
    - IPbus is a protocol used to communicate between software and firmware via ethernet (<https://ipbus.web.cern.ch/>)
    - Computer runs the Ph2-ACF software which is designed to perform both Inner and Outer Tracker hardware tests





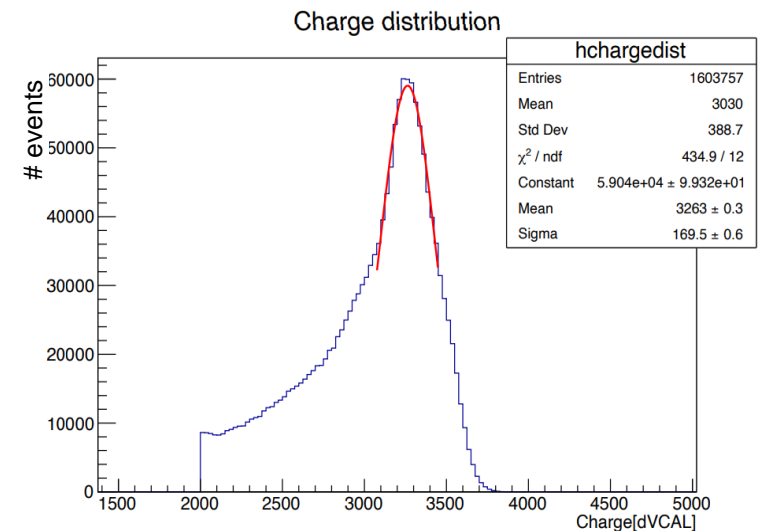
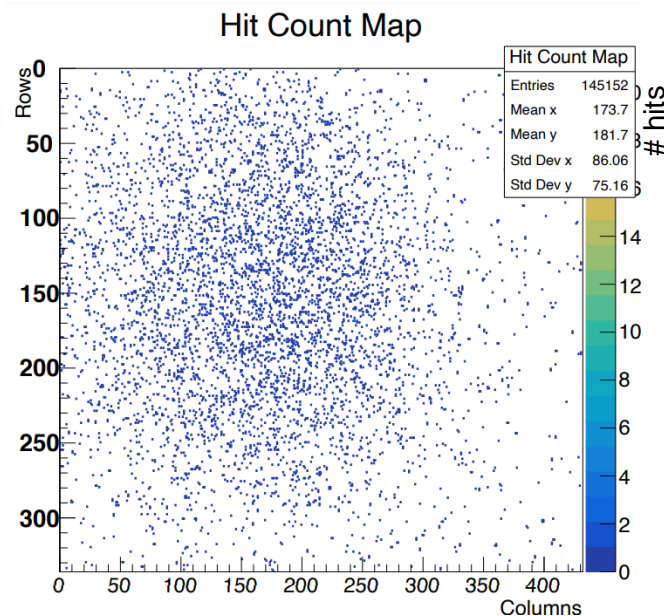
# Chip threshold unit calibration

- Thresholds are measured by injecting calibration pulses of known amplitude
- The chip uses DAC units ( $\Delta V_{Cal}$ ) to determine the calibration pulse and, therefore, the threshold
- We have used the internal voltage multiplexer of the CROC to measure the actual value for the threshold
- The nominal value given by chip designers is 5.5 electrons of signal per  $\Delta V_{Cal}$  unit
- Our measured  $\Delta V_{Cal}$  values on 2 different chips were closer 5.0 electrons of signal
- The threshold unit value of  $\sim 5.0$  electrons was also confirmed by using  $^{241}\text{Am}$  x-ray source (measurement done by Oceane Poncet)
  - X-rays are monochromatic (59.54 keV) and always release the same amount of signal in the sensor (16312 electrons)



$1 \Delta V_{Cal} = 9.96 \times 10^{-5} \text{ V}$   
 $C_{cal} = 7.94 \times 10^{-19} \text{ F}$   
 $1 \Delta V_{Cal} \rightarrow 7.91 \times 10^{-19} \text{ C}$   
 $1 \Delta V_{Cal} \rightarrow 4.93 \text{ e}^- \text{ of charge}$

Recorded pixel hits with  $^{241}\text{Am}$  source

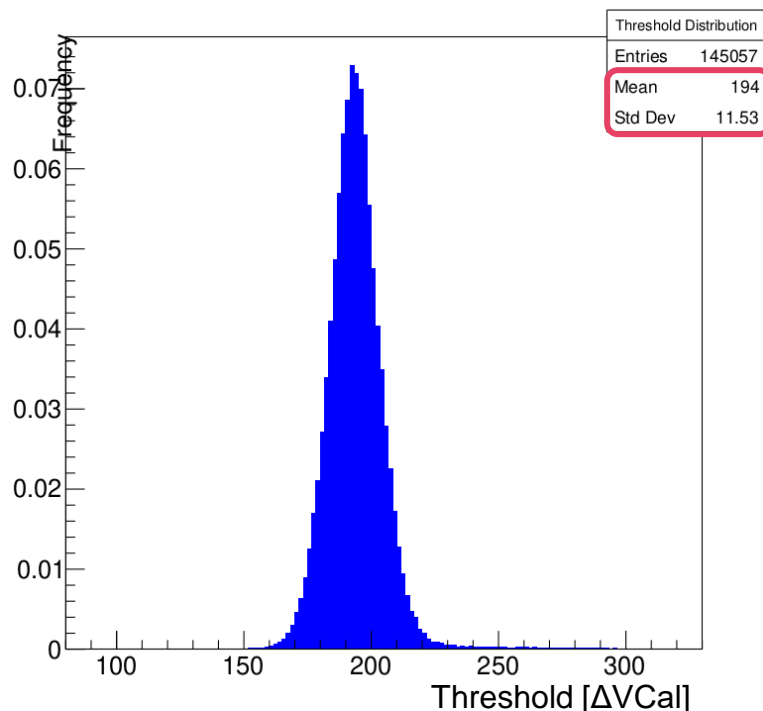


$16312 \text{ electrons} / 3263 \Delta V_{Cal} = 4.99 \pm 0.26 \text{ e}^- / \Delta V_{Cal}$

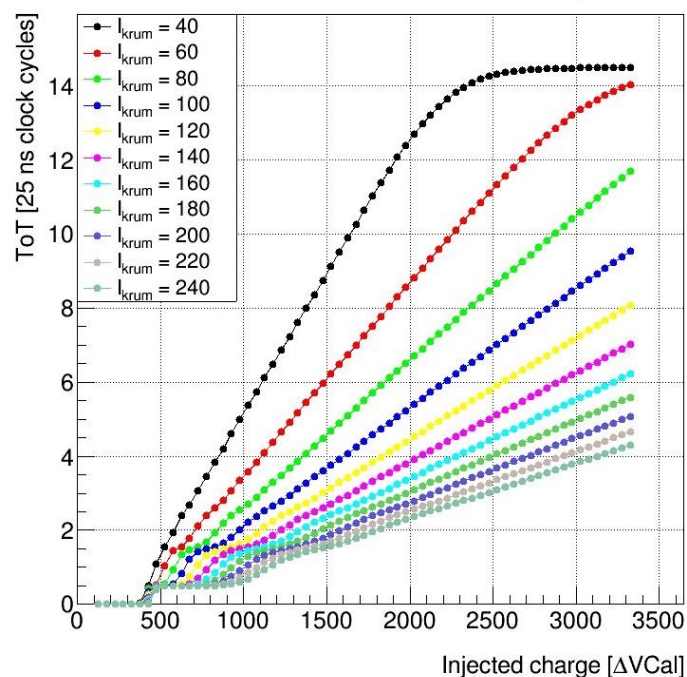
# Chip threshold and ToT gain tuning

- The threshold CROC chip can be successfully tuned at 1000 e<sup>-</sup> of signal (and possibly lower) with a threshold spread of only ~50 e<sup>-</sup> between the pixels
  - This is made possible by the trimming DAC, having 4 bits to trim the threshold for each pixel individually
- Pre-amplifier feedback (“Krummenacher”) current can be tuned to obtain different ToT gain curves
  - Charge resolution can go below 1000 e<sup>-</sup> per ToT (with very low dynamic range) or as high as 3500 electrons per ToT and more (with very high dynamic range)
  - ToT gain slope does not depend on the threshold itself, as expected with the linear analog front-end

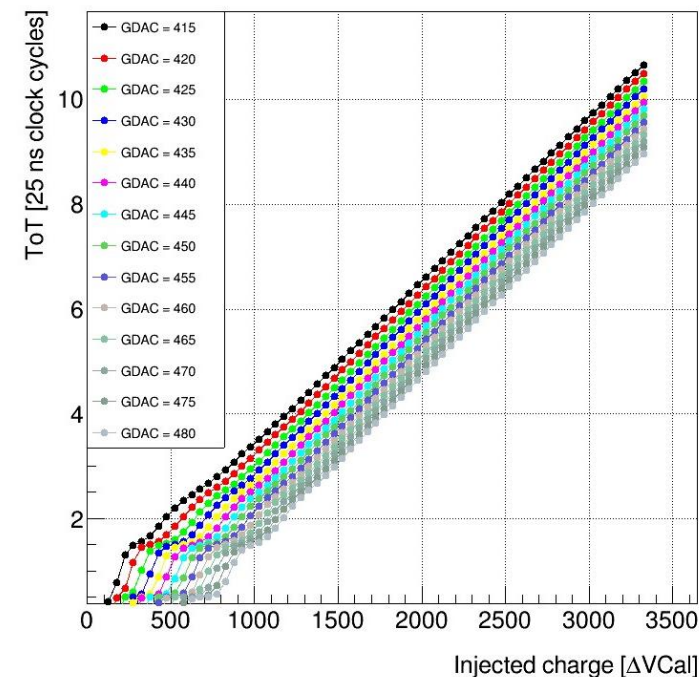
Threshold Distribution



Average ToT vs. injected charge



Average ToT vs. injected charge



- The HL-LHC upgrade will highly increase the physics potential but also will pose new challenges for the detector makers
- The detectors will need higher resolution, higher data output rates, and higher radiation tolerance
- A completely new tracker is being prepared for CMS
- Pixel detector chips for the Inner Tracker are developed by the RD53 collaboration
- 2<sup>nd</sup> generation chips, called CROC, are undergoing tests and showing good performance



Thank you!



# Pixel modules

- Two types of Pixel Modules
  - 1x2 and 2x2 readout chip
- 3892 module plus spares (1156 1x2, 2736 2x2)
  - 2 Billion pixels (124 million in current detector)
- Read Out Chip (ROC) – only active element on module

