A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology ⋆

Ivan Perić [a,*]

[a] *Institut für Technische Informatik, Mannheim, Germany*

Abstract

A new concept for monolithic pixel detector with 100 % fill-factor is presented. The detection is based on the charge collection in the depleted zone of the reverse biased diode. Complex pixel electronic, including charge sensitive amplifier, amplitude discriminator and digital storage element is placed completely inside the diode cathode (N-well). A test chip that comprises a small pixel matrix and test structures has been fabricated in a 0.35 μm high-voltage CMOS process and successfully tested. The results of the electrical tests and measurements with X-ray and beta radioactive sources are presented.

Key words: Monolithic pixel detector, Monolithic active pixel sensor, MAPS, High-voltage CMOS technology, Deep N-well, triple well.

1. Introduction

1.1. *High-voltage technologies*

The high-voltage CMOS technologies are originally used to design the electronic chips that drive automotive or industrial devices by means of high-voltage signals. By the term "high-voltage" we mean here any voltage which is significantly higher than the standard supply voltage for a typical low-voltage CMOS chip. The high-voltage technologies allow combination of the standard low-voltage CMOS transistors, used to implement internal electronics of the chip, and the high-voltage devices used in output drivers. In order to ease the interface between the low-voltage and the high-voltage circuits, most of the commercial high-voltage technologies offer so called "floating logic". Assuming a P-substrate process, the cross section of the floating logic looks like depicted in fig. 1. All transistors in fig. 1 are placed in a lowly doped deep N-well. The PMOS transistors are placed directly in the N-well, while the NMOS transistors are in the P-wells which are inside the deep N-well. It is possible to bias the deep N-well with a high voltage respecting to the P-substrate, typically more than 50 V. All transistors inside the N-well have only low voltages between their electrodes, which allows the use of small transistors. (The technology used in this project has the minimum gate length of 0.35 μm.)

⋆ This paper draws on results from an ongoing research project commissioned by the Landesstifftung Baden-Württemberg.

* Tel.: +49-621-1812732, *Email address:* peric@ti.uni-mannheim.de

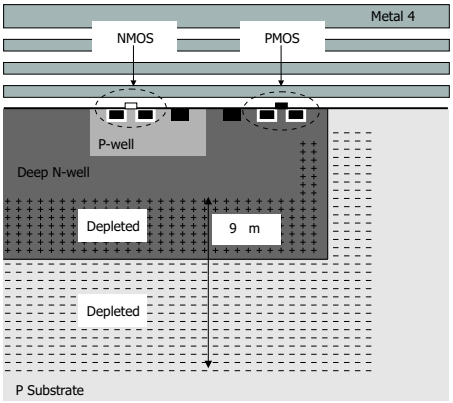

Fig. 1. Floating logic

1.2. *Monolithic detector in high-voltage technology*

The basic idea is to use the floating logic structure to implement a pixel detector for high-energy particles with 100 % fill-factor. Note, the depleted area between the deep N-well and the P-substrate (fig. 1) is relatively thick when the junction is reversely biased close to its breakdown. For 60 V reverse bias a depleted zone of about 9 μm is formed. [1] The particles which penetrate the depleted area generate relatively large amount of charge ($\sim$ 700e). The charge is separated by action of strong electric field in the depleted zone. This leads to a fast current signal.

The floating logic structure allows implementation of arbitrary complex CMOS readout circuits inside the deep N-well. These circuits can amplify the signal and allow the signal processing as threshold discrimination, time measurement, and data sparsification similar to that in a hybrid detector. The 3D-view to four pixels implemented as four "floating logic" blocks is shown in fig. 2. The depleted areas of neighboring pixels overlap and there are no insensitive areas.

The detector structure in fig. 2 might look similar to the triple-well MAPS described in [1]. There is, however, one important difference. The triple-well MAPS is implemented in a standard low-voltage process. It is a standard MAPS structure, which means that the signals are generated

[1] All numbers given here hold for the used 0.35 μm CMOS technology.

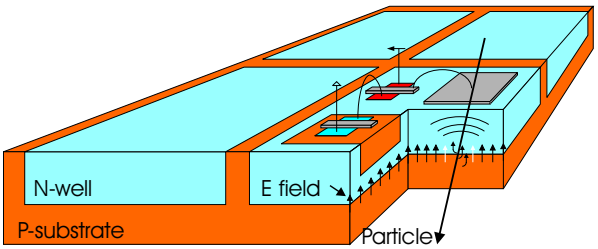

Fig. 2. Four high-voltage pixels

in the undepleted lowly-doped bulk or epi-layer and collected by *diffusion*. The detector proposed here is based on a different principle. It uses a high-voltage to induce a large depleted area and the main portion of signal comes from that depleted region. The signal is generated by *drift* in the high electric field. This makes the detector suitable for the applications where fast signals are needed. Also, a high radiation tolerance can be expected due to fast signal collection.

In order to demonstrate the feasibility of the concept a test chip has been designed in a 0.35 μm high-voltage CMOS process and tested. The test chip contains a small pixel matrix and a few test structures. Design details and test results are presented here.

2. Design details

Fig. 3 shows the schematic cross section of a pixel and the block scheme of the pixel electronics as implemented on the test chip. The pixel electronic

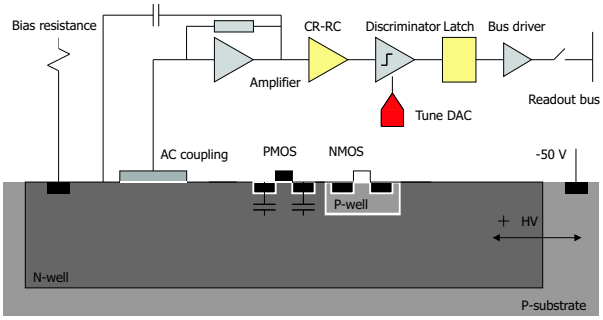

Fig. 3. Block scheme of the pixel

is completely implemented inside the deep N-well.

The P-substrate is biased with a high negative voltage respecting to the N-well. In this way a large depleted area is generated. The pixel electronics comprises a charge sensitive amplifier which is capacitive coupled to sensor, continuous reset, passive CR-RC filter, discriminator, 4-bit threshold-tune DAC (D/A converter) and a digital latch which stores the hit flag. The latch can be readout using a digital differential bus.

The large deep N-well (fig. 3) plays two roles. First, it is the substrate for the PMOS transistors and P-wells. Second, the deep N-well is the cathode of the sensor diode. It is common practice in the CMOS chip design to bias an N-well that contains PMOS transistors by shorting it with the positive supply. In this way it is assured that the source and drain diodes of the PMOS transistors are reversely biased. A low-ohmic bias is important to prevent the dangerous latch-up effect - the triggering of the parasitic thyristor which leads to a high current between positive supply and ground. In the case of the pixel structure in fig. 3, shorting of the N-well with the positive supply would lead to a signal loss. The electrons generated by a particle hit would simply flow into the positive supply line before the amplifier can react. To avoid such signal loss, the N-well is connected to the positive supply using a high (typically 1 GΩ) resistance. The potential of the N-well is in this case not constant. After a particle hit, the voltage of the N-well drops by a few hundred microvolts. This small voltage change is amplified by the amplifier and slowly cancelled by the current flow through the bias resistance. The latch-up can be prevented by careful biasing of the P-wells inside the deep N-well and by the use of guard rings.

An additional design problem is the crosstalk. Every PMOS P+ diffusion is capacitively coupled to the deep N-well and therefore to the sensor cathode. Since we are dealing with relatively weak input signals, even the crosstalk generated by a moderate voltage signal on a minimum size P+ diffusion can overtop the input signal. A great attention has to be paid; we will discuss the possible solutions of the problem in the following sections.

2.1. *Bias resistance*

The bias resistance (see fig. 3) is implemented using a PMOS transistor which operates in linear region (transistor Mb in fig. 4). A poly-silicon implementation would require unreasonably large space and would lead to a large parasitic capacitance. The gate voltage of the transistor Mb can be generated by a diode connected PMOS transistor placed outside the pixel, as shown in fig. 4. The bias current can be varied using a bias DAC placed on the chip periphery. The bias circuit works even when the DAC current is set to zero. The P+/N-well diodes that have anodes connected to the positive supply (*vdd*) act then as bias resistors and define the N-well potential. One such diode is depicted in fig. 4. The diode-based bias is used in some MAPS implementations with continuous reset and AC-coupled sensor [2,3]. The P+/N-well diodes conduct small leakage currents. They work at the onset of forward region having high dynamic resistance. They introduce therefore very little noise.

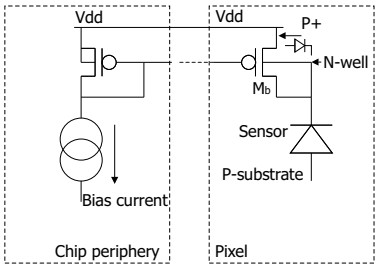

Fig. 4. Bias resistance

2.2. *Amplifier*

The transistor scheme of the charge sensitive amplifier is shown in fig. 5. The amplifier is AC-coupled to the sensor. The AC-coupling allows the use of the amplifier types that have input node DC-voltage different than the N-well bias potential. In our case the amplifier has a folded-cascode single-ended topology with a PMOS transistor as input device. The amplifier is biased with a relatively small current (9 μA).

As already mentioned, every P+ diffusion (denoted in fig. 5 by letters a, b, c and d) is capacitively

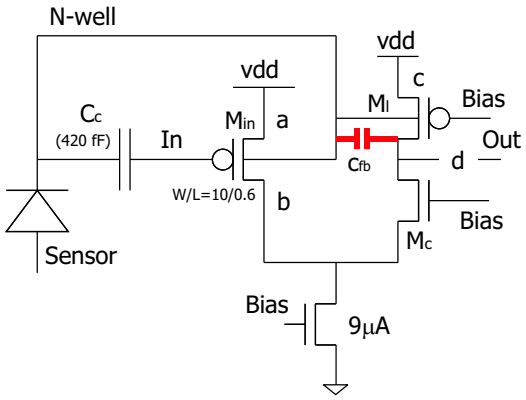

Fig. 5. Charge sensitive amplifier

coupled to the N-well and can be source of unwanted crosstalk. P+ diffusions a and c are shorted to the positive supply and represent solely an additional detector capacitance. The same holds for P+ diffusion b which is kept by the action of casode transistor Mc at a nearly constant potential. The P+ diffusion d is the output of the amplifier and the signals on this node are capacitively coupled to the N-well (sensor). The capacitance between diffusion d and the N-well (c_{fb}) acts as the parasitic capacitive feedback for the charge sensitive amplifier. The charge sensitive amplifier is designed without any other feedback capacitor, it relies exclusively on c_{fb} capacitance. The charge gain of the amplifier is $1/c_{fb}$.[2] Since the load transistor (Ml) can be made narrow (there is no need for a large trans-conductance) diffusion capacitance c_{fb} can be kept small (0.9 fF). In this way a high charge gain can be achieved.

It is worth mentioning that the parasitic feedback connects the output of the charge sensitive amplifier with the input prior to the coupling capacitor Cc, see fig. 5. The coupling capacitor is therefore included in the feedback loop. Usually, the feedback capacitor of an charge amplifier is placed between its output and the gate of the input transistor. The coupling capacitor is then placed outside the feedback loop. Including of the coupling capacitor in the feedback loop has the advantage that there is no signal loss due to charge division between the coupling and sensor capacitance (provided the gate capacitance of the input transistor is much smaller than the sensor capacitance). The coupling capacitance does not need to be larger than the sensor capacitance.

[2] In the real circuit, there is a certain additional feedback due to parasitic capacitances between metal traces.

2.3. *Resistive feedback as continuous reset*

The scheme of the continuous reset circuit is shown in fig. 6. The circuit stabilizes the amplifier

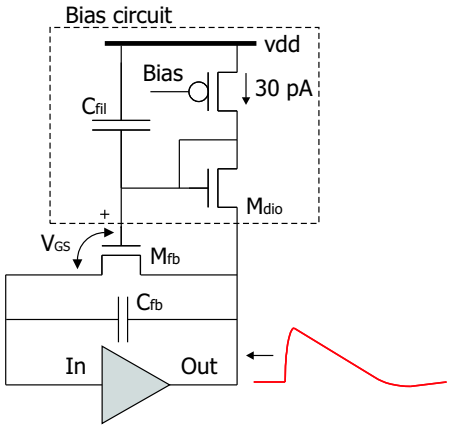

Fig. 6. Continuous-reset circuit

and discharges the feedback capacitance after signal integration. For large positive output signals the current of the feedback transistor Mfb saturates and the feedback capacitance is discharged with a constant current until the output signal drops below a few thermal voltages ($v_T \sim 26\,\mathrm{mV}$). A typical output waveform is sketched in fig. 6. The bias circuit (shown in fig. 6) is used to generate the gate-source voltage for the feedback transistor which is independent on the DC potential at the input of the amplifier. The same circuit has been used in [4]. The bias circuit in fig. 6 allows us to change the amplifier bias without to influence the feedback resistance.

2.4. *Passive shaper and threshold control*

Fig. 7 shows the CR-RC shaper, threshold tune circuit and discriminator. The shaper and discriminator are implemented using of only NMOS transistors in order to avoid the capacitive crosstalk

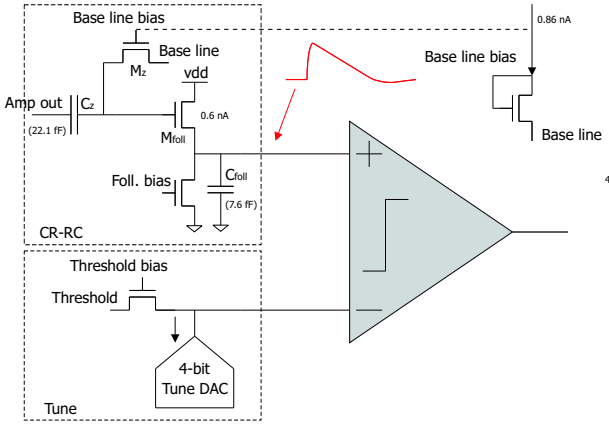

Fig. 7. Shaper, threshold tune circuit and discriminator

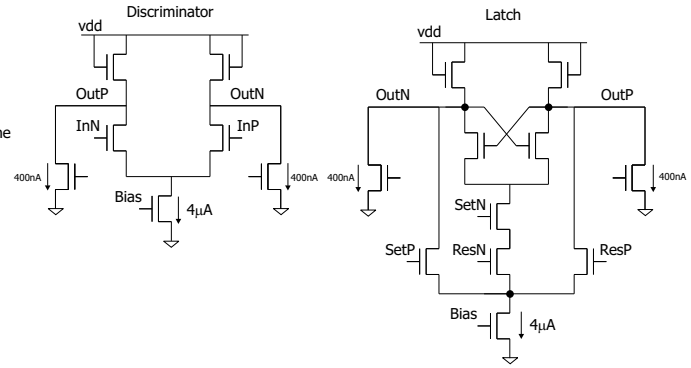

Fig. 8. Discriminator and current-mode latch

of signals to the N-well sensor electrode. The CR stage (devices Mz and Cz) has the purpose to improve the threshold matching and prevent the low-frequency noise passing the shaper. The bias settings of the transistors can be varied using the in-chip DACs, the typical time constant of the CR stage (derived from the small signal parameters) is 1.3 μs. The RC stage is implemented as a source follower with capacitive load (devices Mfoll and Cfoll), its task is to limit the bandwidth of the system and decrease the noise component generated by the input transistor of the amplifier. The typical RC time constant used in measurements is 500 ns.

Four-bit tune DAC is implemented as a matrix of 15 identical NMOS current sources. The both transistors Mz and Mfoll saturate after receiving of a large signal and the voltage at the output of the shaper returns to the base line with constant speed. The pulse width at the output of the discriminator is linearly proportional to the signal amplitude. (Supposing the signal amplitude is higher than a few thermal voltages.) This gives the possibility to determine the signal amplitude by measuring the discriminator pulse width. The same technique has been used in the ATLAS pixel-chip [5].

2.5. *Discriminator and latch*

The discriminator is implemented as an NMOS-based fully-differential amplifier with NMOS diodes as the load, fig. 8. The circuit is followed by a differential current-mode latch which stores the hit flag. Like the discriminator, the latch is realized exclusively with NMOS transistors, as shown in fig. 8.

2.6. *Pixel layout*

Fig. 9 shows the sketch of the pixel layout. Pixel

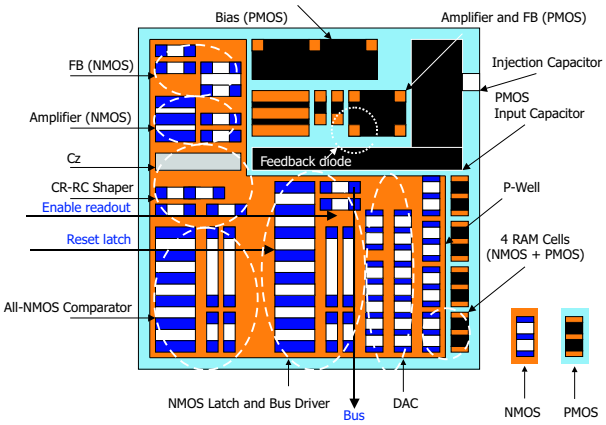

Fig. 9. Pixel layout

dimensions are 50×50 μm^2. About tree-fourth of the pixel area is occupied by the large P-well which contains all the NMOS transistors. The P-well represents a large detector capacitance, about 180 fF. This part of the detector capacitance is much larger than the part coming from the N-well/P-substrate junction capacitance (∼38 fF). The reason for this is that the N-well/P-substrate diode is biased with a high reverse voltage (∼ 60 V) and its capacitance per unity area is significantly decreased. The re-

verse bias of the N-well/P-well junction is only 3.3 V leading to a relatively large area capacitance.

The coupling capacitor is implemented as a large PMOS capacitor.

2.7. *Test chip*

Fig. 10 shows the block scheme of the test chip. It contains a matrix with four times ten "regular"

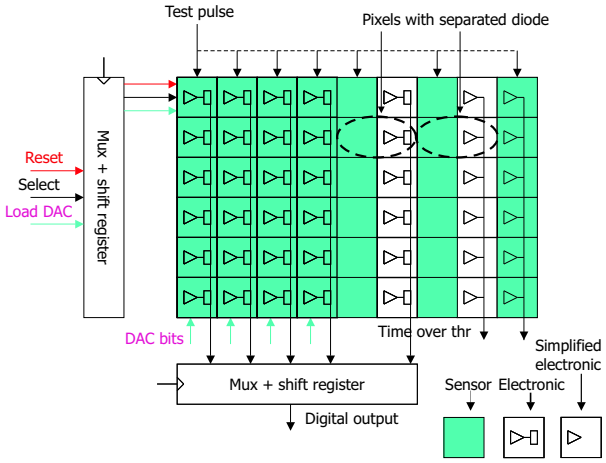

Fig. 10. Block scheme of the test chip

pixels that contain all circuits shown in fig. 3. A pixel row can be selected for readout by applying of horizontal signal *Select*. There is an additional column of ten test pixels. These pixels have the same readout electronics like the regular pixels but the N-well sensor cathodes are separated from the readout circuitry and placed nearby. The N-wells housing the electronics are insensitive and shorted to the positive supply. The separated sensor cathodes have the same size like the N-wells of the regular pixels, however they are relatively empty and do not contain large P-wells. [3] The capacitance of a separated sensor diode is therefore low (38 fF) and one can expect that the test pixels have good noise performances. Of course, a detector with 100% fill factor can not be made by such test pixels since the area below the readout electronics is insensitive. [4] The purpose of the test pixels is solely to measure the signal amplitudes and perform accurate calibrations without limitations that can arise from excessive noise. The last two pixel rows in fig. 10 contain the test and regular pixels with simplified readout electronics. The discriminator outputs of these pixels can be multiplexed out and directly measured. In this way the signal amplitudes can be indirectly measured by measuring the time over threshold. In every pixel there is a small metal-metal capacitor which allows injection of a test charge into the sensor. The chip has been implemented in a 0.35 μm high-voltage CMOS process.

3. Measurements

Electrical tests and measurements with radioactive sources has been performed on the chip.

3.1. *Electrical tests*

The electrical test are based on the test injection circuit which is used to determine the response of the readout channels to a known input charge signal. [5] In the case of the regular pixels, only a binary hit flag can be readout. Because of that the threshold scan has to be used to determine the threshold and noise. In the case of the pixels with simplified readout electronics, the signal amplitude can be determined also by measuring of the discriminator pulse length.

Fig. 11 shows an example of noise measurement. The noise of a regular pixel and the noise of a pixel with separated sensor been measured. Bias current of the charge sensitive amplifier has been varied. Since the bandwidth of the amplifier-shaper system has been kept constant, the increase of the bias

[3] The separated cathode contains only a large coupling PMOS capacitor and a PMOS bias transistor.

[4] We neglect here the lateral diffusion from the P-substrate.

[5] The capacitance of the metal-metal test injection capacitor can be estimated from the layout using a capacitance extraction tool. The extracted value has been checked by measurements with Fe-55 X-ray source.

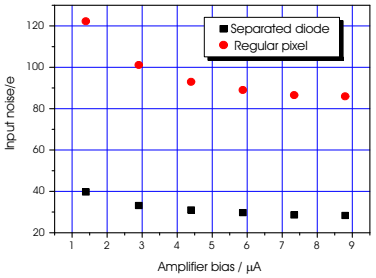

Fig. 11. Measured noise versus amplifier bias current

current led to decreased output noise.[6] For the standard amplifier bias current (9 μA) the noise of the regular pixel was $\sigma \sim 85$ e and the noise of the pixel with separated sensor $\sigma \sim 30$ e. This is result of different sensor capacitances (regular pixel: $c_{det} \sim 220$ fF, pixel with separated sensor: $c_{det} \sim 38$ fF).

Thresholds of pixels in the matrix have been measured; after the measurement the threshold dispersion has been alleviated using the threshold-tune DACs. Fig. 12 shows the results. The dispersion of the tuned thresholds was $\sigma \sim 75$ e.

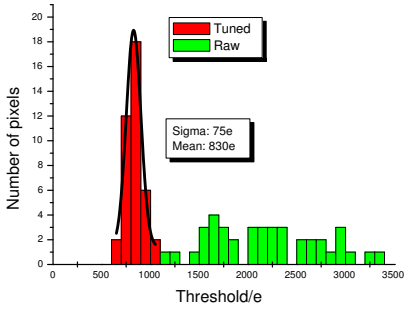

Fig. 12. Measured threshold dispersion before and after tuning

The noise and threshold measurements presented here give us the estimation of the minimum signal which can be detected in all matrix pixels by keeping the noise occupancy low:

$$S_{min} \sim 6 \cdot \sigma_{Th} + 6 \cdot \sigma_N \sim 960\ e.$$

[6] Note, the increase of the trans-conductance of the input transistor causes the decrease of its the gate-referred noise spectral power.

3.2. *Measurements with radioactive sources*

The aim of the measurements with radioactive sources was to calibrate the test capacitors, determine the minimum ionizing particle signal and demonstrate spatial resolution.

The spectral measurements required pulse-length calibration. Fig. 13 shows a typical pulse-length (time over threshold) vs. input signal characteristic measured with the test injection circuit. Note, the input signal is expressed as the voltage step applied to the injection capacitor. As can be seen, the time over threshold characteristic is nearly linear in the case of large input signals.

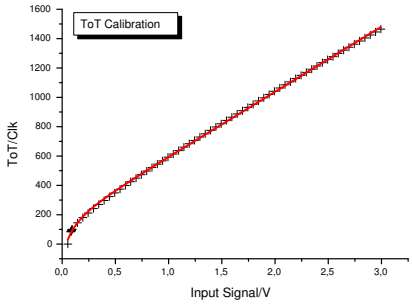

Fig. 13. Measured time over threshold versus input signal, Clk = 20 ns

Fig. 14 shows the Fe-55 spectrum measured with a regular pixel. The signal amplitude is represented in time over threshold units. The 6 KeV peak can be clearly seen. The threshold has been set high enough and there is no noise peak. By knowing the

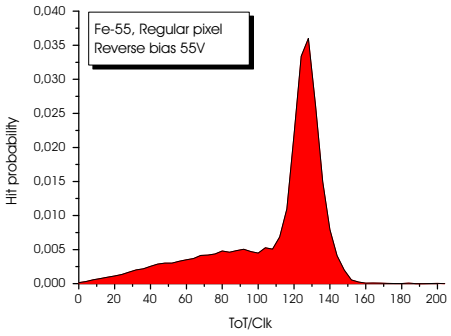

Fig. 14. Fe-55 spectrum measured with a regular pixel

time over threshold corresponding to the input of 6 KeV and by using the characteristic in fig. 13, injection capacitance can be calculated.

Fig. 15 shows the Fe-55 spectrum measured with a pixel with separated sensor. It can be seen that

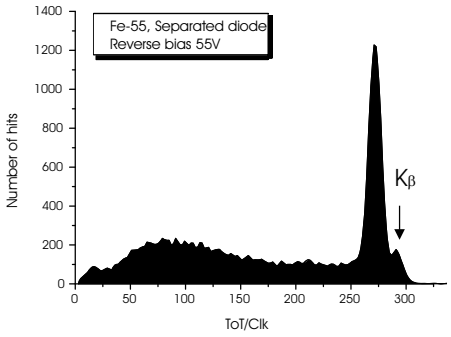

Fig. 15. Fe-55 spectrum measured with a pixel with separated diode

this pixel has lower noise than the regular one. K_β peak can be clearly recognized.

Fig. 16 shows the Sr-90 spectrum measured with a regular pixel. The measurement has been done

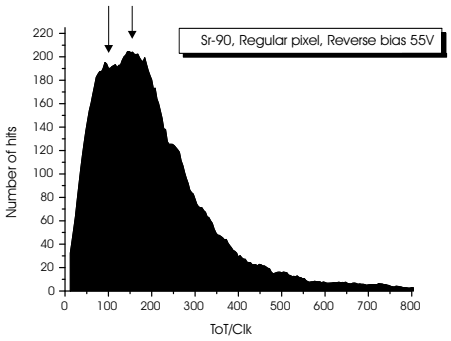

Fig. 16. Sr-90 spectrum obtained with a regular pixel

without trigger. The figure shows the amplitude histogram of all signals received from the pixel during the irradiation. The low-energy β^- particles has been shielded by a 2 mm thick plastic absorber. The spectrum appears to have two peaks. The higher peak corresponds to an input signal of 2000 e and the lower peak to an input of 1100 e. The results are not easy to interpret since no trigger have been used. One explanation is the following. The higher peak is the result of two effects. First, the signal generation in the depleted zone. Second, the ionization in the *undepleted* lowly-doped P-substrate below the pixel. The lower peak comes from the ionization in the depth of the P-substrate caused by the particles that pass near the pixel. The charge generated in the undepleted P-substrate is collected by diffusion, like by the standard MAPS structures. If we assume that the β^- particles coming from the shielded Sr-90 source generate in average 20% more charge than the minimum ionizing particles, [7] we can estimate a minimum ionizing signal to be about 1700 e. Note, the six sigma value for the noise and the threshold dispersion is about 960 e.

The estimated MIP signal is substantially higher than the signal we theoretically expect to come from a depleted zone of 9 μm ($\sim$ 700e). The signal excess of about 1000 e can be result of the ionization in the undepleted substrate. This would be in agreement with the measurements performed on the MAPS without epi-layer [6].

The results shown in fig. 17 can be understand as the confirmation of the assumption that the higher spectral peak reflects the ionization in the depleted area. The figures show Co-60 spectra for different reverse bias voltages of the sensor diode. Fig. 17 (a) shows the spectrum for a high reverse voltage (60 V). Two peaks can be easily distinguished. If we decrease the reverse bias voltage (figures (b) and (c)), the higher peak moves towards lower amplitudes which can be effect of decrease of the depleted zone. The lower peak stays unchanged. This peak is most probably the result of the signal generation outside the depleted zone.

Fig. 18 shows the image of a wire obtained by irradiation with Fe-55 source. The average threshold was about 830 e.

4. Conclusions and perspectives

A novel concept of a monolithic pixel detector with 100% fill-factor has been proposed and verified on a test chip. The detector has been implemented in a commercial 0.35 μm high-voltage

[7] This can be calculated starting from the known thickness of the absorber and the beta spectrum of Sr-90.

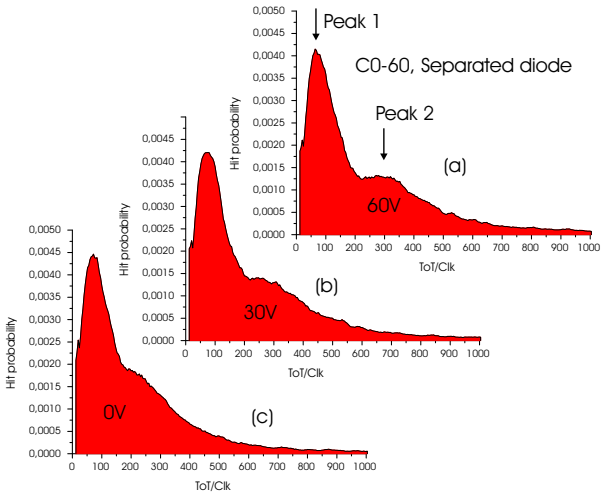

Fig. 17. Co-60 spectra for different reverse bias voltages

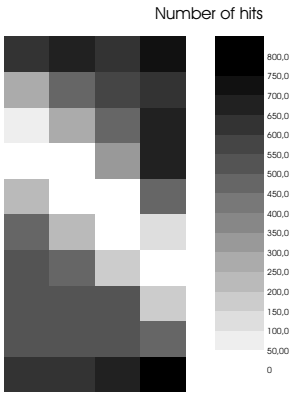

Fig. 18. Image of a wire obtained with Fe-55 source

CMOS process. The detection of high energy particles is based on the use of a lowly doped N-well/P-substrate diode as sensor. The junction is depleted by applying of a high reverse bias voltage. The signals generated in the depleted zone are collected by the drift in the strong electric field. Using the possibility to place CMOS circuits inside the N/well, complex readout electronics is implemented inside the sensor cathode.

There is no other monolithic pixel sensor based on a commercial CMOS process with 100% fill-factor that uses the charge drift in depleted zone as the main signal source known to the author. Since the charge collection does not rely on diffusion (like by all other reported MAPS) a high radiation tolerance can be expected. This detector is potentially very fast due to high electric field in the active zone.

The prototype chip has been successfully tested. All circuits work as expected. The preliminary results lead to an estimated MIP signal which exceeds 1.7 times the minimum signal required for the efficient detection and low noise occupancy. The numbers are based on the measured noise and threshold dispersion.

More accurate measurements of the MIP signal and spatial resolution are planned. A new prototype chip will be submitted soon. The goal of the new design is to decrease noise and threshold dispersion and implement a trigger based readout. The new prototype will be designed using the radiation tolerant layout techniques. This will allow the measurements of radiation hardness.

References

[1] G. Rizzo et al., A novel monolithic active pixel detector in 0.13 μm triple well CMOS technology with pixel level analog processing, Nucl. Inst. and Meth. A 565 (2006) 195

[2] G. Deptuch et al., Development of monolithic active pixel sensors for charged particle tracking, Nucl. Inst. and Meth. A 511 (2003) 240

[3] G. Deptuch et al., Monolithic active pixel sensors with on-pixel amplification and double sampling operation, Nucl. Inst. and Meth. A 512 (2003) 299

[4] L. Blanquart et al., Pixel analog cells prototypes for ATLAS in DMILL technology, Nucl. Inst. and Meth. A 395 (1997) 313

[5] I. Peric, L. Blanquart, G. Comes, P. Denes, K. Einsweiler, P. Fischer, E. Mandelli, G. Meddeler, The FEI3 readout chip for the ATLAS pixel detector, Nucl. Inst. and Meth. A 565 (2006) 178

[6] W. Dulinski, et al., CMOS monolithic active pixel sensors for minimum ionizing particle tracking using non-epitaxial silicon substrate, IEEE Trans. Nucl. Sci. 51 (2004) 1613