Status and Upgrade Plans of the Belle Silicon Vertex Detector

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Abstract

Second generation of Belle silicon vertex detector has been operated well for more than three years. With increasing beam-induced background, degradation of the detector performance is expected. To avoid such a difficulty, we are planing a next upgrade, third generation of the silicon vertex detector. Currently, its design is almost finalized.

Key words: Belle; KEKB; Silicon strip detector, APV25

1. Introduction

The Belle detector (1) is a large-solid-angle magnetic spectrometer designed to study CP violation in B meson decays. The B mesons are produced in pairs at the KEKB energy asymmetric electron-positron (8 and 3.5 GeV) collider operating at the $\Upsilon(4S)$ resonance with the world highest luminosity of 1.7×10^{34} cm^{2}s^{-1} . The $\Upsilon(4S)$ is produced with a Lorentz boost factor of $\beta\gamma = 0.425$, and subsequently decays into two B mesons. One of the main goals of the experiment is precise measurement of the time-dependent CP violating parameters in the neutral B meson system. An accurate determination of the distance between decay vertices of the two B mesons is a crucial point in these studies. Since the distance between the two vertices is 200 μm on average, the vertex detector must be able to measure the distance between them with a precision better than 100 μm. The Belle Silicon Vertex Detector (SVD) plays a key role in these measurements.

The initial version of the SVD (SVD1 (2)) has been working since 1999. Its very good performance contributed to many important physics results, like the discovery of CP violation in the B sector in 2001 (3). The SVD1 design had, however, several shortcomings, like limited radiation tolerance, non-negligible dead time and sensitivity to the so-called pin-hole effect. To solve these problems, SVD1 was replaced with a new version, SVD2 (4), and since October 2003 successfully operates in the experiment. Problems associated with SVD1 and a comparison of the performance of SVD1 and SVD2 are described elsewhere (4; 5; 6)

The beam-induced background is gradually increasing as a side effect of the luminosity improvement of the KEKB, and the performance degradation of the SVD is expected. To avoid such difficulties, we are planing a next upgrade, SVD3. In this paper, we describe the status and the upgrade plans of SVD.

2. SVD2

2.1. *Detector configuration*

The schematic view of SVD2 is shown in Fig. 1. The detector is built from 246 AC couple double-sided silicon detector (DSSD) fabricated by Hamamatsu Photonics. Their configurations are summarized in Table 1. The DSSDs are arranged in four layers surrounding the beam pipe. The radii of the four layers are 20, 43.5, 70 and 88 mm. The layers are constructed from 6, 12, 18 and 18 independent ladders consisting of 2, 3, 5 and 6 DSSDs, respectively. To minimize the capacitance of the single readout channel, the ladders are split in halves each of which is read out on the outer end. The SVD2 covers the geometrical acceptance of the drift chamber ($17° < \theta < 150°$ in polar angle).

The SVD2 has in total 110,592 strips, and their signals are read out by the VA1TA chips from IDEAS (7). The VA1TA chip is fabricated using a 0.35 μm CMOS process, and can stand up to 200 kGy irradiation. Four VA1TA chips have been deployed on for each hybrid boards, and they are mounted at both ends of each ladder. The p and n sides of each half-ladder are read out by separate hybrids. A single hybrid board read out 128 $\times$ 4 = 512 channels with about 800 ns shaping time. The signals are transmitted to a repeater system installed in boxes at the end-plate outside the main detector volume. To avoid the pin-hole effect, the ground of the readout electronics is at level of the detector bias voltage ($\pm$40 V). The decoupling from the ground potential of the rest of the electronics takes place in the repeater system by opto-coupler devices. Amplified signals are transmitted to outside of the Belle detector with 35 m long CAT5 cables. A fast analog-to-digital converter (FADC) system digitize the signals, and the digital data is read out via custom PCI link boards to PCs. Data sparsification, partial event building are performed by the PCs, and the data are transmitted to the Belle data acquisition system.

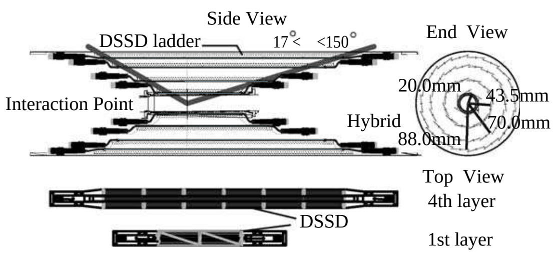

Fig. 1. Mechanical structure of the SVD2 detector.

Table 1
DSSD configuration for SVD2 and SVD3

	SVD2				SVD3	
Layer	1, 2, 3		4		1, 2	
Side	p(z)	n($r\phi$)	p(z)	n($r\phi$)	n(z)	p($r\phi$)
Thickness (mm)	0.3		0.3		0.3	
Strip length (mm)	25.6	76.8	33.3	73.8	26.1	77.7
No. of strips	1024	512	1024	512	1024	1024
Strip pitch (μm)	75	50	73	65	76	22.5
Readout pitch (μm)	150	50	146	65	152	51
Strip width (μm)	50	10	55	12	24	10

2.2. *Performance*

During three years of operation, the SVD2 has been operated well. The innermost layer has approximately 6.5 kGy radiation dose. Since this is small compared to the maximum exposure dose applied in the radiation test, no significant gain change for the VA1TA is observed due to radiation damage. The signal-to-noise ratios (S/N) have been stable for the third and fourth layers, while the degradation of the first and second layers has been about 20 %. This degradation is mostly due to an increasing shot noise accompanied by an increased leakage current.

The offline analysis shows good matching efficiency of about 98 % which is defined by the probability that the tracks reconstructed in the drift chamber can be extrapolated to the hits in the vertex detector. The typical trigger rate is about 400 Hz and the average detector occupancy is around 3 %, A considerably higher occupancy of 10 % is obtained in the first layer, drops to 3 % in second layer and to 2 % in the third and fourth layers. The situation of the beam-induced background is occasionally worth than the usual due to the troubles in KEKB such as the leakage of air into the vacuum chamber and so on.

Figure 2 shows the hit efficiency of the first layer as a function of its occupancy, it is obtained from collision data. Here, we require that both p and n sides of the detector have been hit. Almost 90 % detection efficiency is achieved for the first layer, and they are more than 90 % for outer three layers.

The impact parameter resolutions which obtained from cosmic ray data are $\sigma_{d(r\phi)} = 21.9 \oplus 35.5/(p\beta\sin^{3/2}\theta)$ (μm) and $\sigma_{dz} = 27.8 \oplus 31.9/(p\beta\sin^{5/2}\theta)$ (μm), where p is the track momentum in the unit of GeV/c and θ is the dip angle relative to the detector. Figure 3 shows the impact parameter resolutions in the $r\phi$-direction using μ pair events as a function of the first layer occupancy comparing the collision data with the Monte Carlo (MC) data. In the MC, DSSDs are assumed to be perfectly aligned.

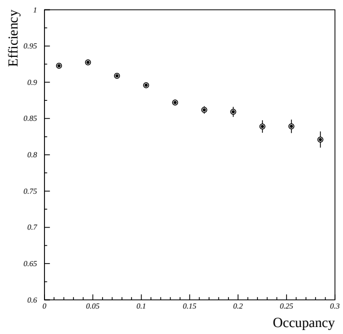

Fig. 2. Hit efficiency as a function of occupancy for the inner most layer of SVD2 using data in collision.

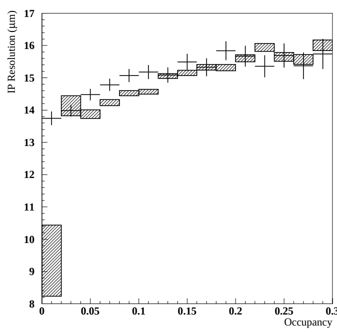

Fig. 3. Impact parameter resolution in $r\phi$ as a function of first layer occupancy using μ pair events. Crosses (boxes) indicate the collision data (Monte Carlo).

2.3. *Future prospects*

With improvement for the luminosity of the KEKB, the beam currents are also increasing gradually. In general, the higher beam currents gives the higher beam-induced background, i.e. the higher occupancy, as well as the higher luminosity. We roughly estimate to have 2 or 3 times higher beam-induced background than now within two or three years later. It corresponds to the cases of 20∼30 % occupancy for the first layer as in the Fig. 2 and 3, and about 10 % degradation of the performances is expected. For the case of the important physics, for example $B^0 \to J/\psi K_S$ decay, the MC predicts 17 % degradation for the decay vertex resolution; from 86 μm to 104 μm. It is worse than the requirements for the detector. To avoid such difficulties, we are planing a additional upgrade, SVD3.

3. SVD3

3.1. *Occupancy reduction*

The high occupancy in the first and second layers causes the performance degradation. Off-timing hits from the beam-induced background increase the occupancy. Readout with the fast shaping time is good solution for the occupancy reduction. By changing the readout chip from the VA1TA to APV25 (8), the SVD3 will realize the low occupancy condition.

The APV25 was developed for the CMS experiment at the LHC. Some nice features are implemented on this chip; an adjustable short shaping time of 50∼200 ns and a 192-cell deep pipeline for each of the 128 channels, where sampled values of the shaper output are stored at 40 MHz (the beam synchronous clock frequency of LHC). We do not use a "deconvolution" method (9), a switched capacitor filter on the chip with synchronizing the LHC bunch crossing timing, since the bunch crossing of the KEKB is almost quasi-continuous. However, the waveform sampling of the detector signal is enabled to readout multi samples of the shaper output spaced by the clock period of 25 ns ("multi-peak" mode).

The short shaping time of the APV25 will provide approximately 1/10 lower occupancy than the VA1TA case. One more order occupancy reduction can be possible with the multi-peak mode operation. About 2 ns of peak time resolution was confirmed by the beam test study using 4 GeV π^+ beam in KEK (10).

3.2. *Status of design and development*

The electric noise related with the detector capacitance ($\propto C/\sqrt{T_p}$) is serious when we use the APV25 chip, where, C is the detector capacitance and T_p is the peaking time. The S/N is 1/4 of current value if we use the same sensor as for the SVD2. Therefore, we developed new DSSD which is optimized for the APV25 readout. Its configuration and the comparison with the SVD2 are summarized in Table 1. To reduce the detector capacitance, the strip pitch or the strip width are modified to be half size. We obtained enough $S/N = 34$ from the beam test by using the prototype single-sided n-strip sensors. With scanning test with infrared laser (980 nm of wavelength) irradiation, we also confirm enough charge collection efficiency for the new DSSD (Fig. 4). Since three DSSDs are connected in a series for the third and fourth layers, the detector capacitance is still high even if we use the new DSSDs. Therefore, there is no modification for the third and fourth layers, i.e. we still use same DSSDs and VA1TA chips for outer two layers.

The FADC system for SVD3 is developed. It performs pedestal subtraction and sparsification as well as the digitization of incoming signal. The implementation of the peak time reconstruction algorithm in an FPGA on the FADC board is also discussed (10).

Since the APV25 chip is about 1 mm wider than the VA1TA chip, rearrangement of the hybrid board shape and the ladder structure is necessary. Width of the hybrid board is modified from 27 mm to 31 mm, and the hybrid board position in the second layer is moved 7 mm outside for the radial direction. We confirmed enough clearance for this new mechanical design based on the mock-up test. We are planning to construct new ladders within several months.

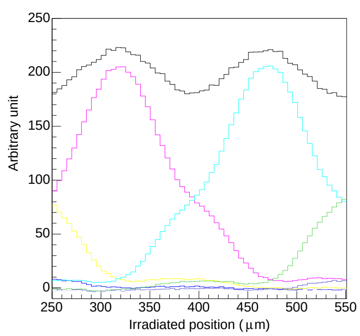

Fig. 4. Charge of readout signals for each strips and their sum as a function of irradiated position by infrared layer.

4. Summary

In summary, the SVD2 has been operated well during three years of operation. Its performance degradation is expected with increasing the beam-induced background. We are planing a next upgrade to avoid such a difficulty, and its design is almost finalized.

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