ALICE Silicon Pixel Detector (SPD)

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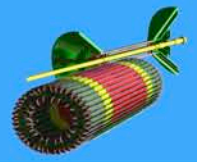
CERN-PH/ED

VERTEX 2006
CERN, Sept 25-29, 2006

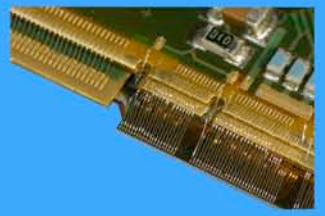
Overview

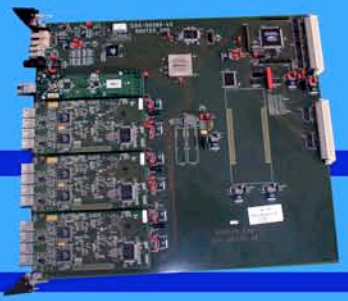
- **ALICE SPD**
  - Detector, Specification and Challenge



- **Components**
  - On detector
  - Off detector

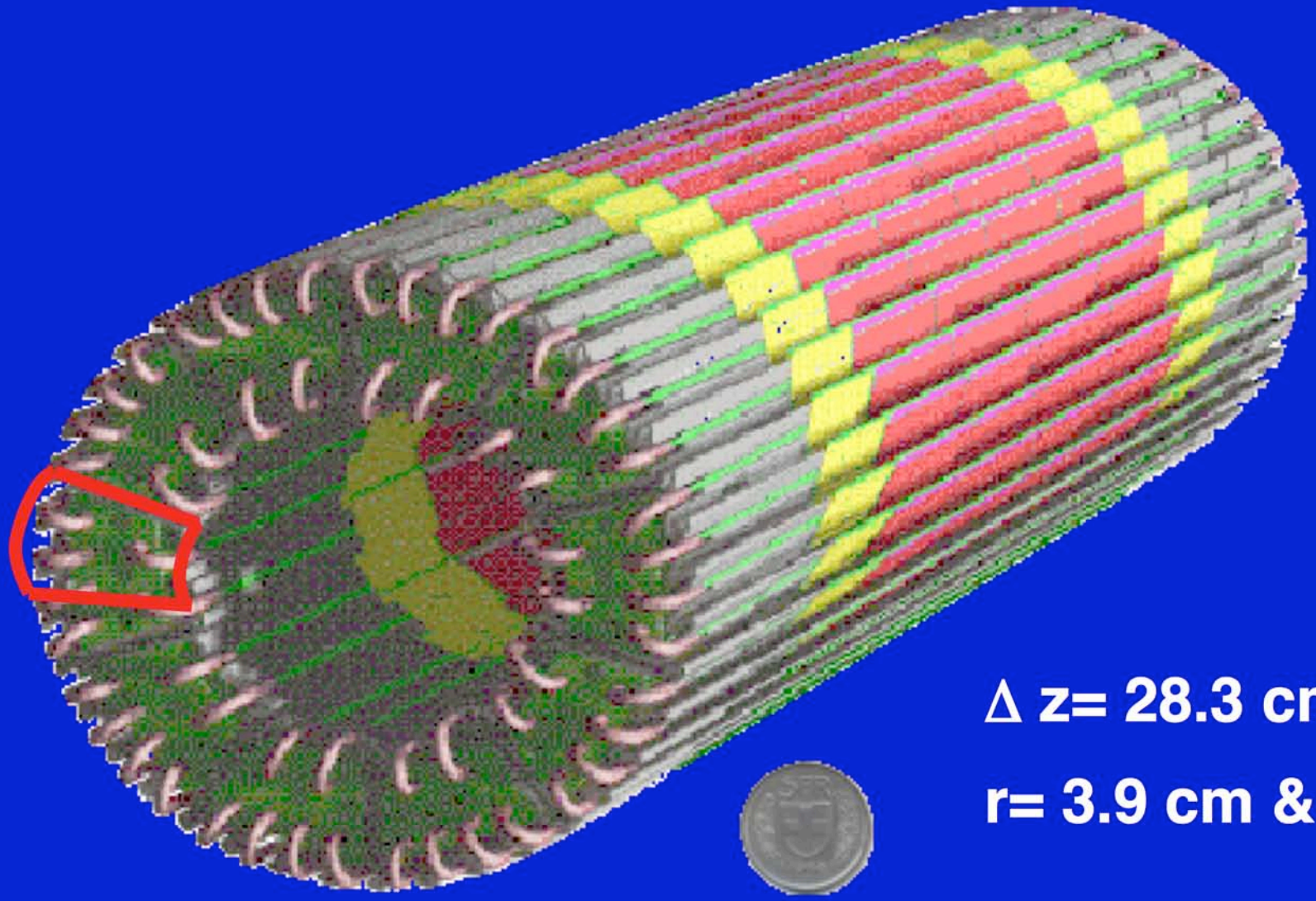
- **Status of**
  - Assembly
  - Integration
  - DAQ
  - Commissioning





- **Pixel trigger**
- **Conclusion**

The SPD Detector



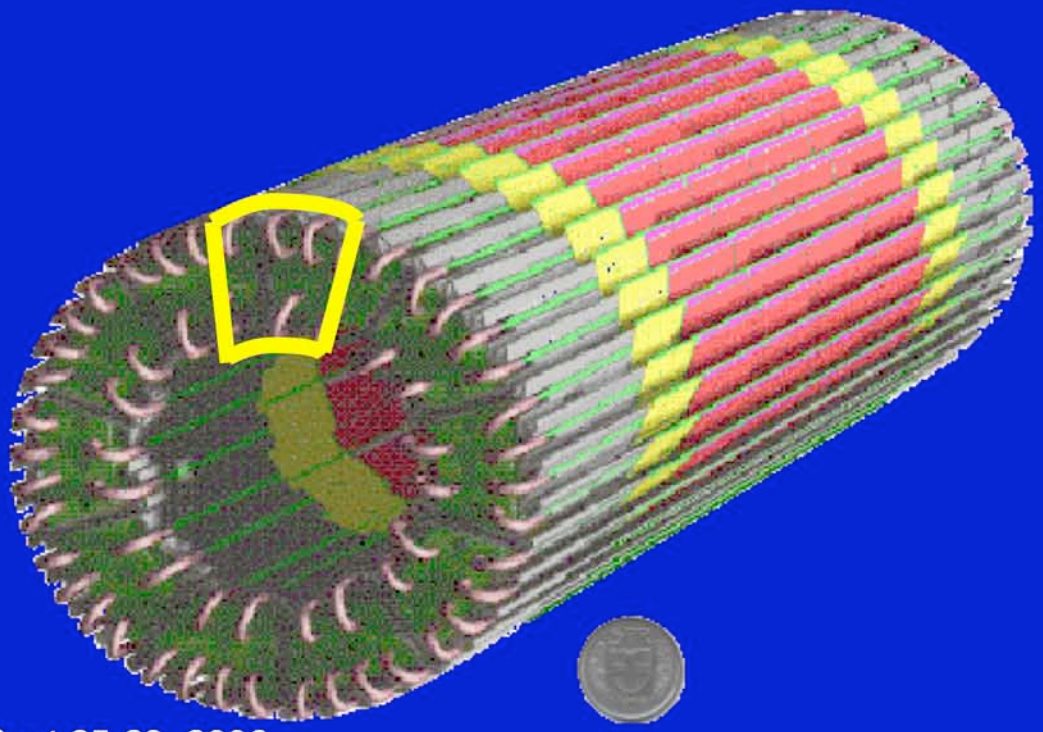
Δ z= 28.3 cm

r= 3.9 cm & 7.6 cm

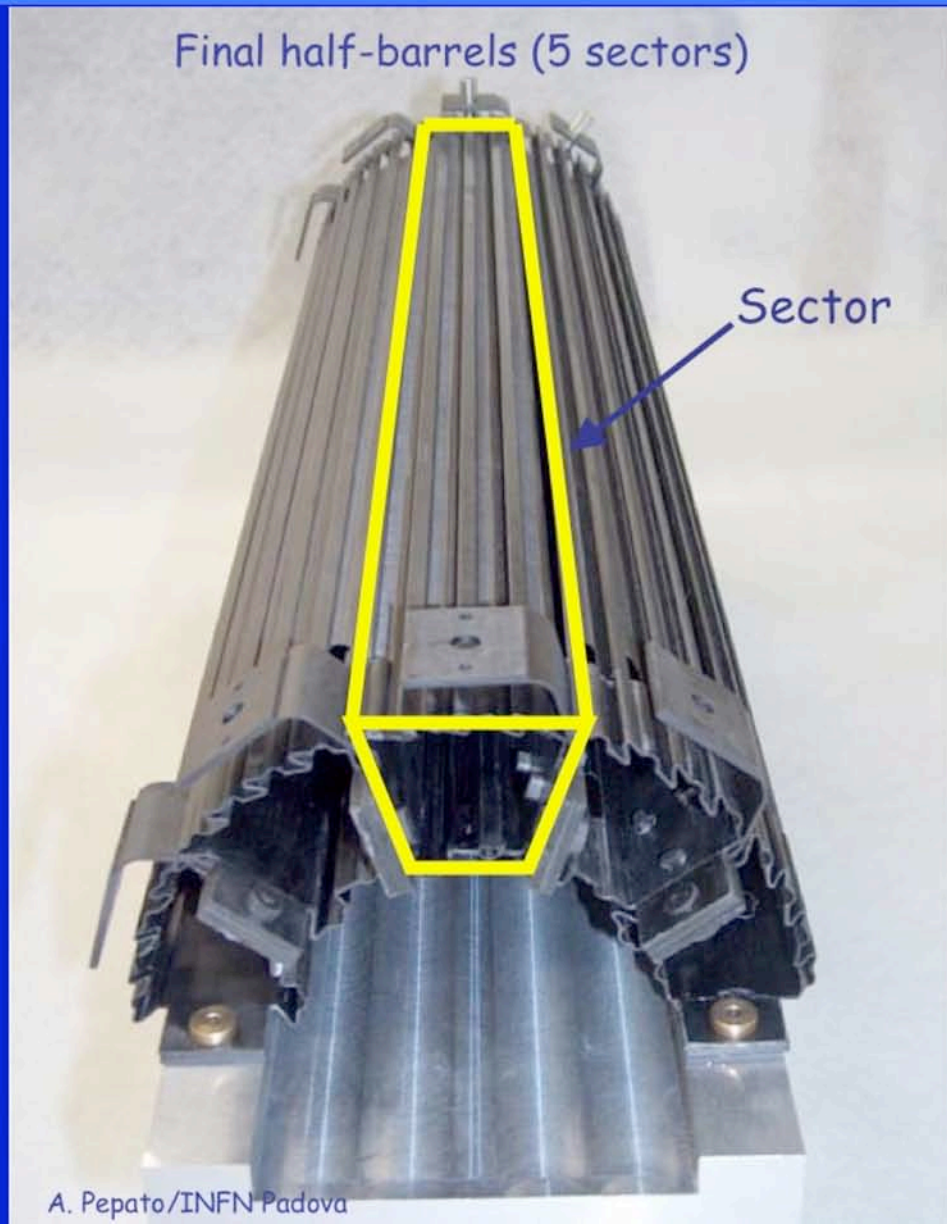
SPD carbon fiber support

200 μm carbon fiber support

40 μm PHYNOX cooling tubes integrated



Sept 25-29, 2006



The SPD half stave

physical size = 200 mm x 15 mm x 2 mm

material budget = 1% X_0 -> no copper

small quantities

cooling of 1kW

beam pipe dist. 4 mm

1 sensor

1 sensor

10 readout chips

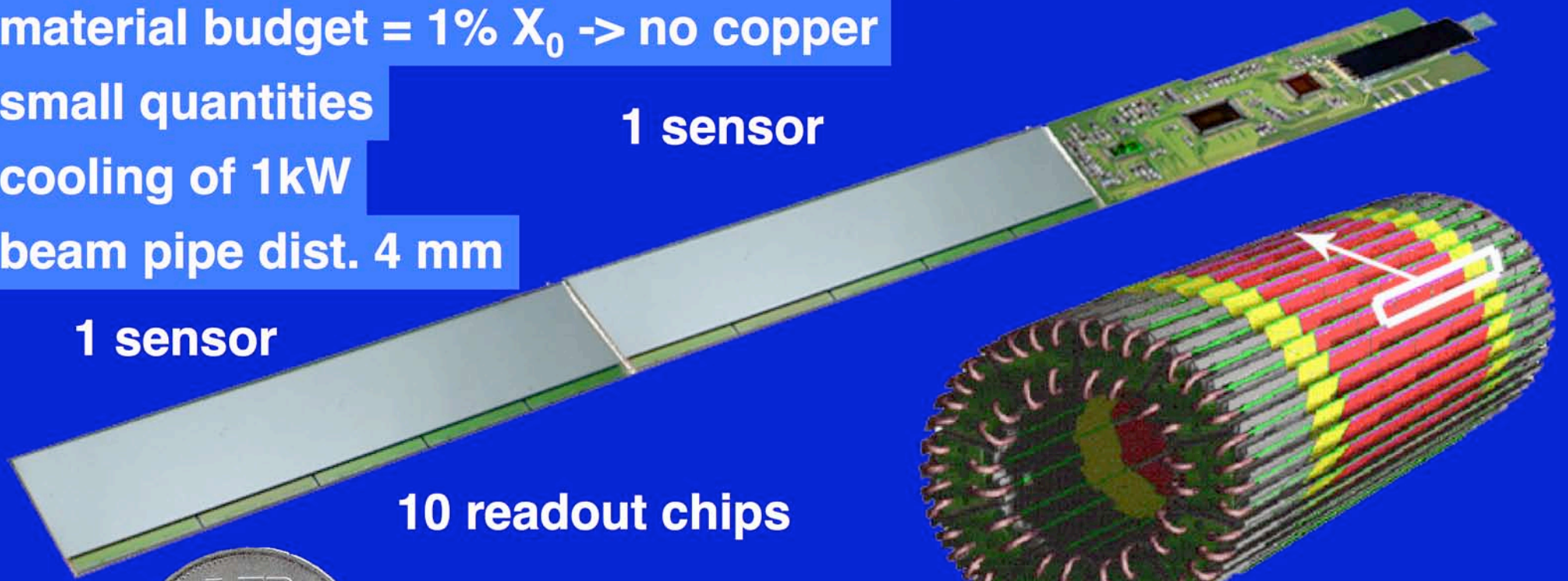


Image:INFN(Padova)

System parameters

System Parameters

- ~ 10 million channels in 1200 pixel chips
- 120 detector modules - half staves
- 10 sectors
- Two trigger levels: ~ 1 GB/s raw data
- Readout time: 256 μs
- Radiation: 250 krad
  neutron flux: $3 \times 10^{11} cm^{-2}$ (10y)
- Material budget: 1% X_0 per layer
- Power dissipation: 1kW (cooling C_4F_{10})
- Operation temperature: 24 °C

On-detector components

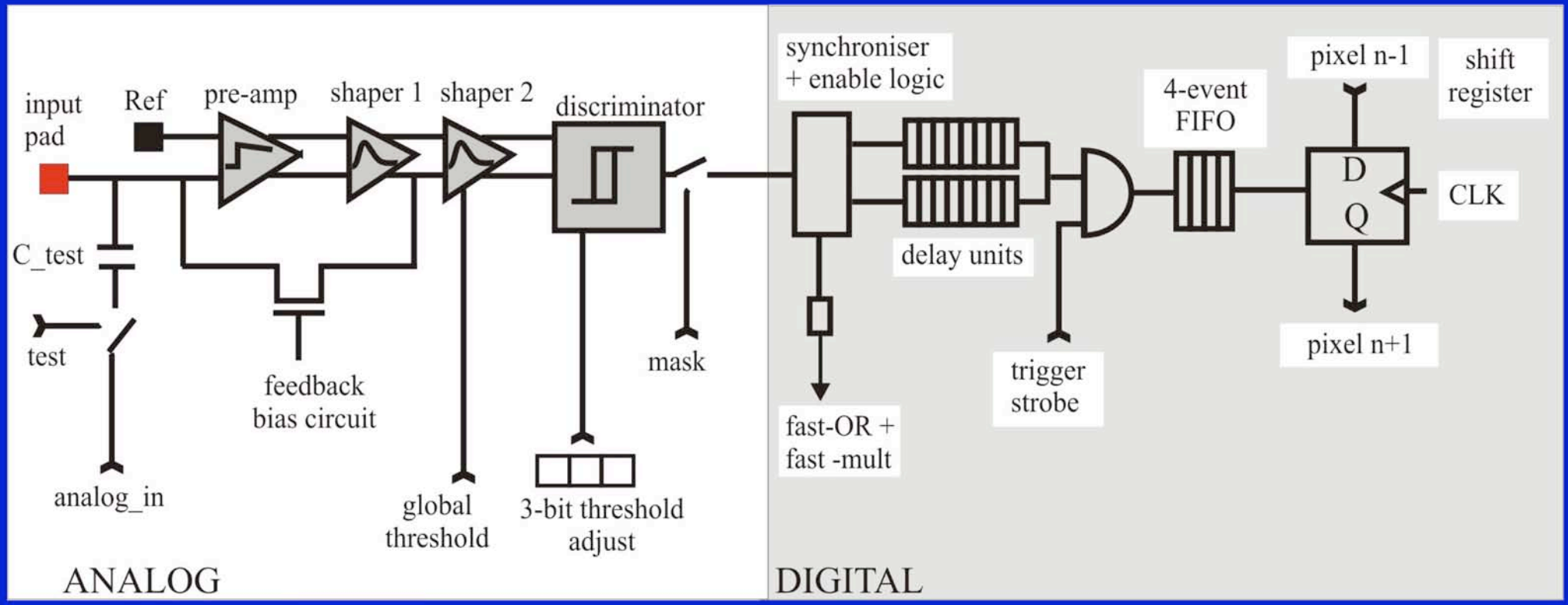
On detector electronics elements

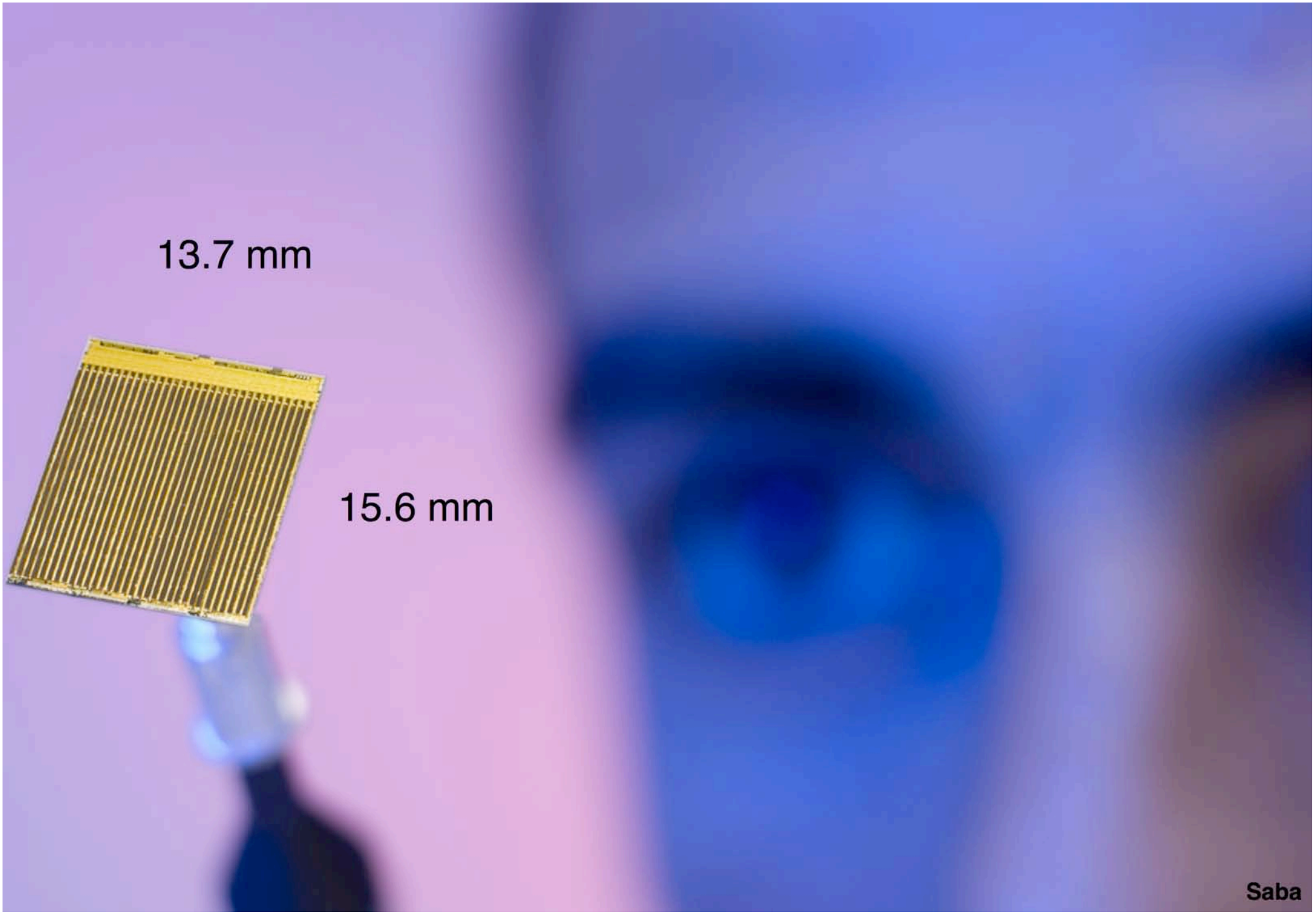
- Pixel chip & sensors
- Multi chip module + ASICs
- Al Multi-layer kapton cables (Bus)

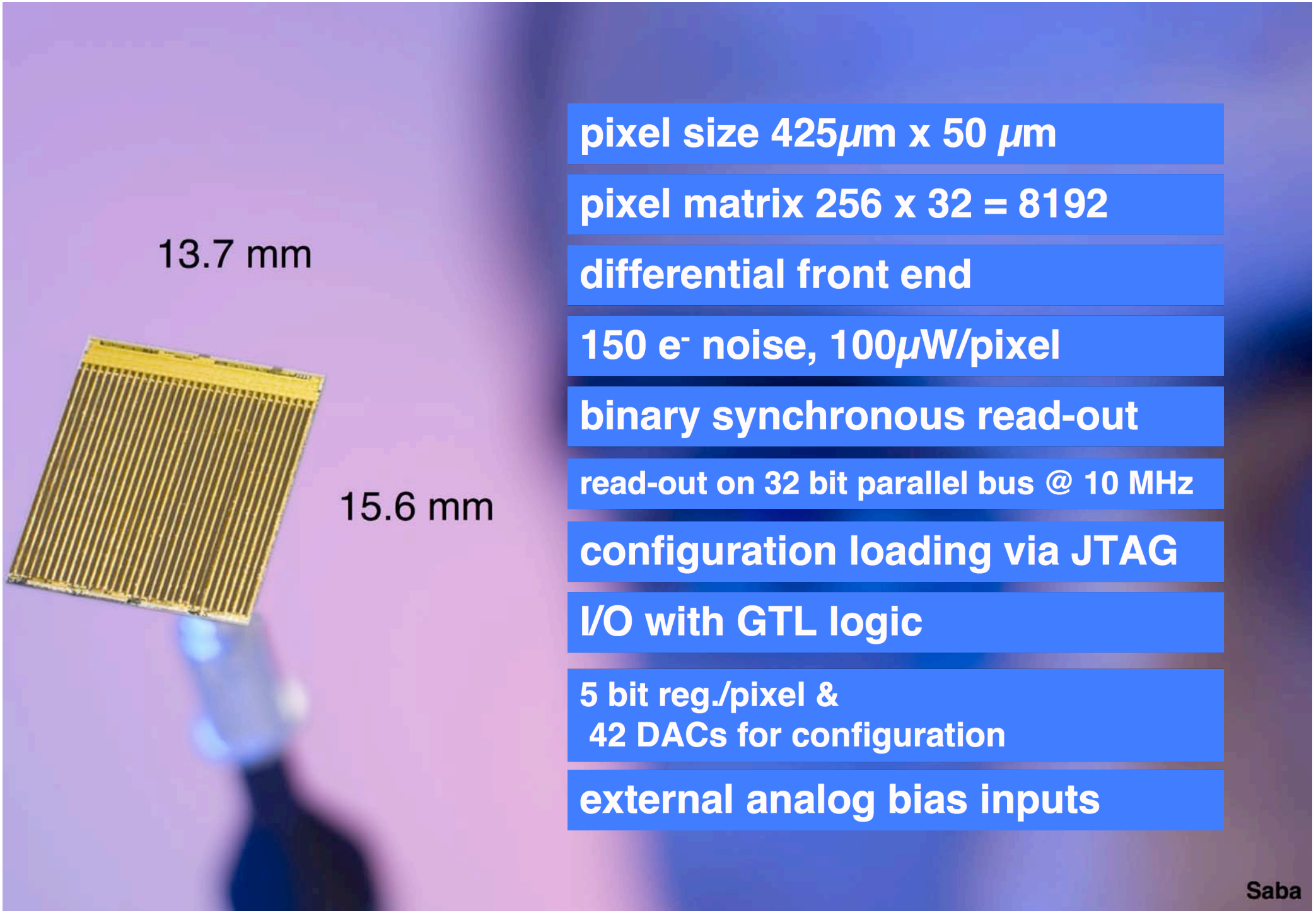
On detector electronics elements

- **Pixel chip & sensors**
- **Multi chip module + ASICs**
- **Al Multi-layer kapton cables (Bus)**

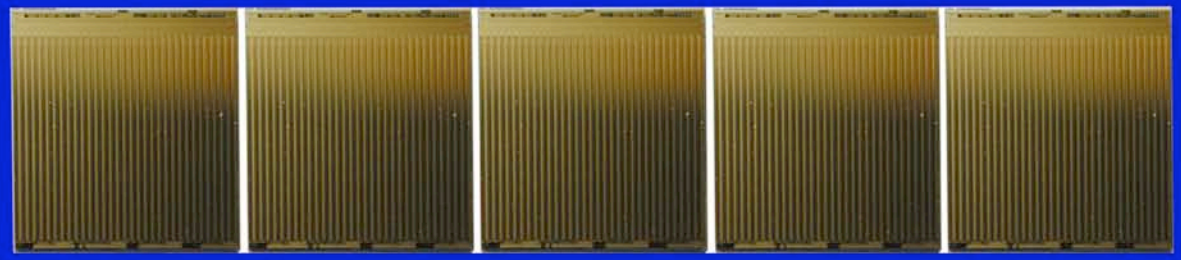
Pixel chip


input pad
Ref
pre-amp
shaper 1
shaper 2
discriminator
C_test
test
analog_in
feedback bias circuit
global threshold
3-bit threshold adjust
mask
ANALOG
synchroniser + enable logic
delay units
fast-OR + fast -mult
trigger strobe
4-event FIFO
pixel n-1
shift register
D
Q
CLK
pixel n+1
DIGITAL


13.7 mm
15.6 mm
Saba

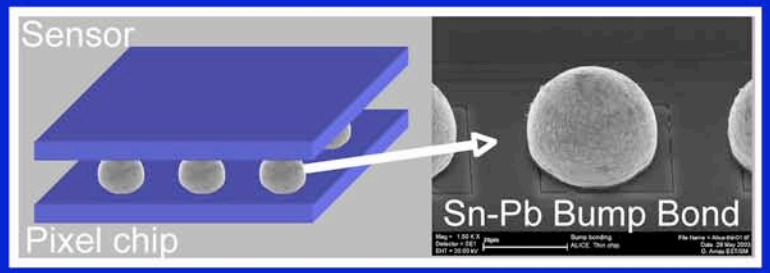

13.7 mm
15.6 mm
pixel size 425μm x 50 μm
pixel matrix 256 x 32 = 8192
differential front end
150 e- noise, 100μW/pixel
binary synchronous read-out
read-out on 32 bit parallel bus @ 10 MHz
configuration loading via JTAG
I/O with GTL logic
5 bit reg./pixel &
42 DACs for configuration
external analog bias inputs
Saba

Sensor & pixel chips



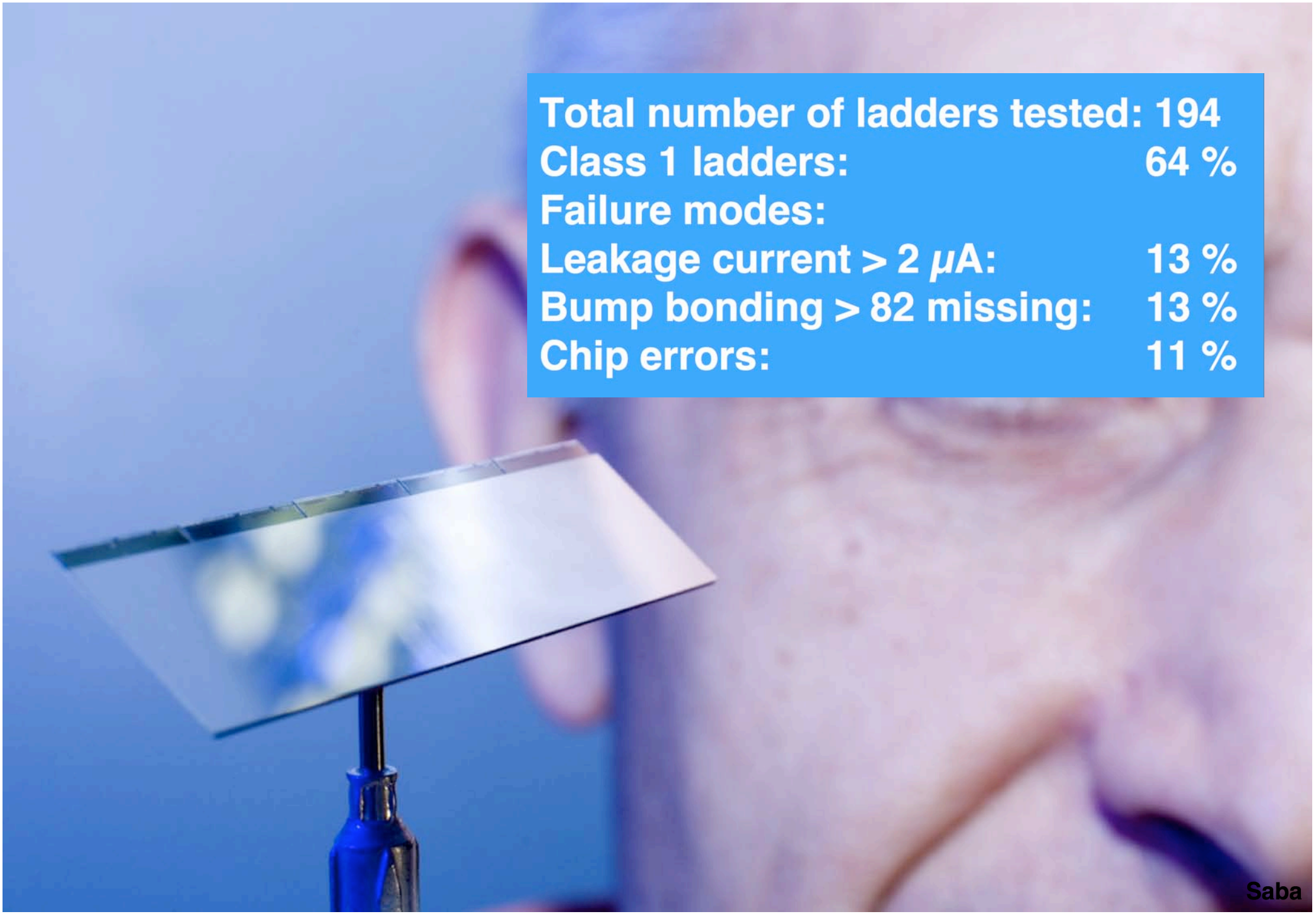
5 readout chips/sensor
0.25μm CMOS
13.68 mm x 15.58 mm
thinned to 150 μm

p-in-n silicon sensor
72.72 mm x 13.92 mm
200 μm thin

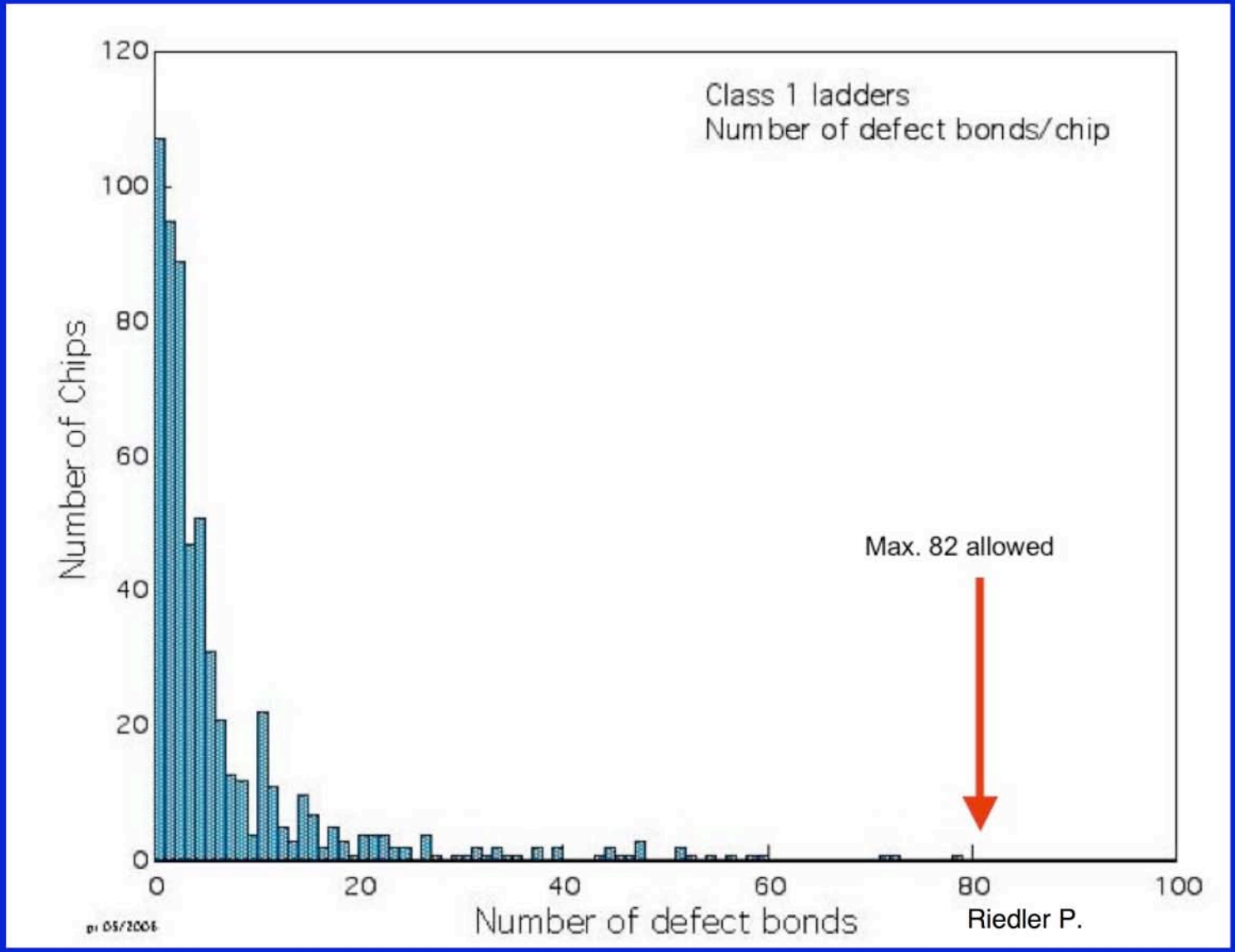


40960 bump bonds
~25 μm diameter
Stand-off:
~12 μm (Pb-Sn)


Saba


Total number of ladders tested: 194
Class 1 ladders: 64 %
Failure modes:
Leakage current > 2 μA: 13 %
Bump bonding > 82 missing: 13 %
Chip errors: 11 %
Saba

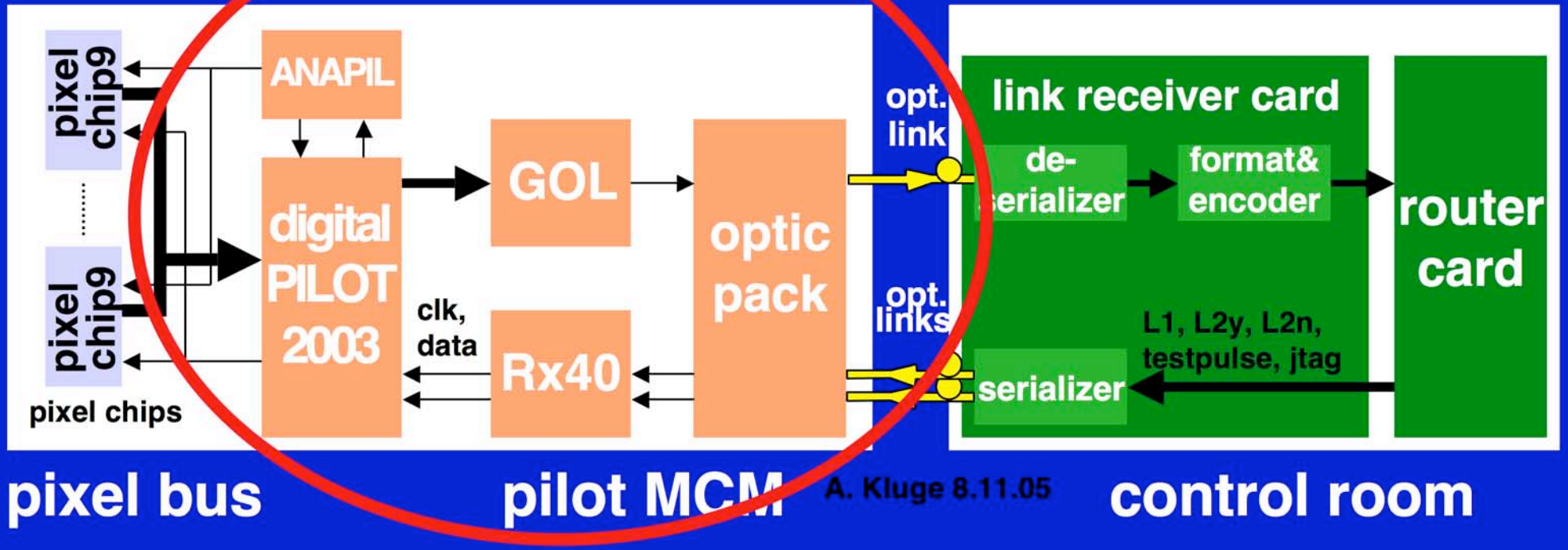
Sensor & pixel chips



On detector electronics elements

- The pixel chip & sensors
- Read-out Multi chip module + ASICs
- Al Multi-layer kapton cables (Bus)

Pixel read out system



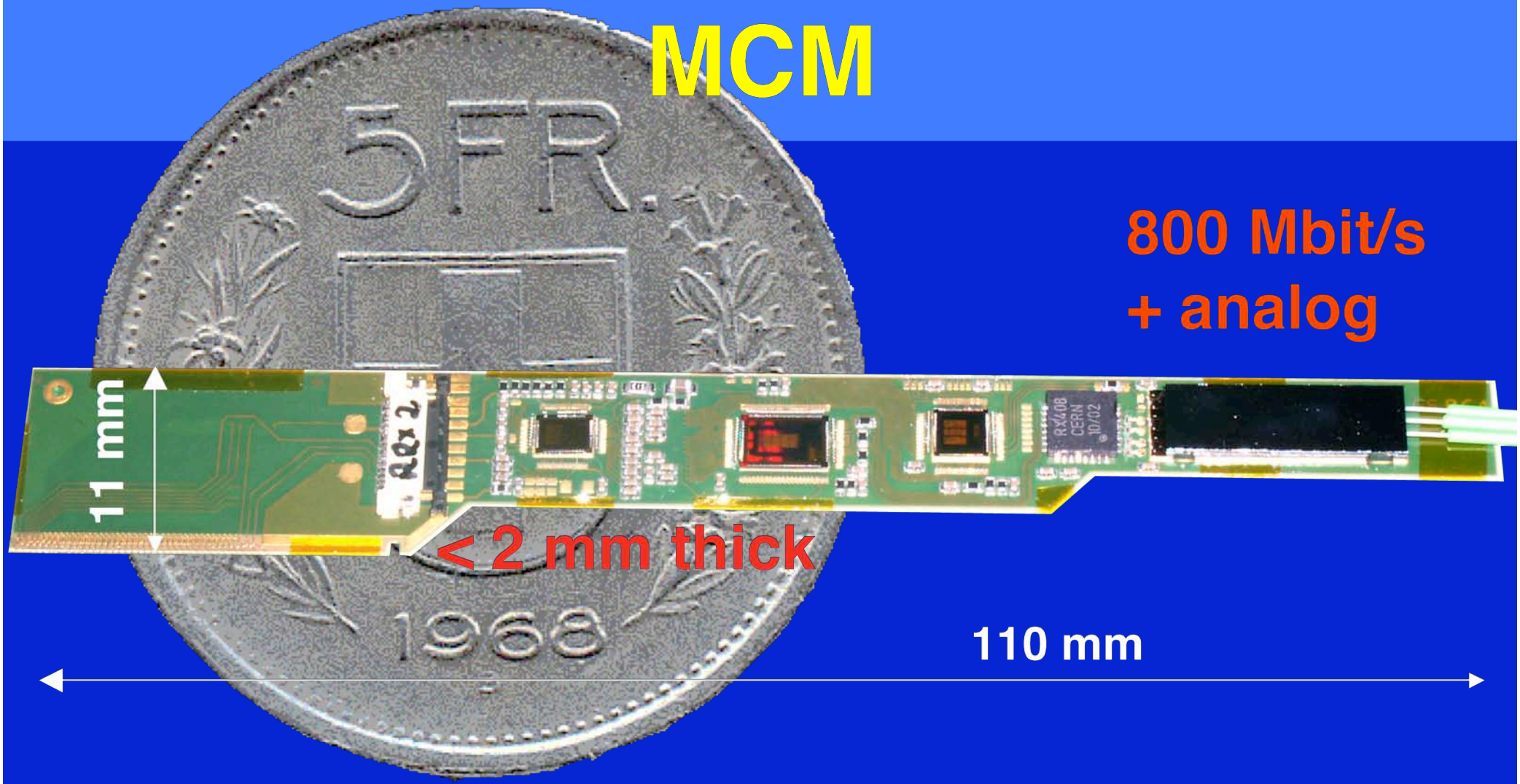
MCM

800 Mbit/s
+ analog

< 2 mm thick

110 mm

MCM



800 Mbit/s
+ analog

MCM

800 Mbit/s
+ analog

< 2 mm thick

110 mm

MCM

No Copper connections

No data processing, no memory

800 Mbit/s + analog

< 2 mm thick

110 mm

Analog (10mV) + digital (800Mbit/s)

Dense, comp. placement, routing

Fragile: thin, no packages

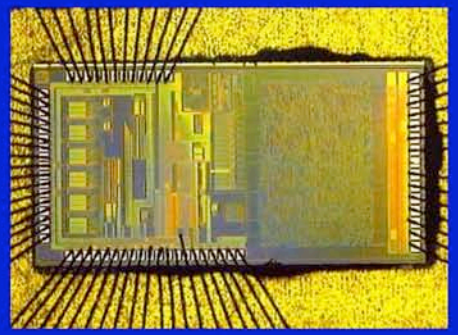
Small quantity

Small: limited reworking

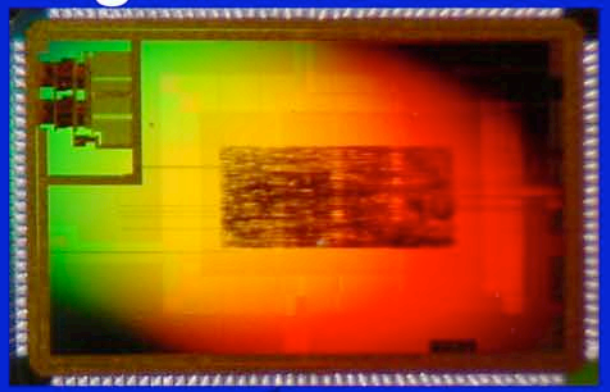
A. Kluge

Pilot MCM ASICs

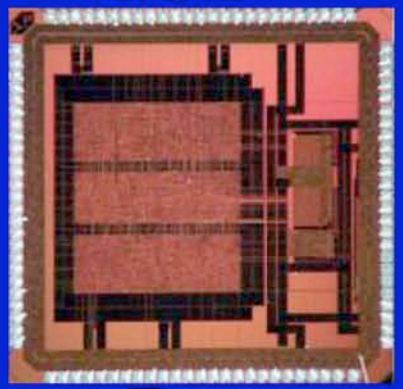
ANAPIL3



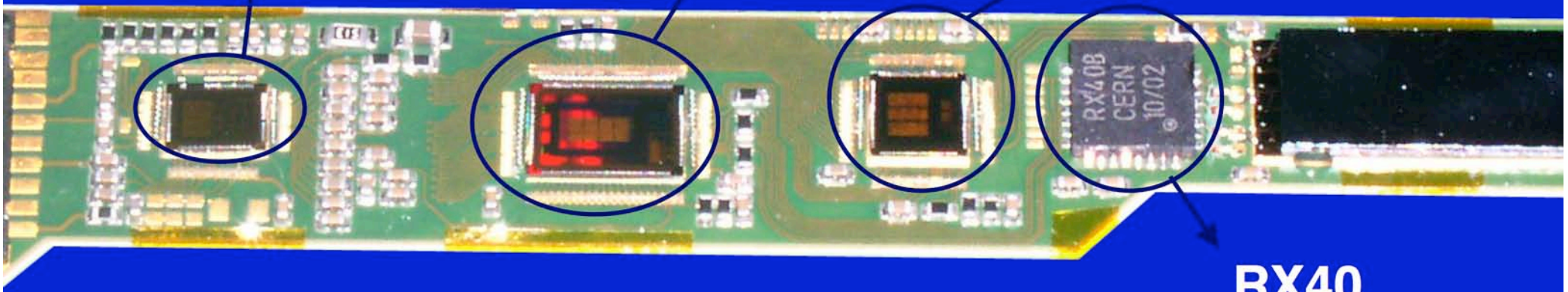
Digital Pilot 2003



GOL

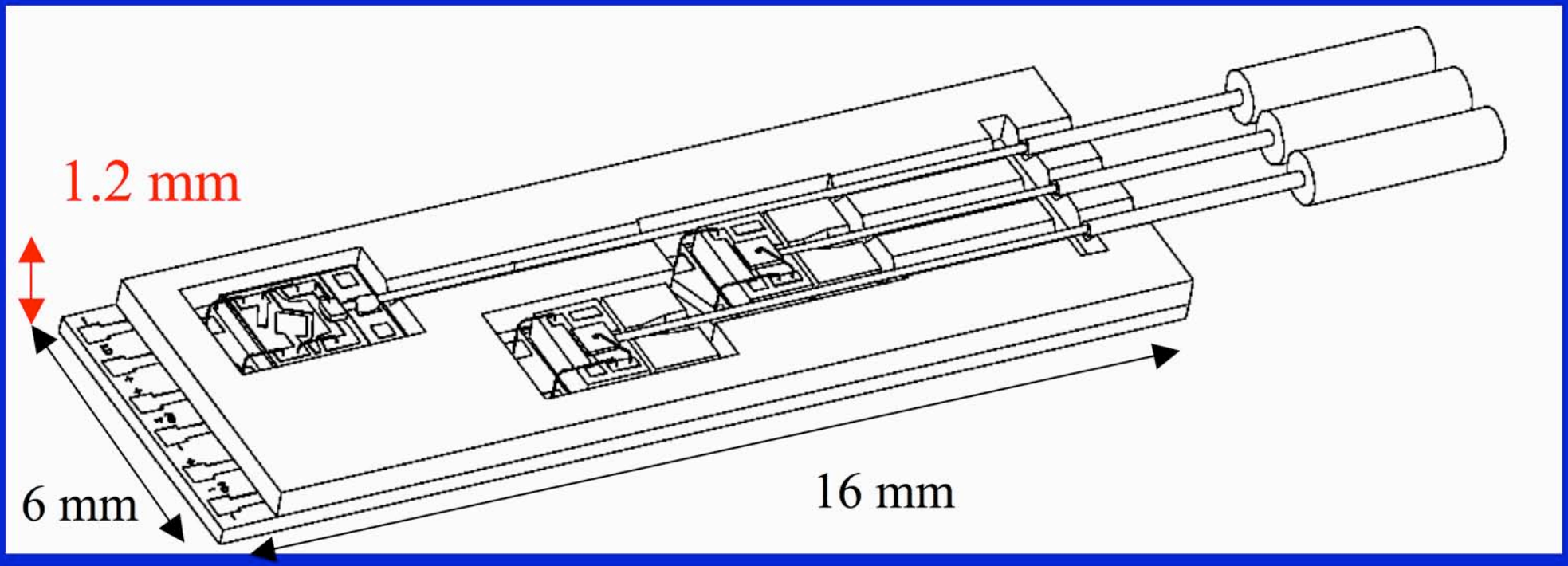


PILOT MCM



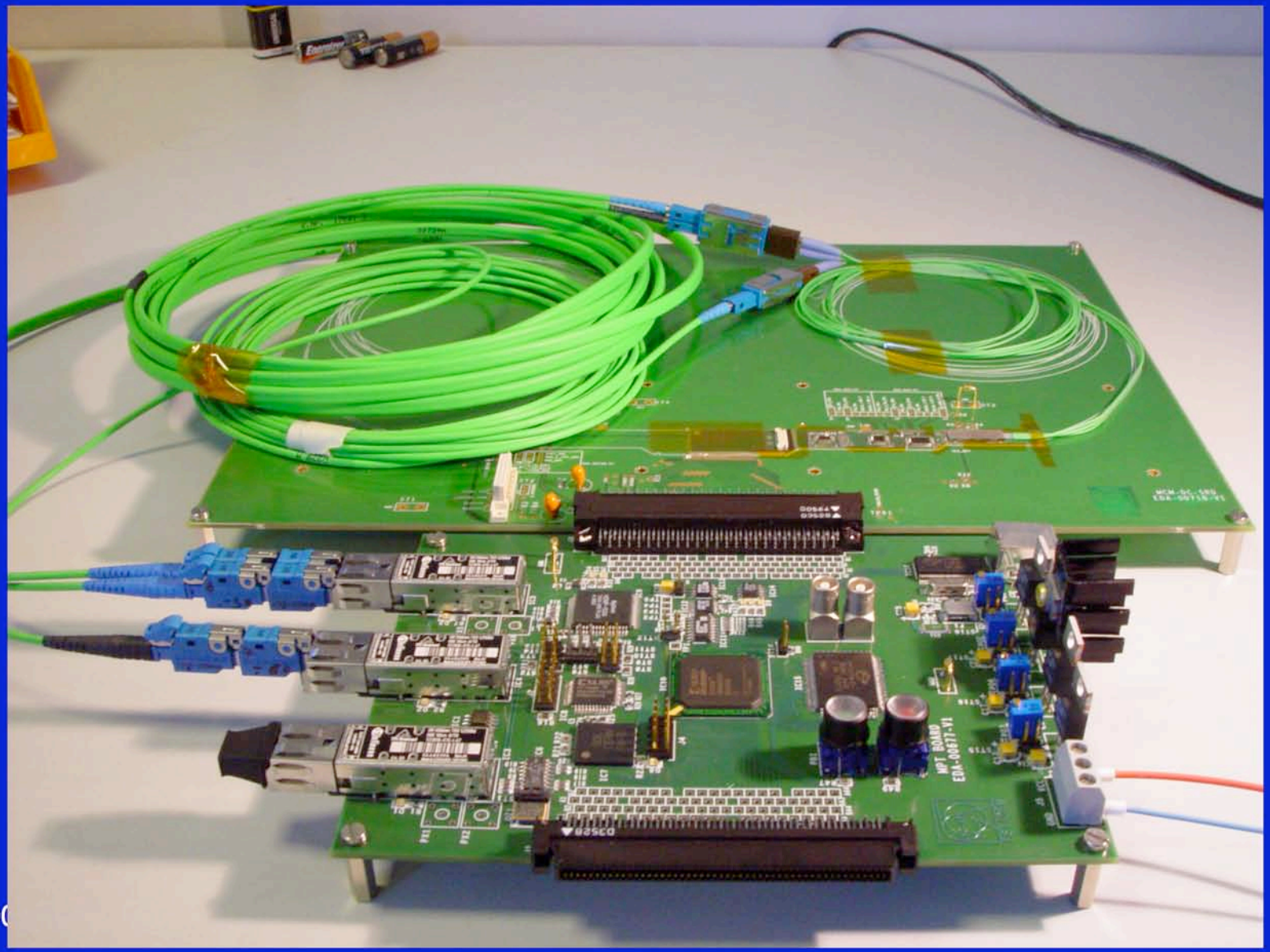
RX40

Pilot MCM Optical package

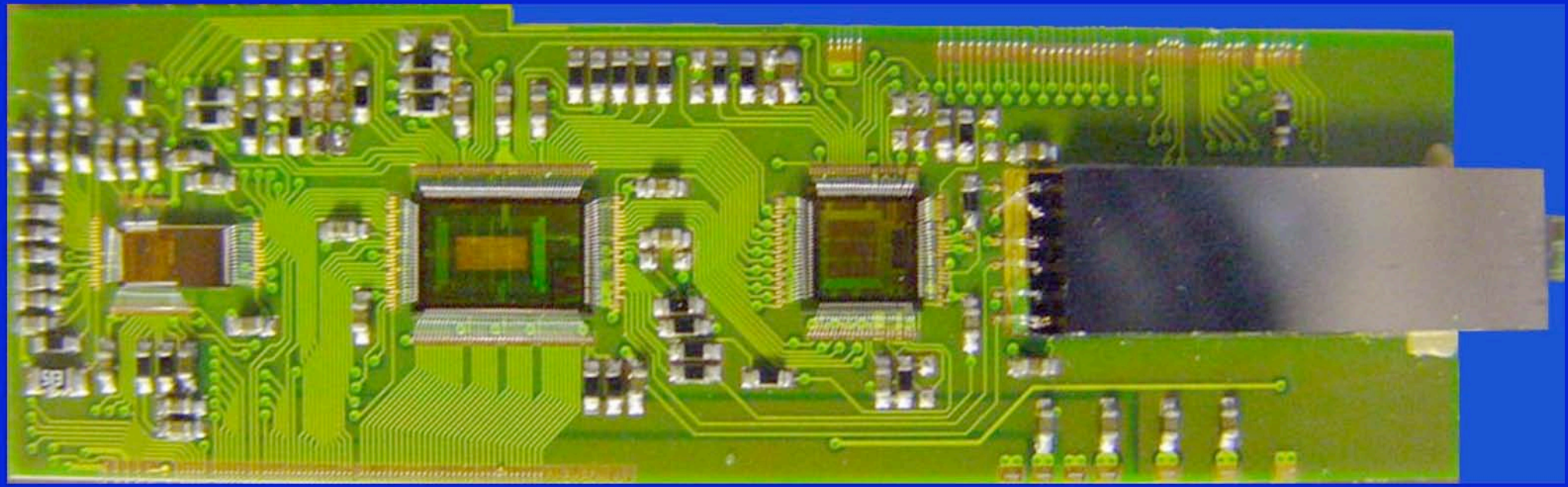


link has 15 dB input and output optical margin

MCM



Pilot MCM ASICs



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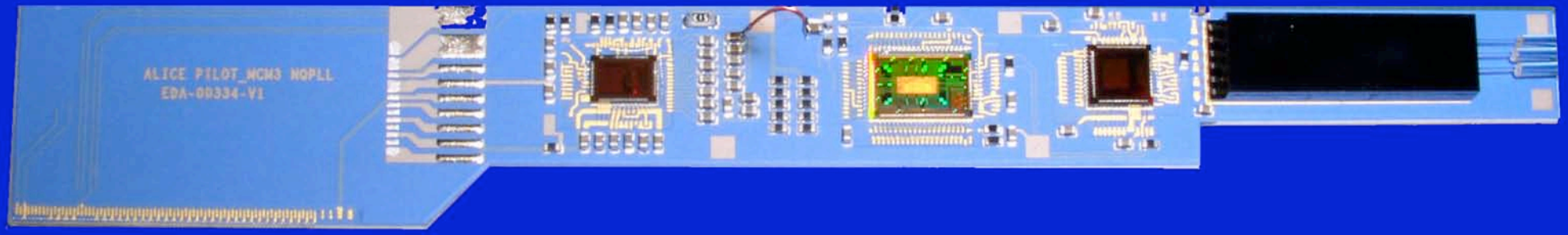
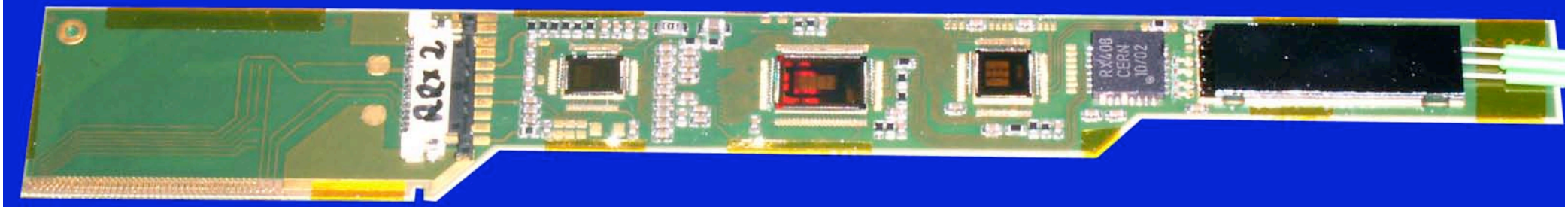
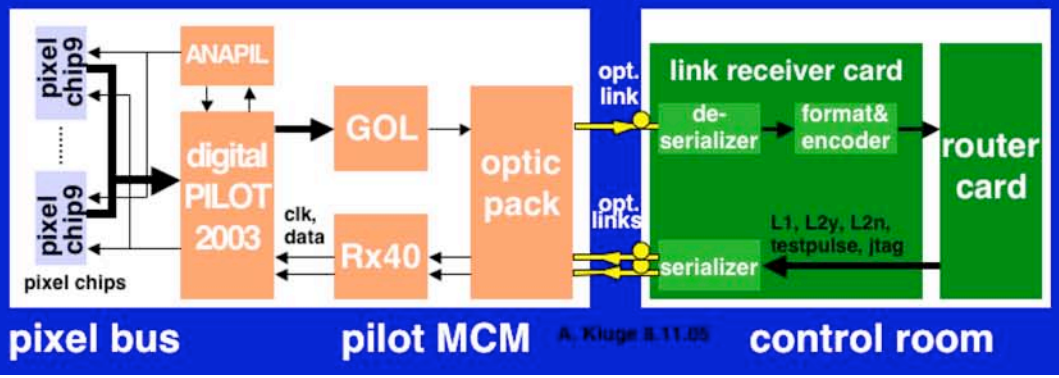


MCM



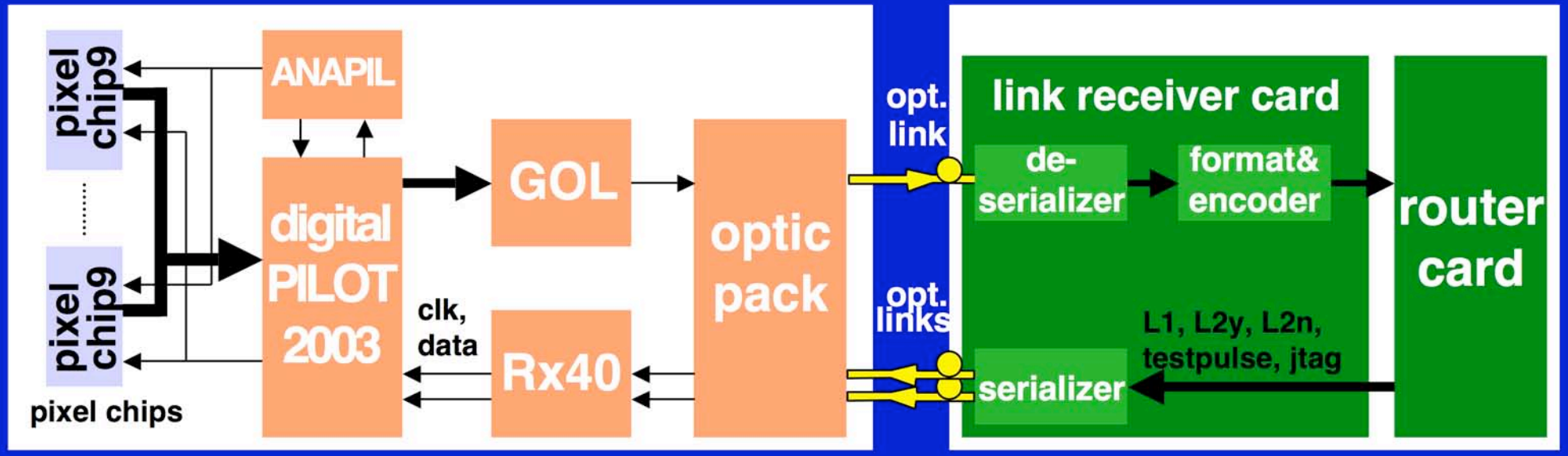
Complexity due to connectivity, limited space, number of signals (bus width, analog bias) and late integration design.



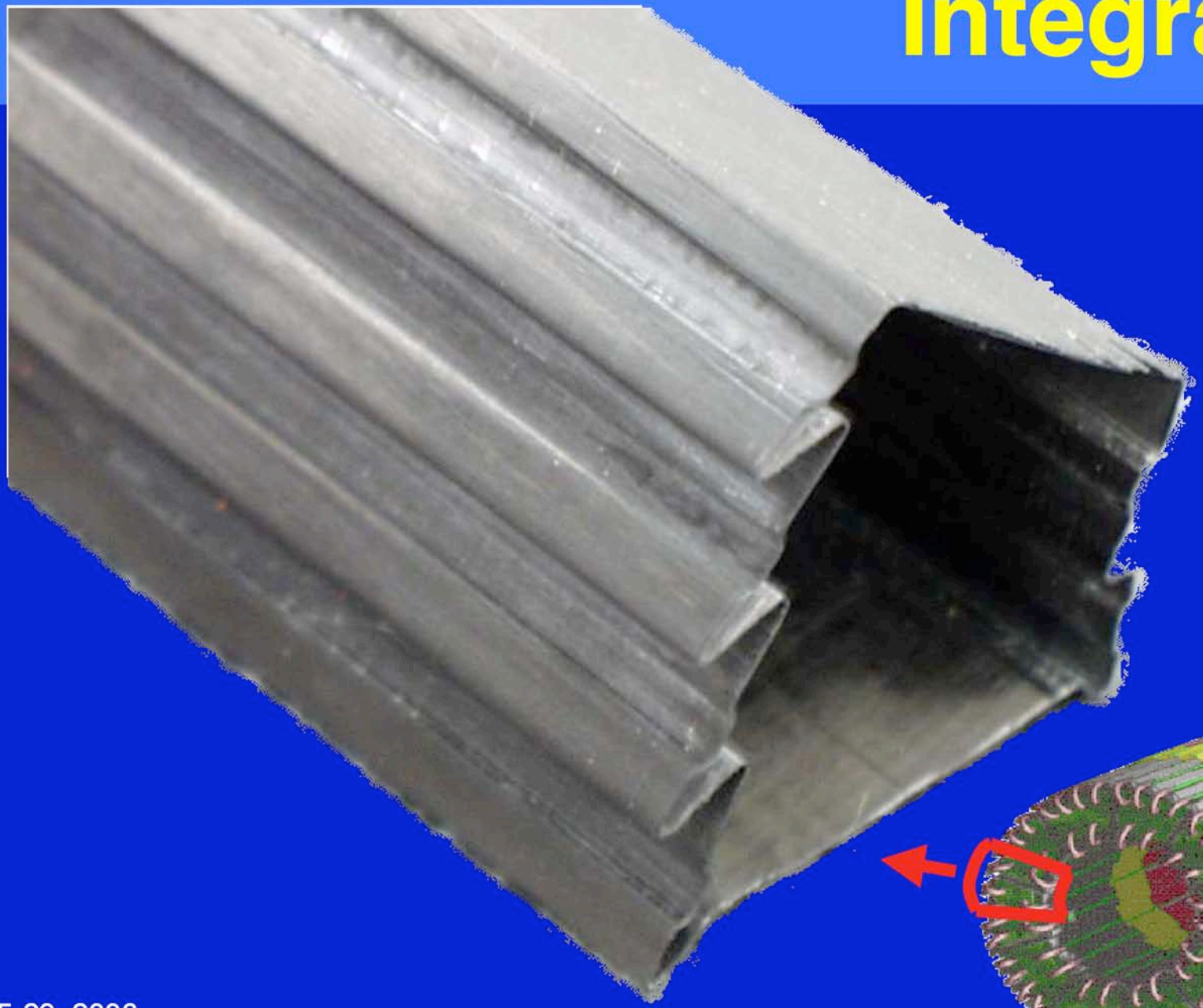
On detector electronics elements

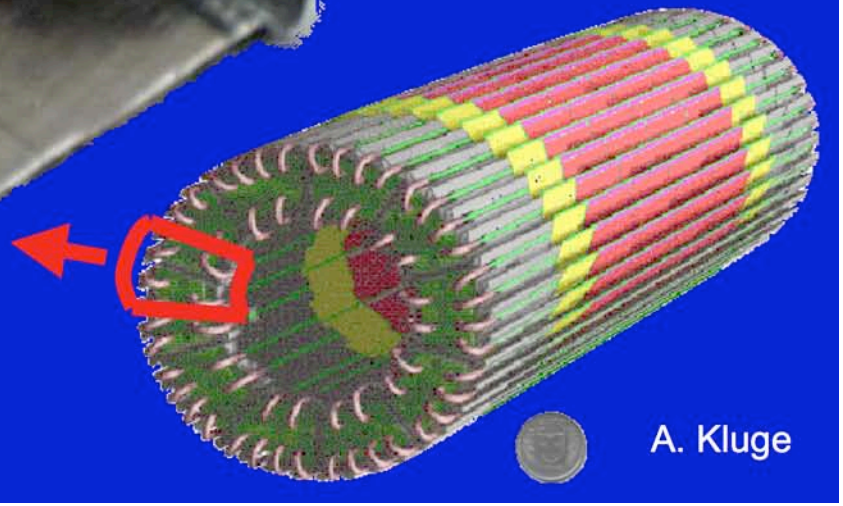
- The pixel chip & sensors
- Multi chip module + ASICs
- Al Multi-layer kapton cable (Bus)

Pixel read out system

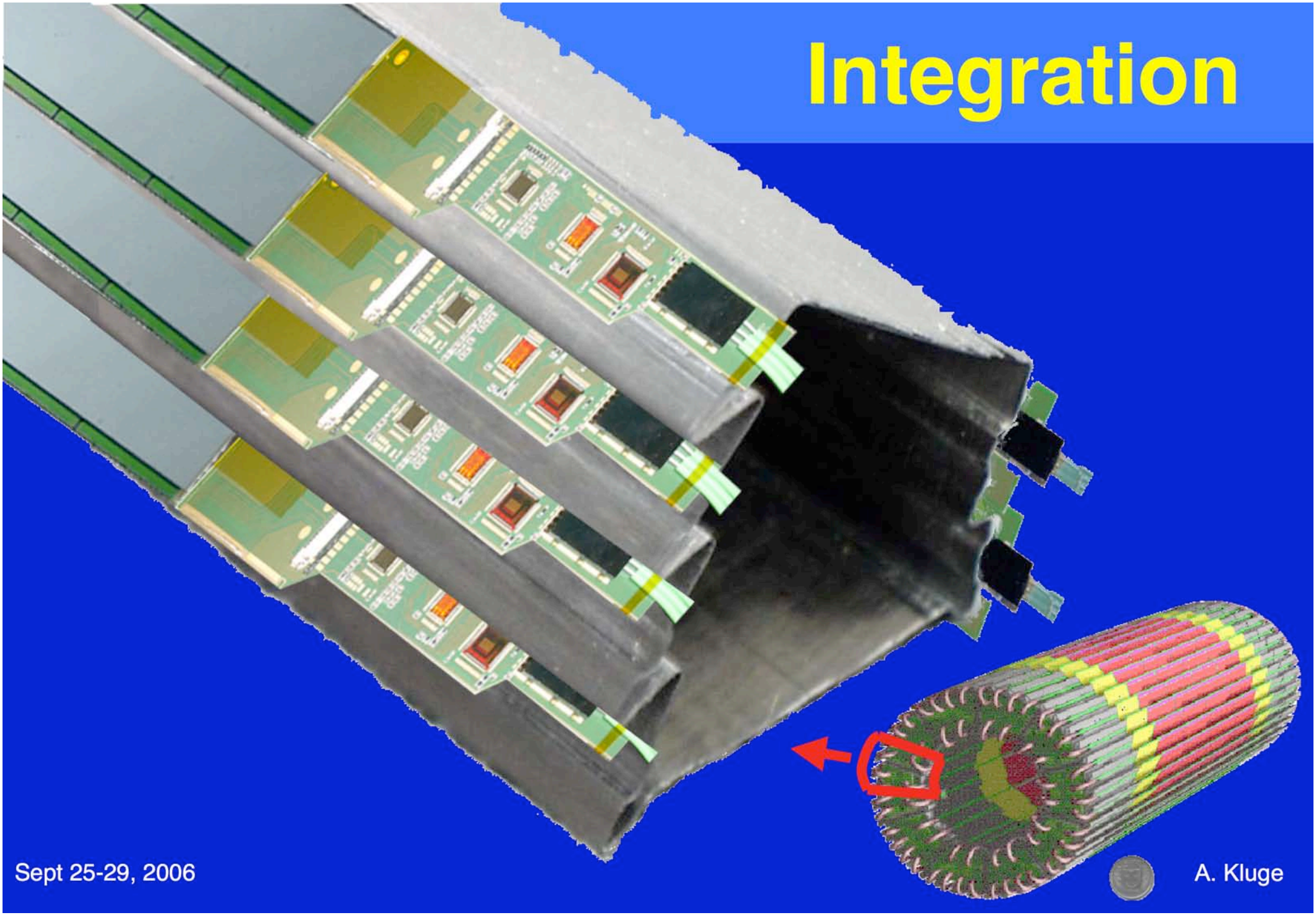


Integration

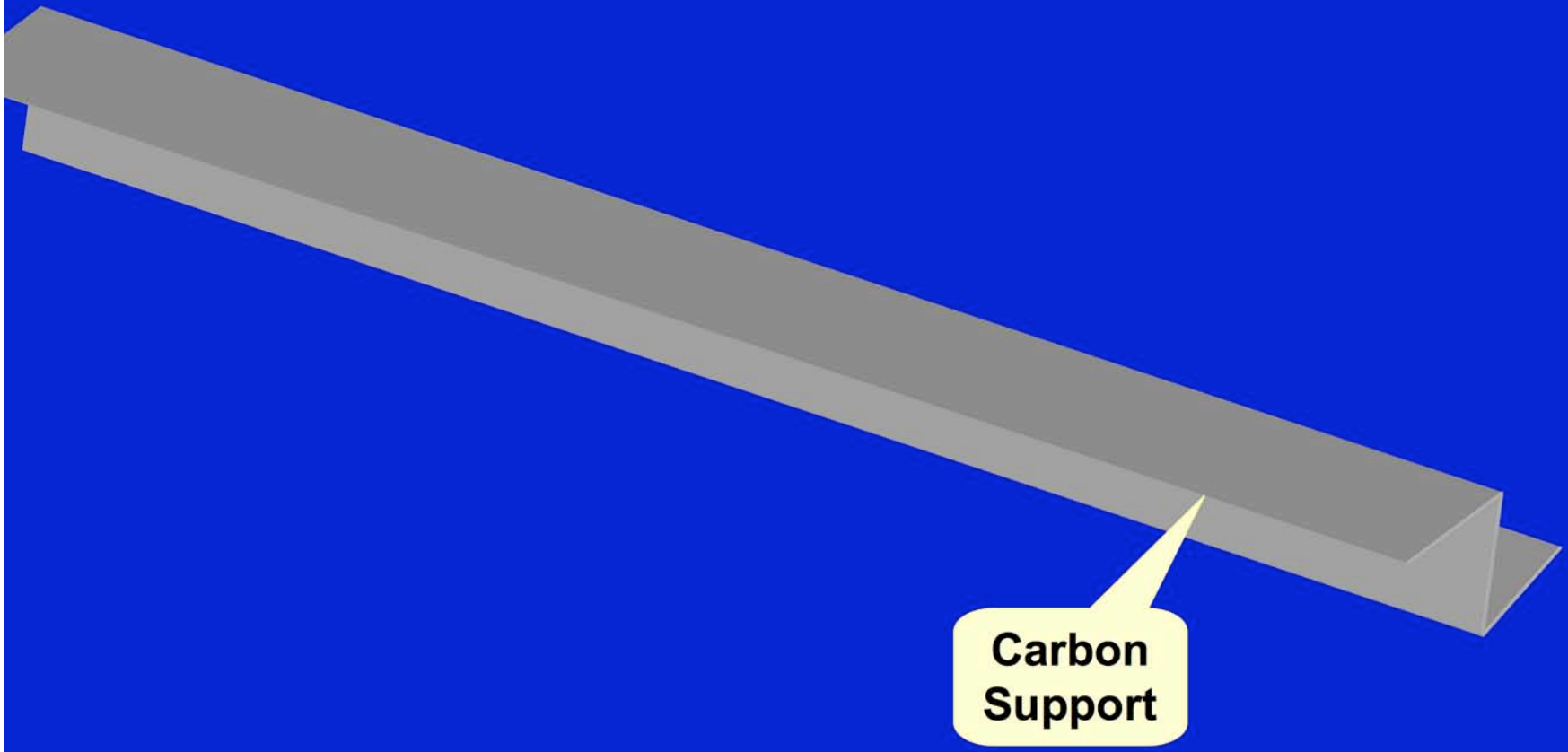




Integration



Electronics integration



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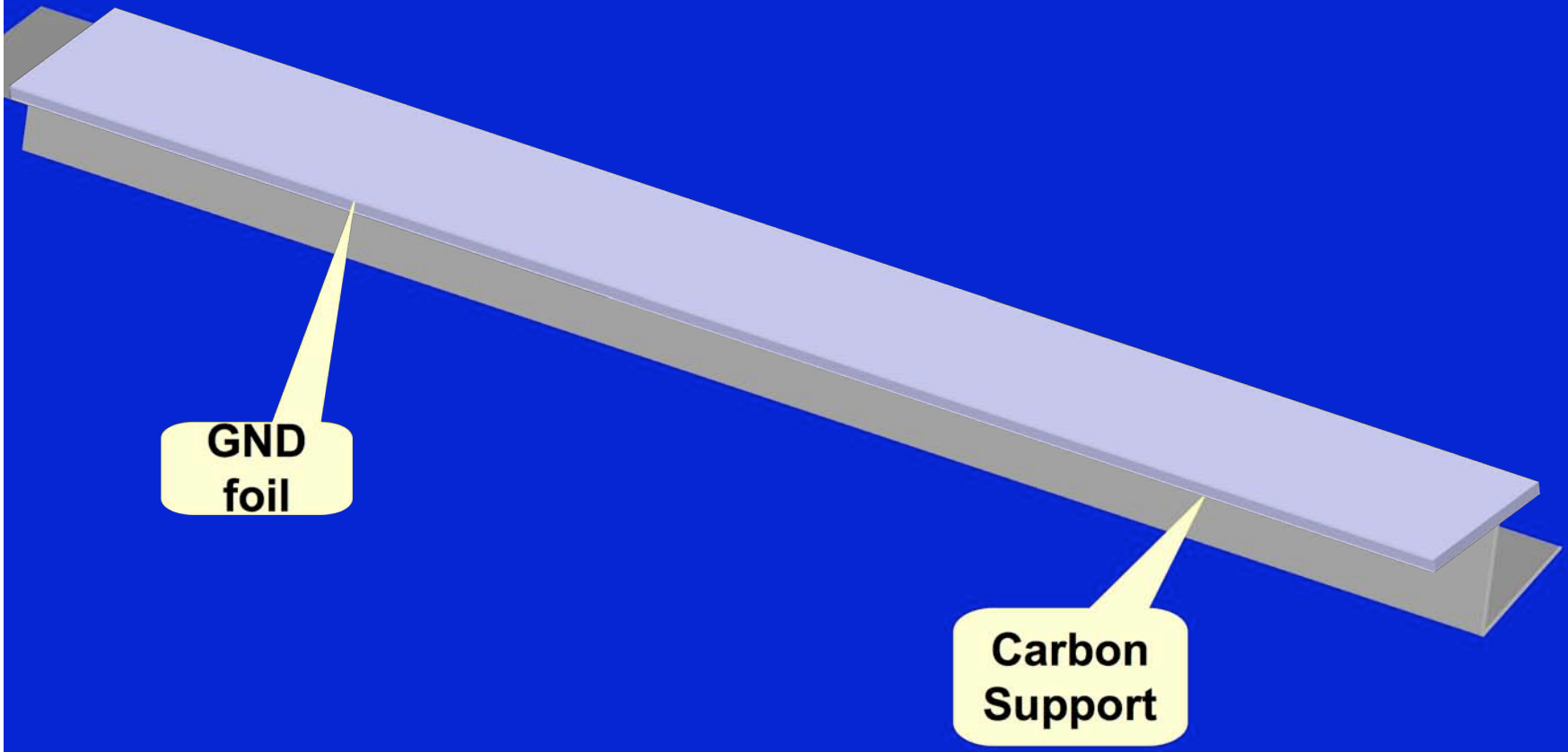

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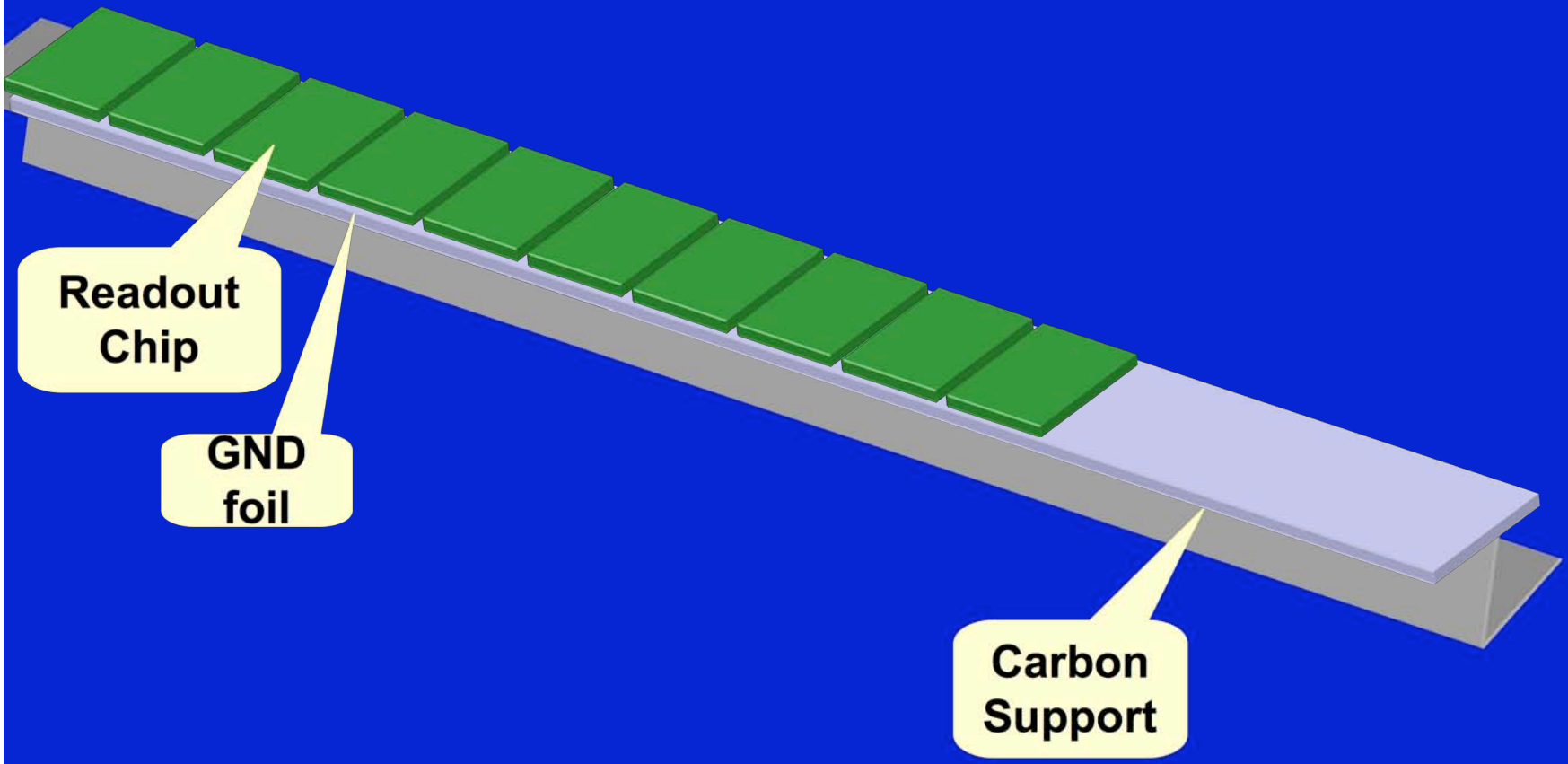

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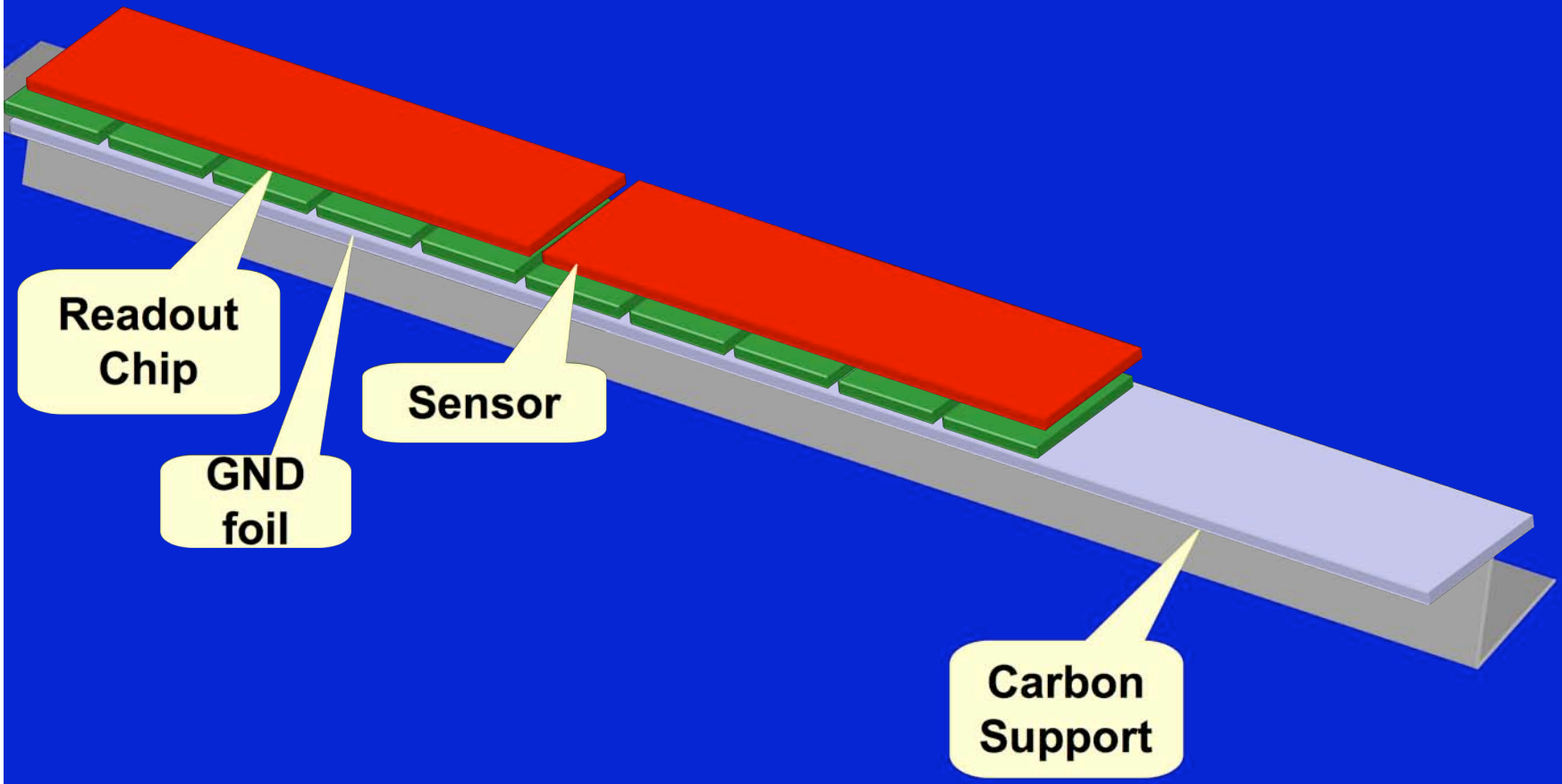
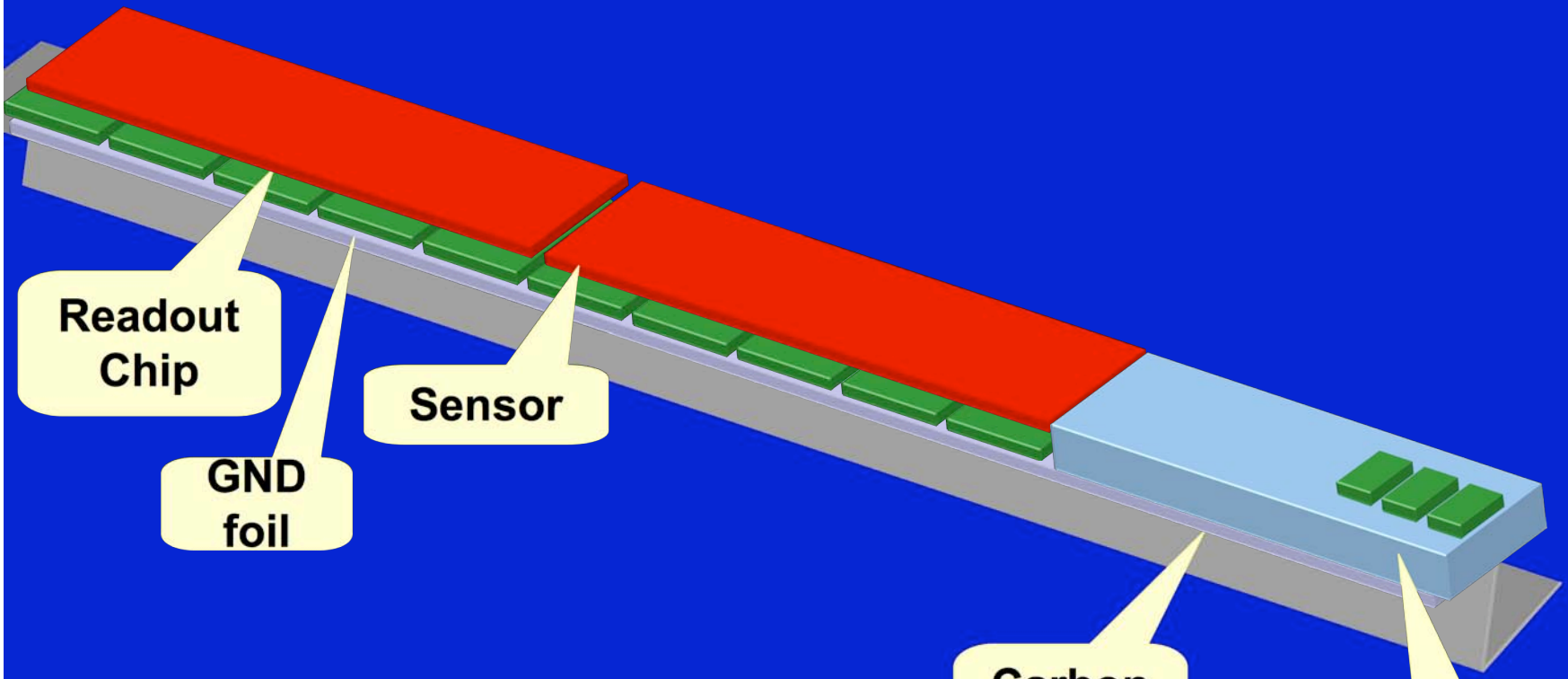


Electronics integration



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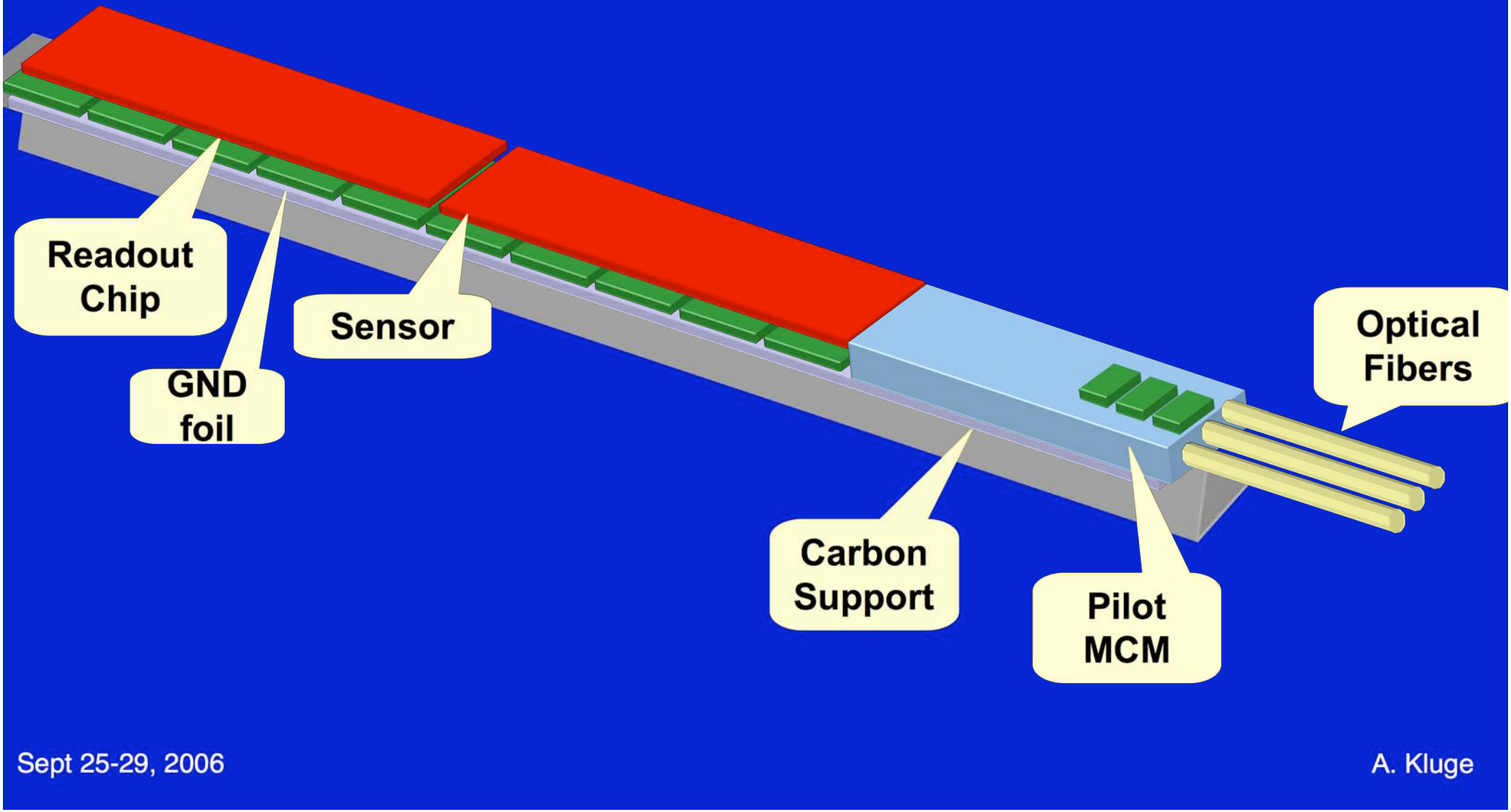

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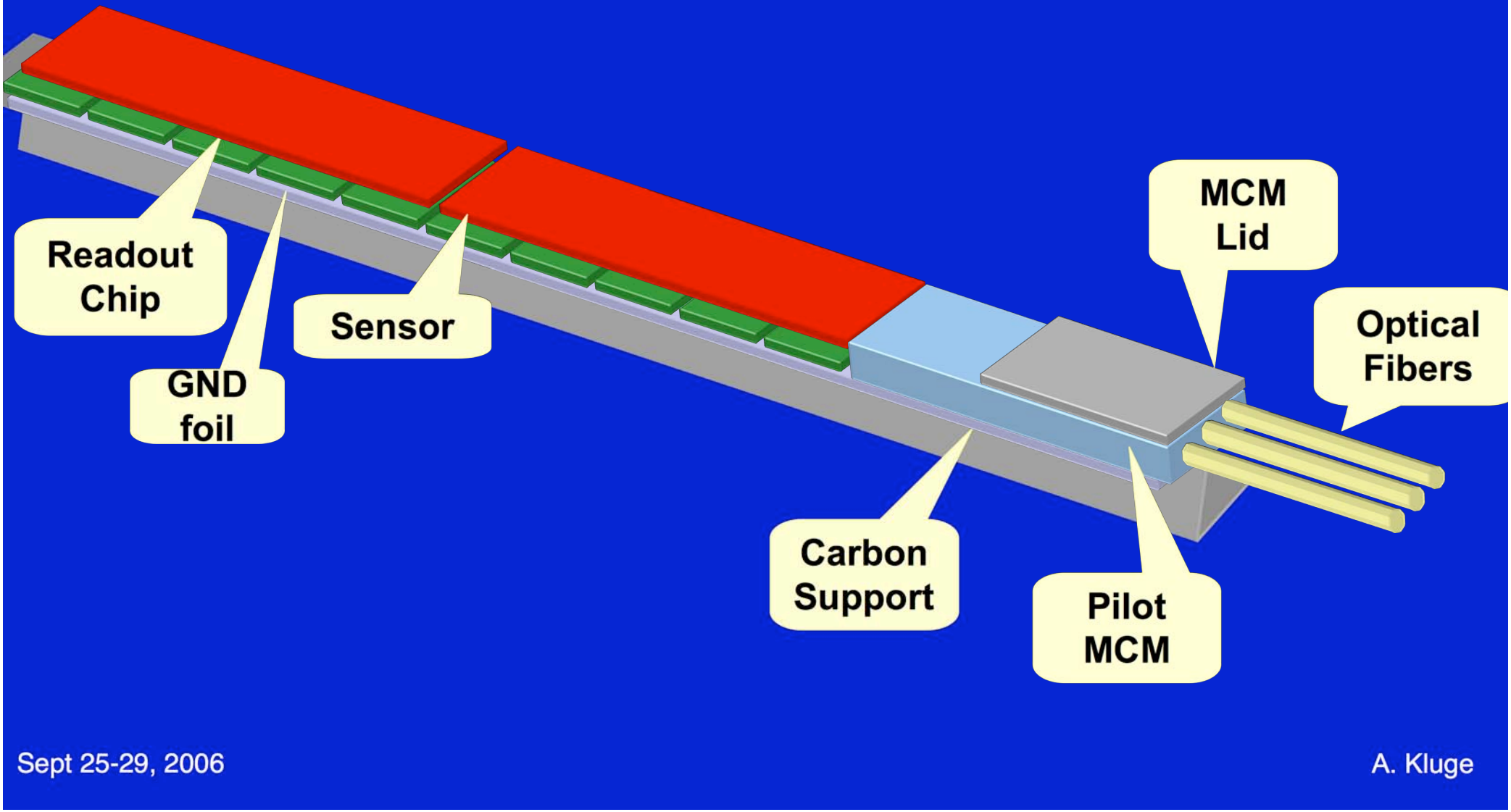
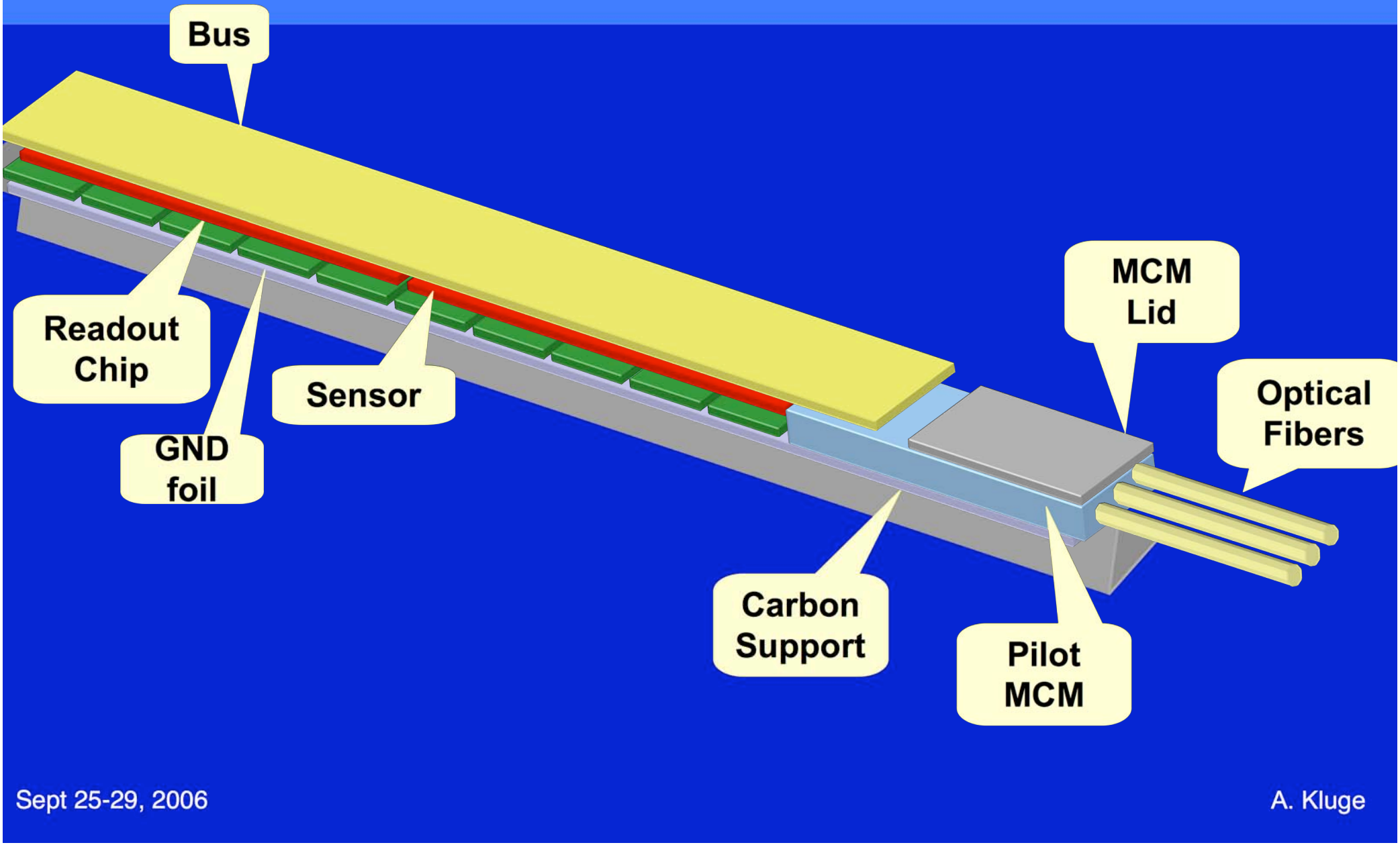


Electronics integration



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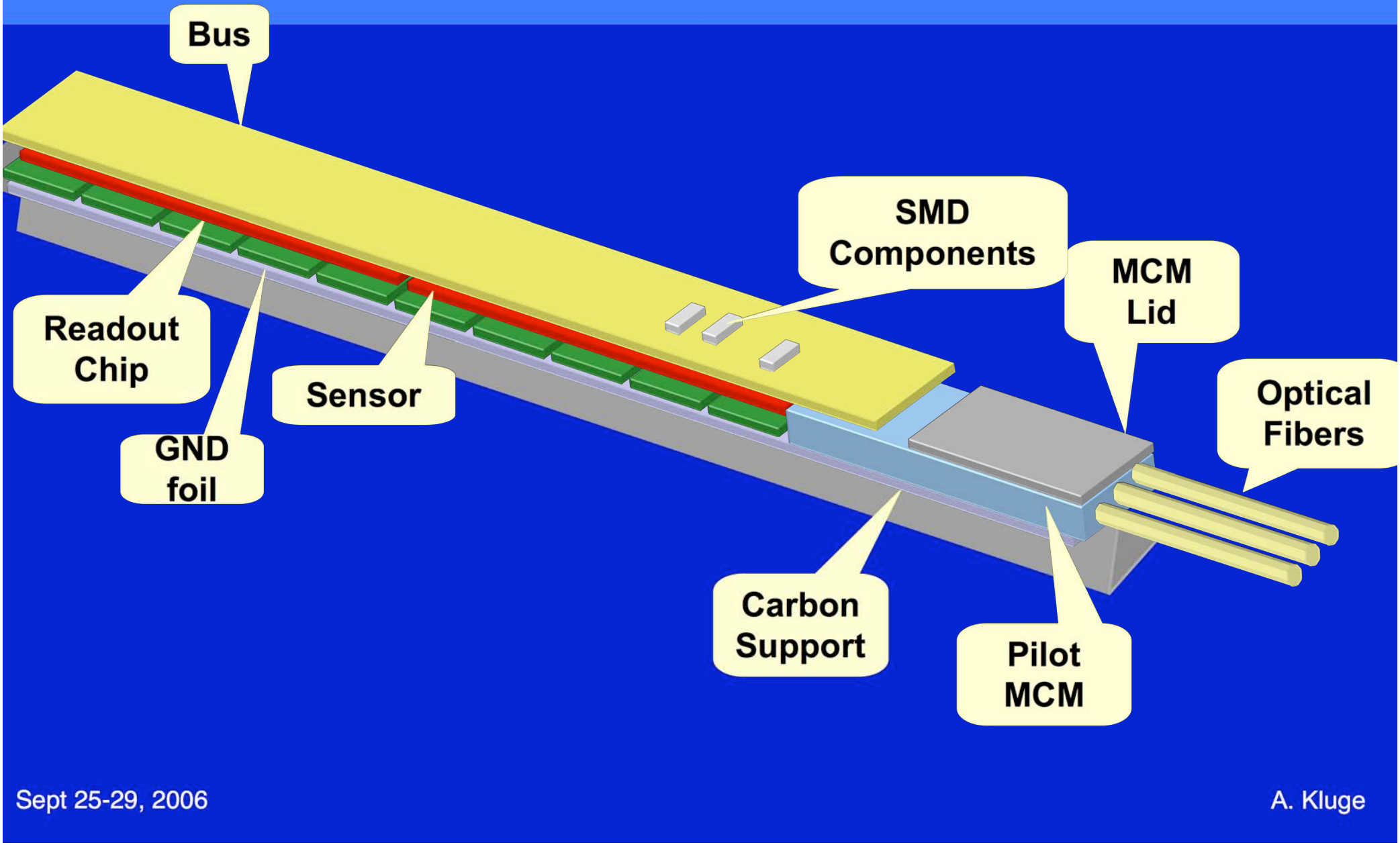

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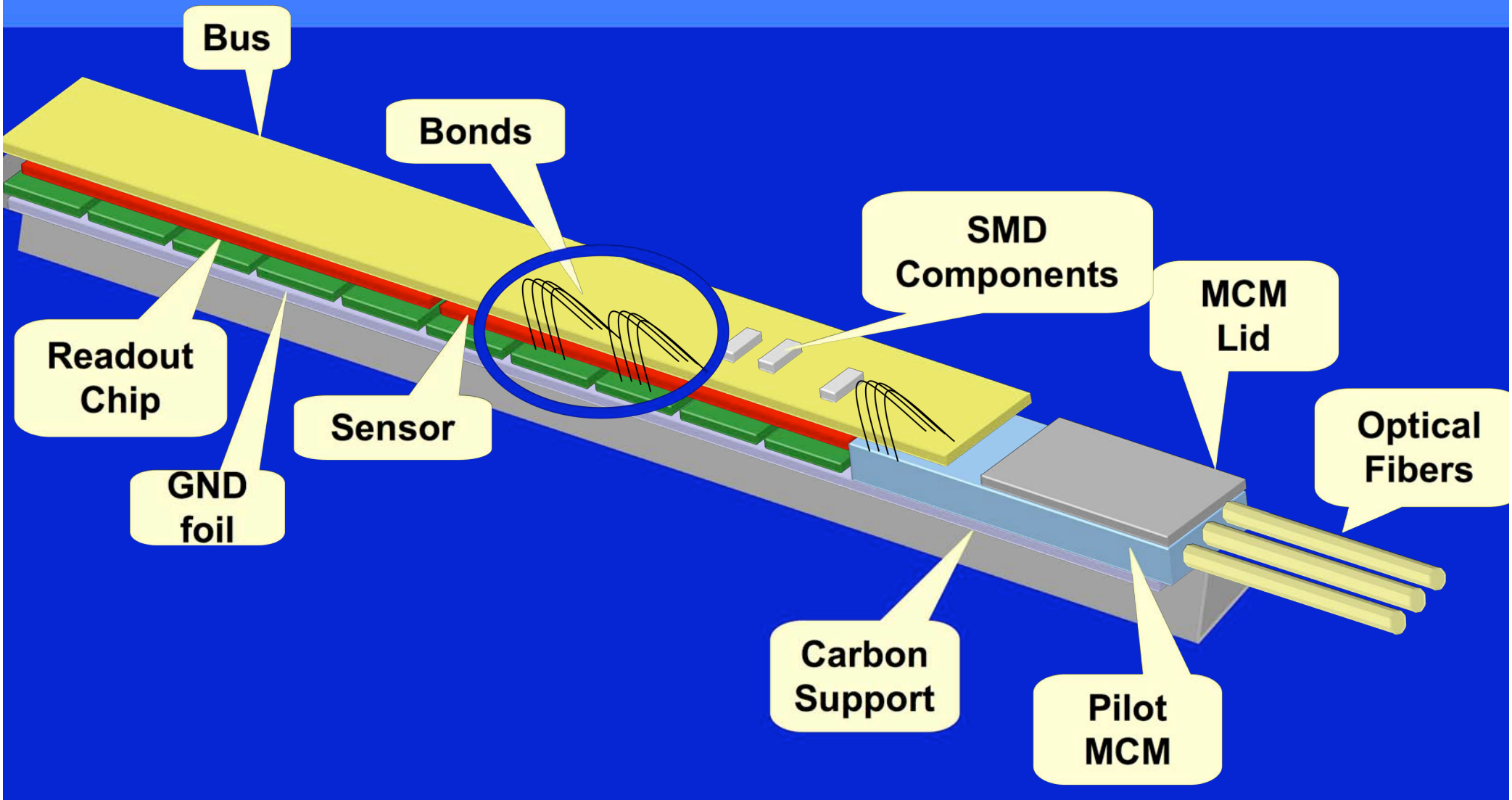
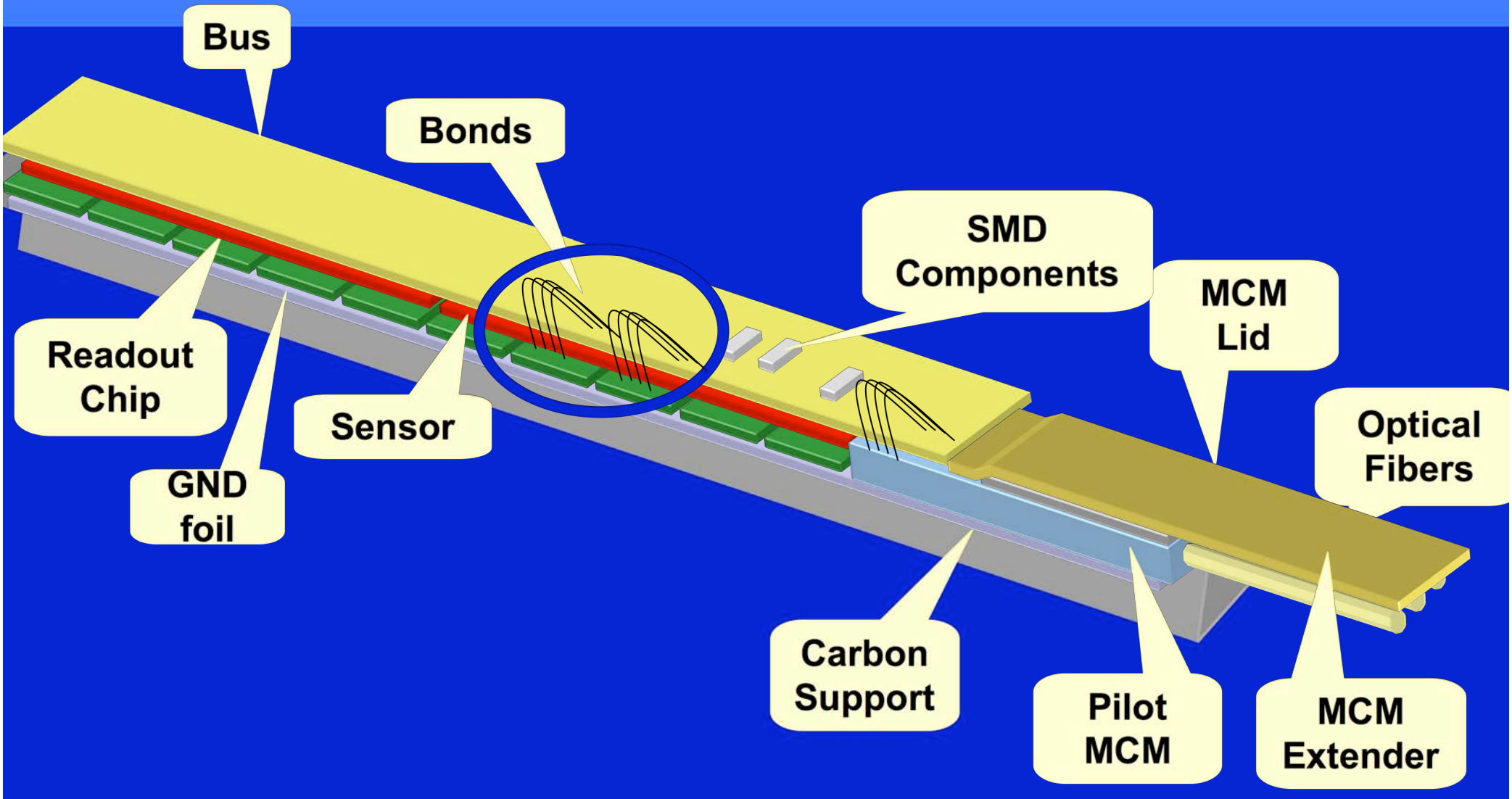


Electronics integration



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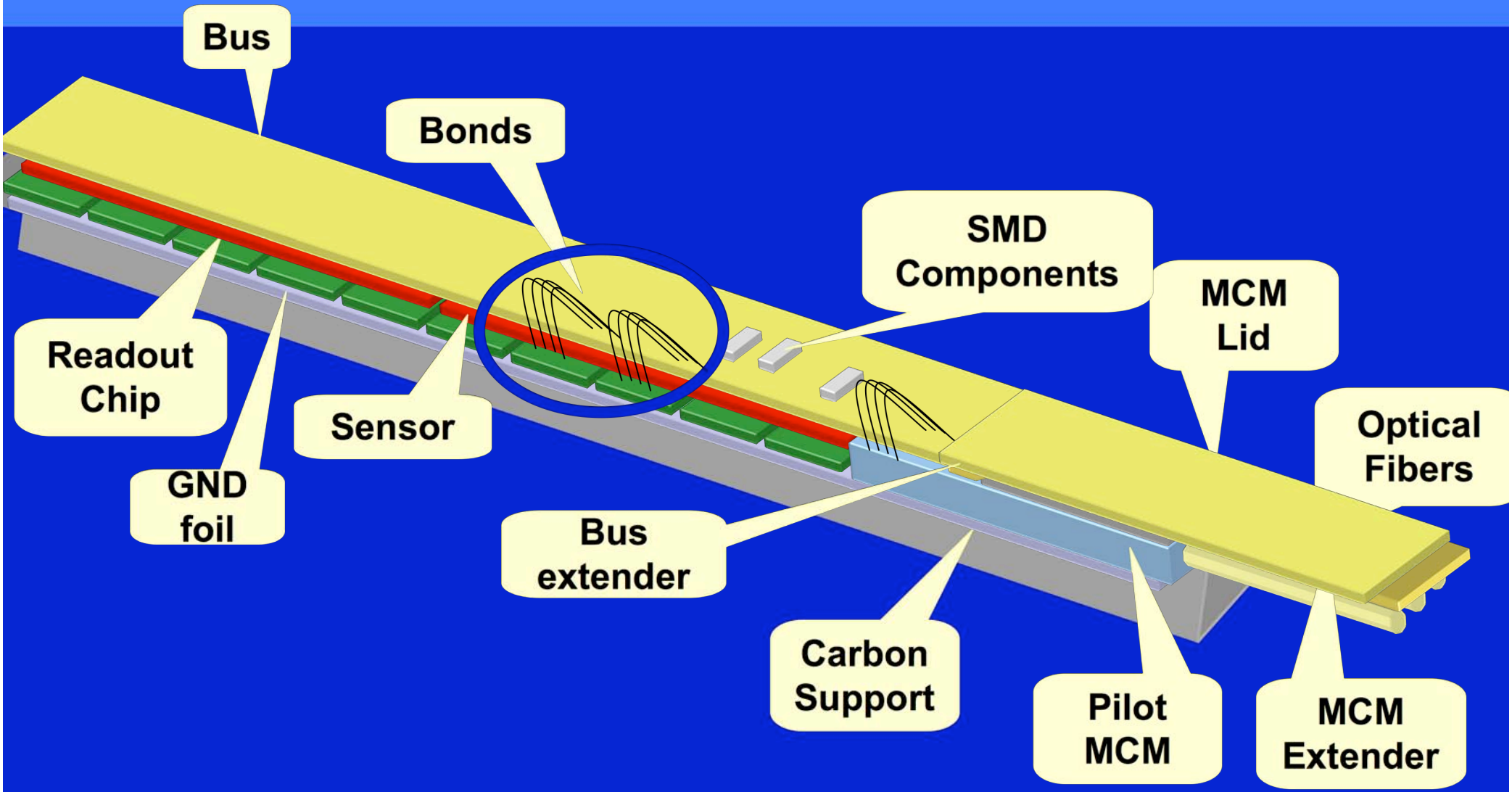

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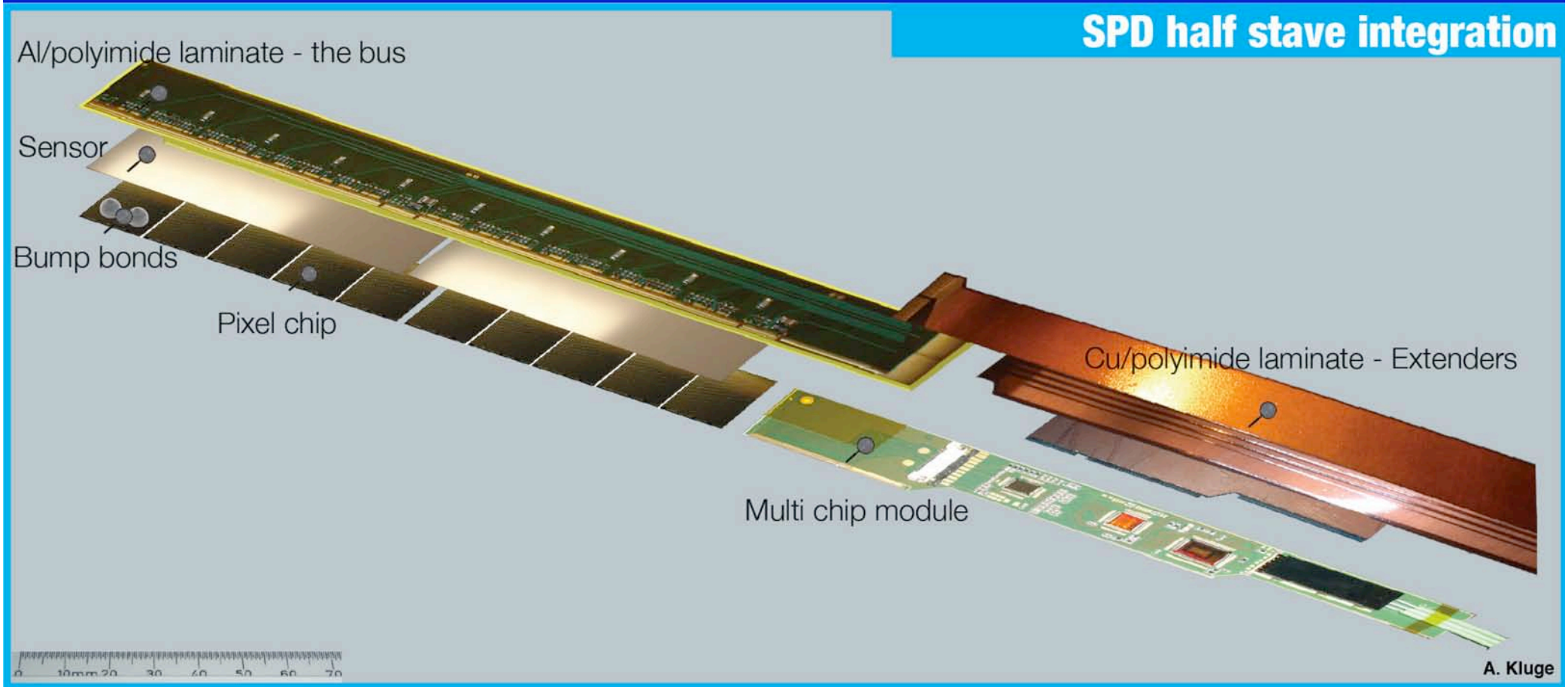
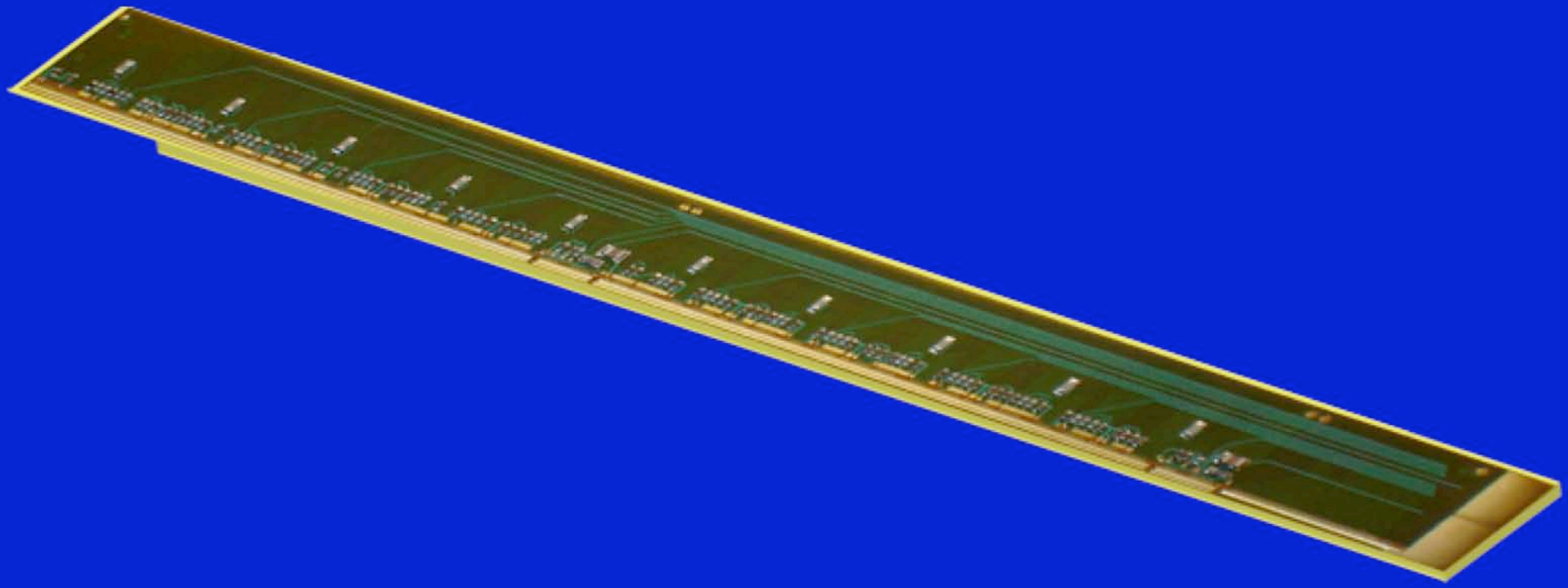
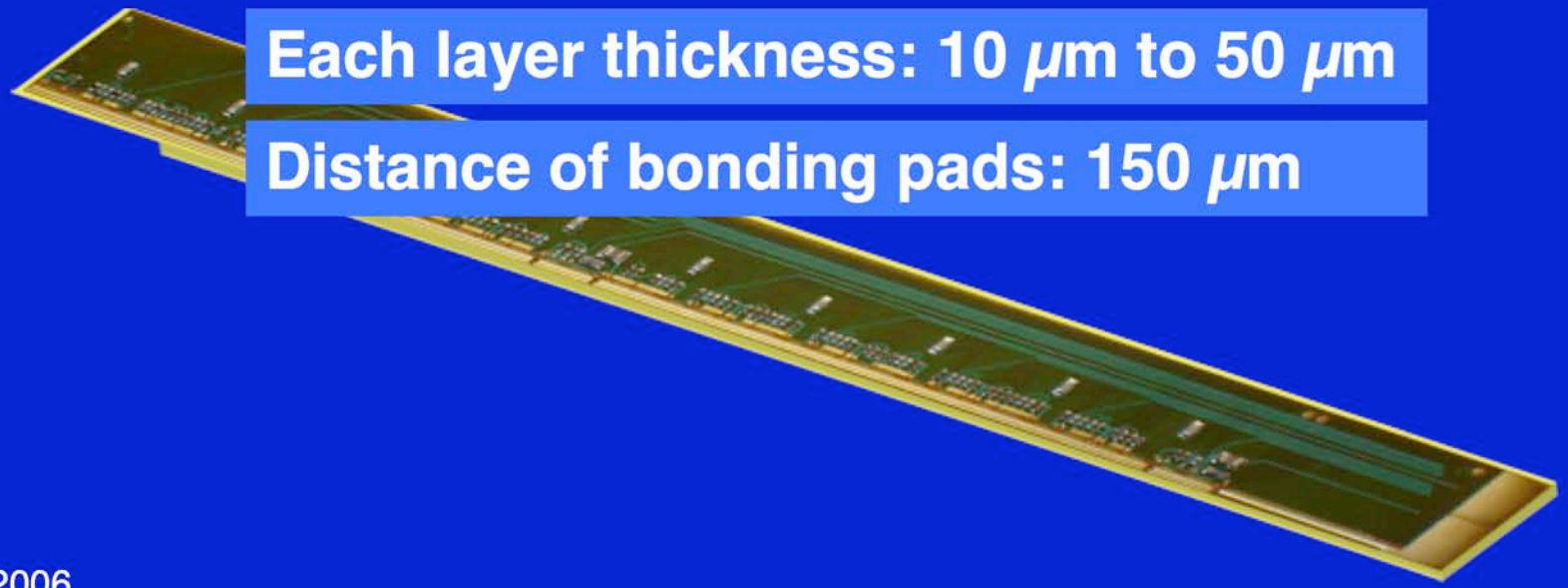


The pixel bus



The pixel bus

- Aluminum
- Length: ~ 20 cm, width ~13 mm
- Total thickness: 220 mm
- 5 layers: Power, GND, 3 signal layers
- Each layer thickness: 10 μm to 50 μm
- Distance of bonding pads: 150 μm



The pixel bus

Material budget -> Aluminum, thin

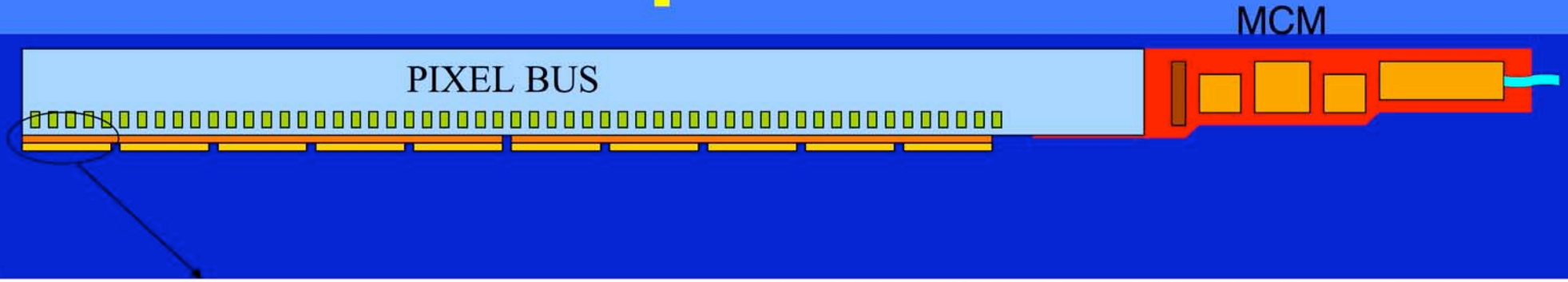
No industrial solution -> industry not interested

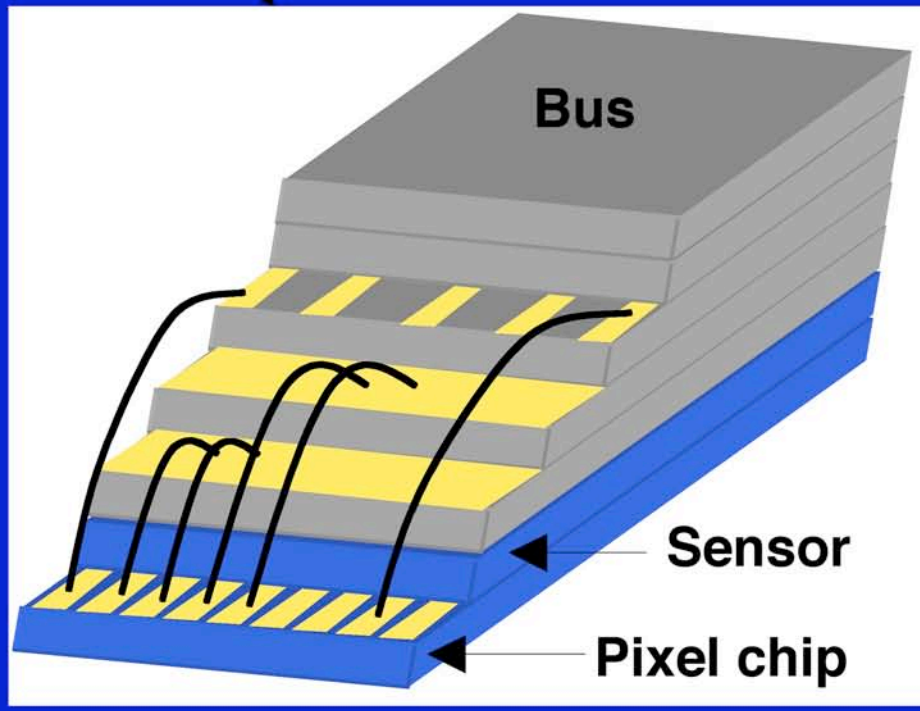
No previous experience in industry or research of Aluminium thin multi layer structures

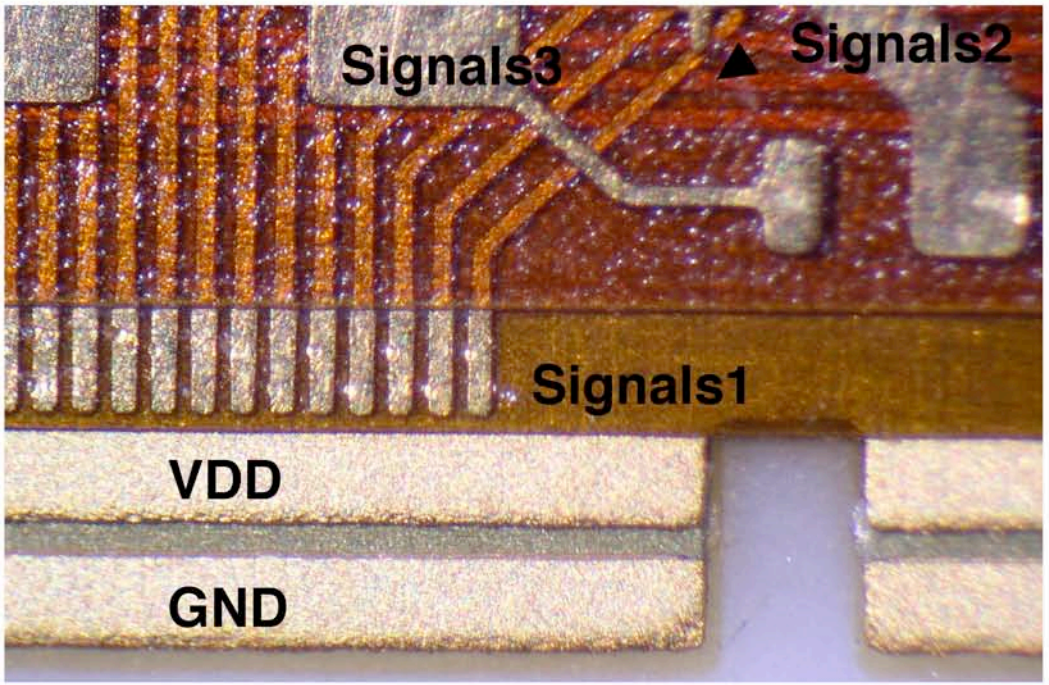
Connections between layers (vias) are difficult to make

Vias only for signals
Power uses stair case structure

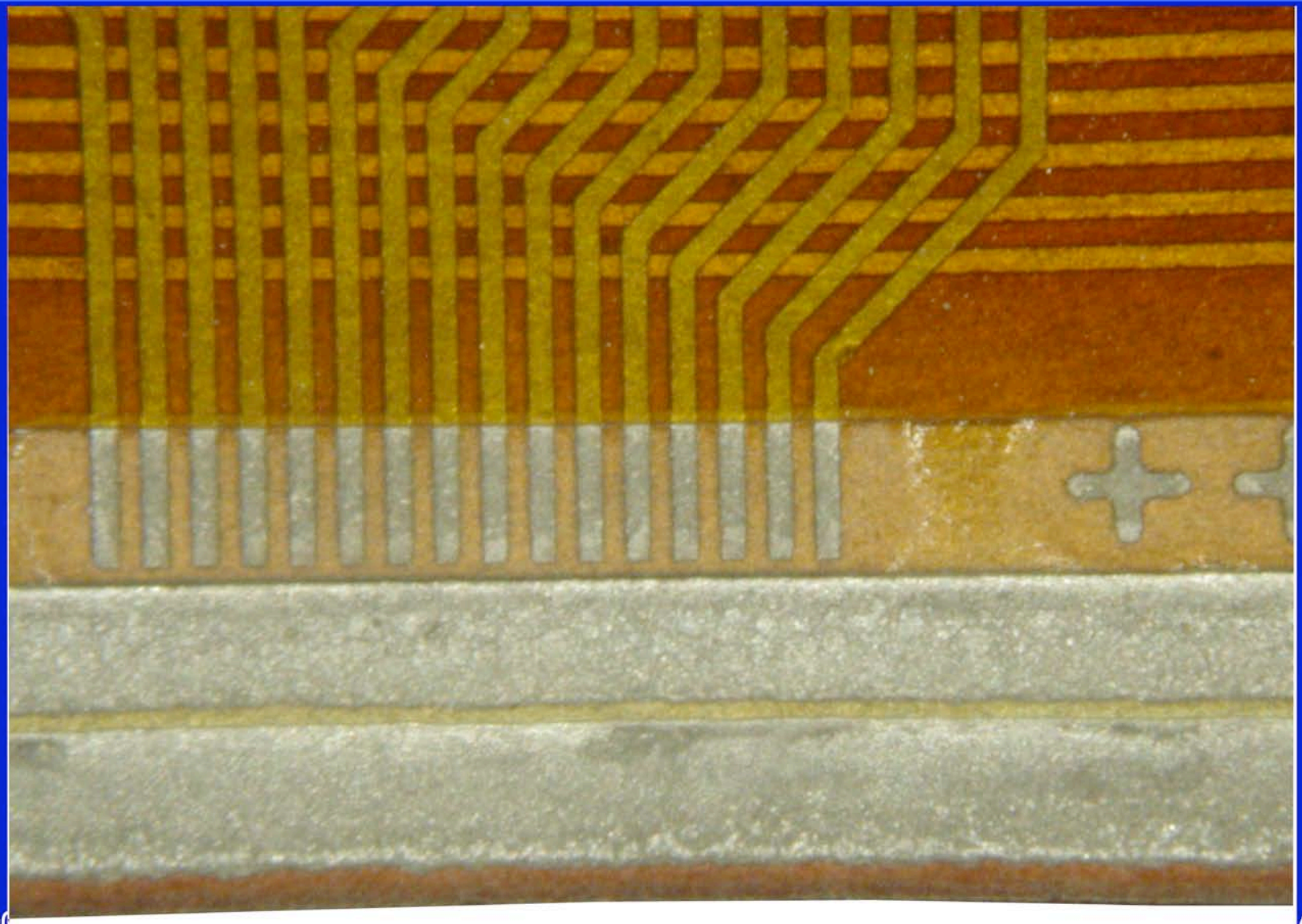
The pixel bus



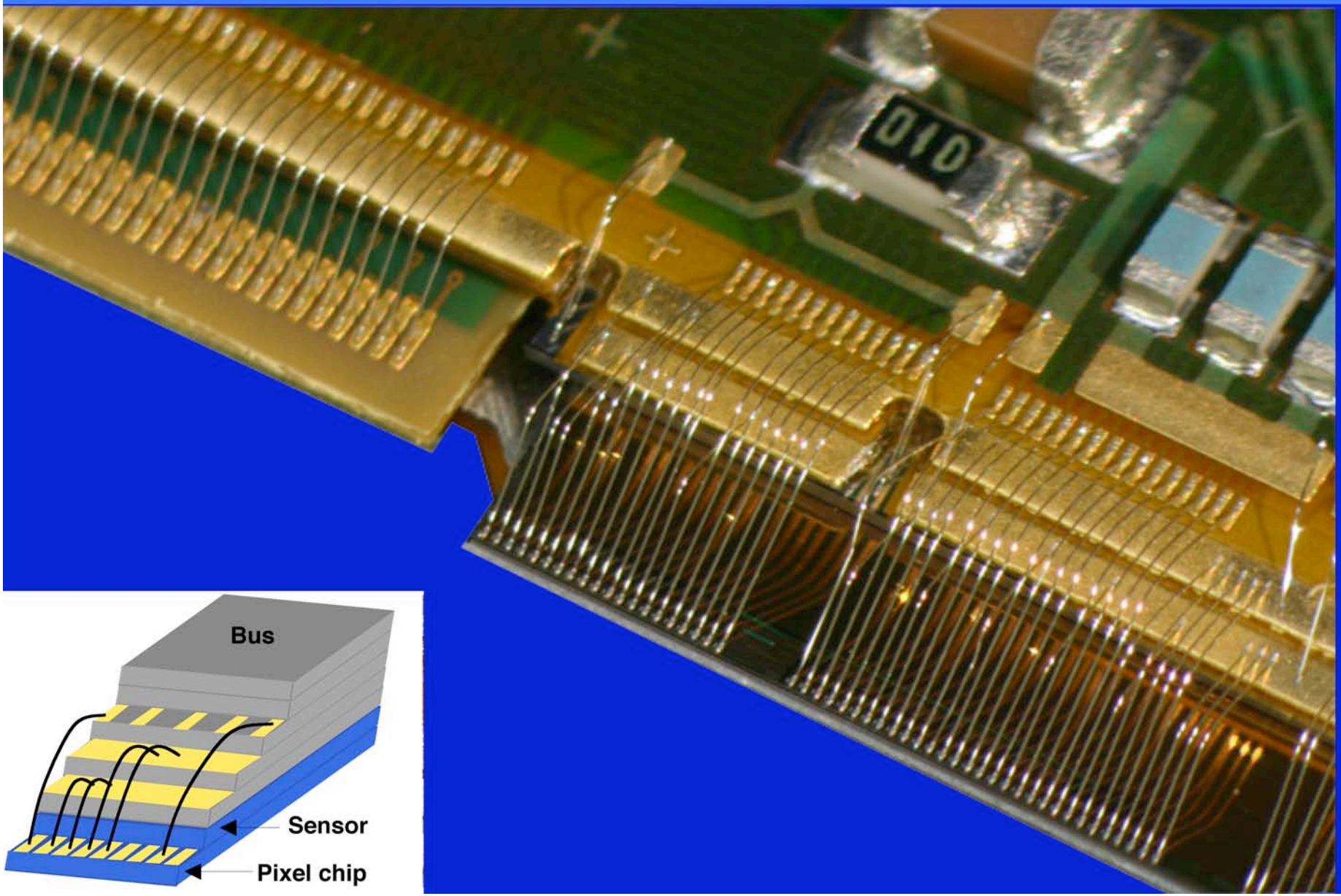




The pixel bus

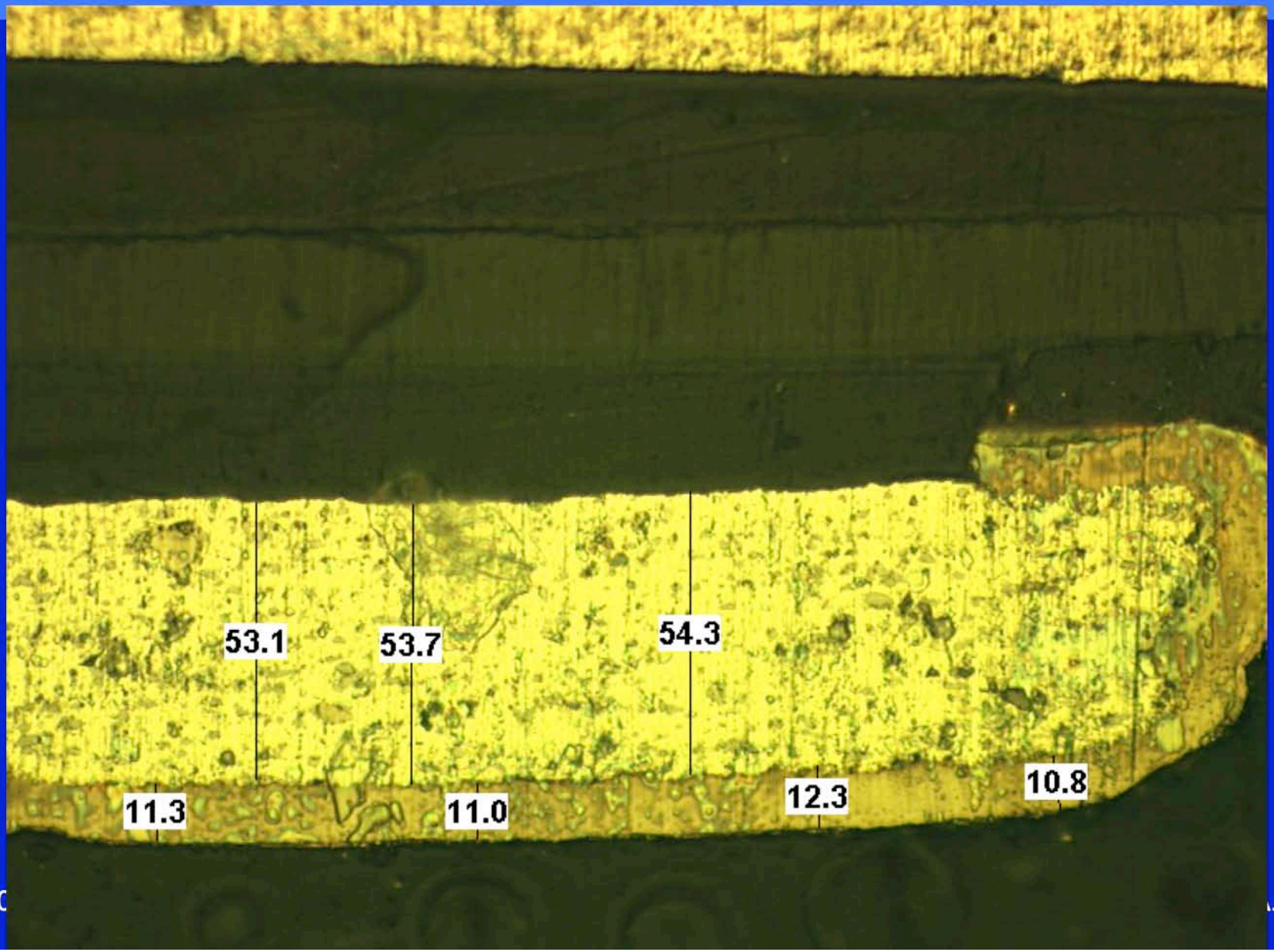


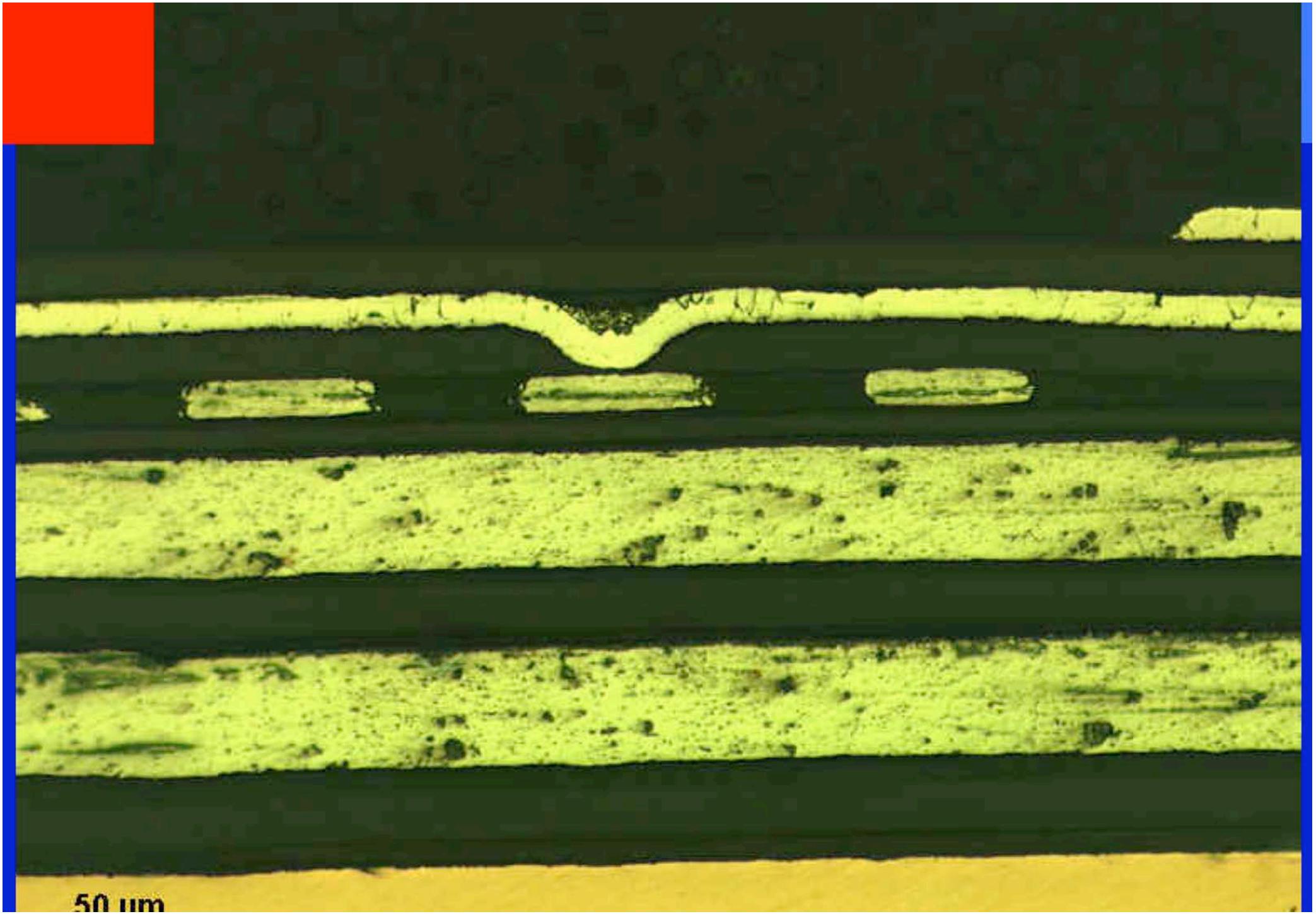
The pixel bus

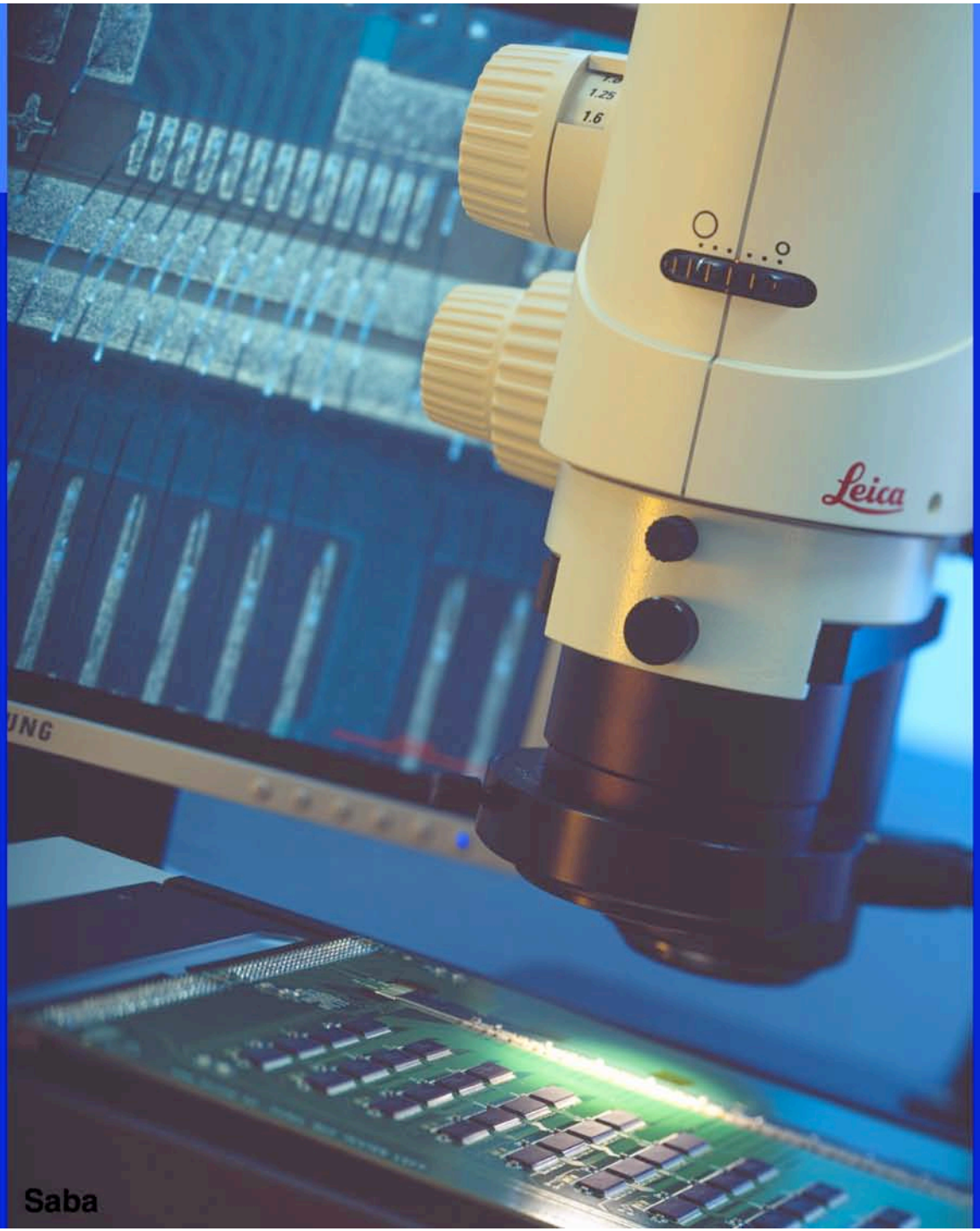


A. Kluge

The pixel bus



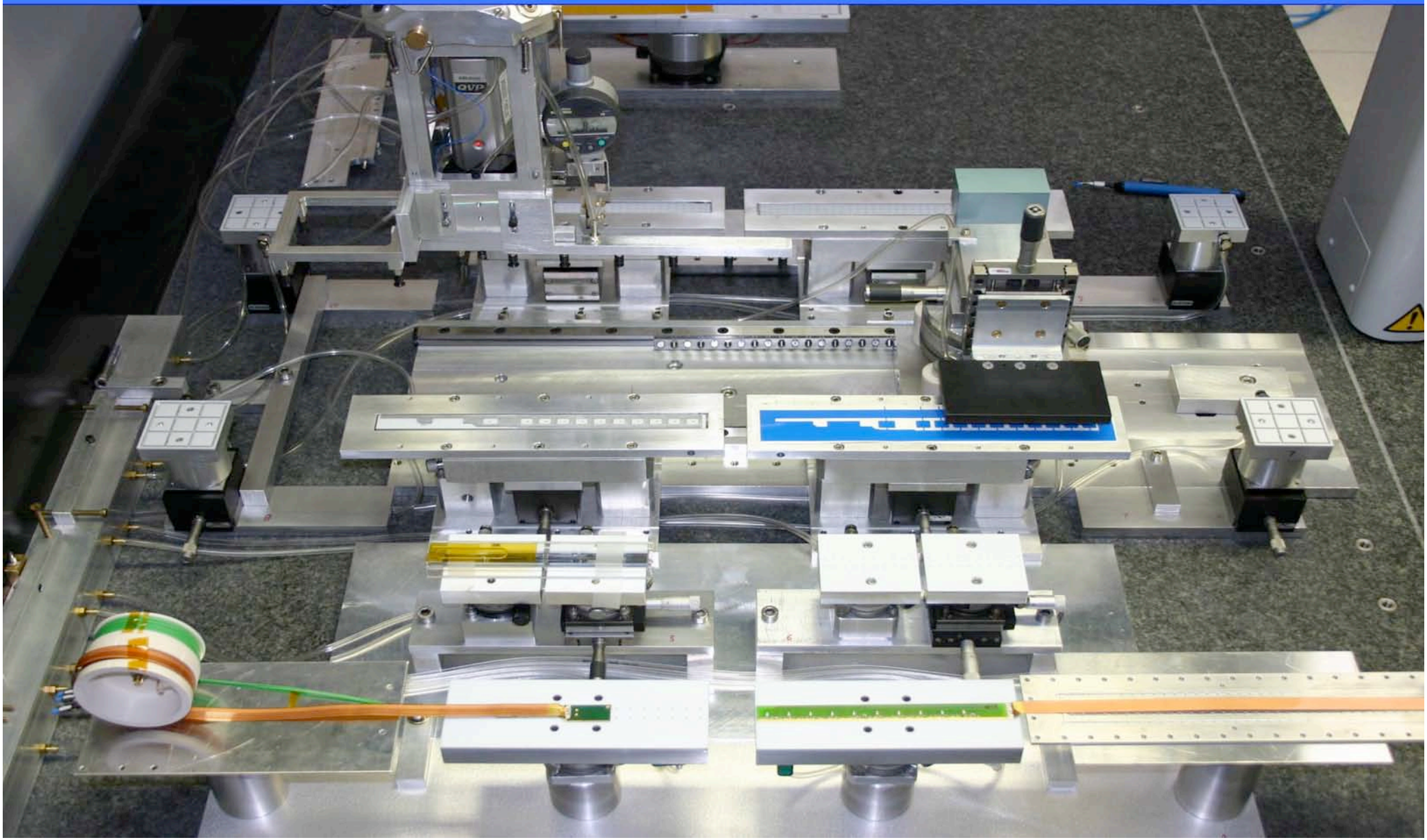

50 um


Leica
Saba

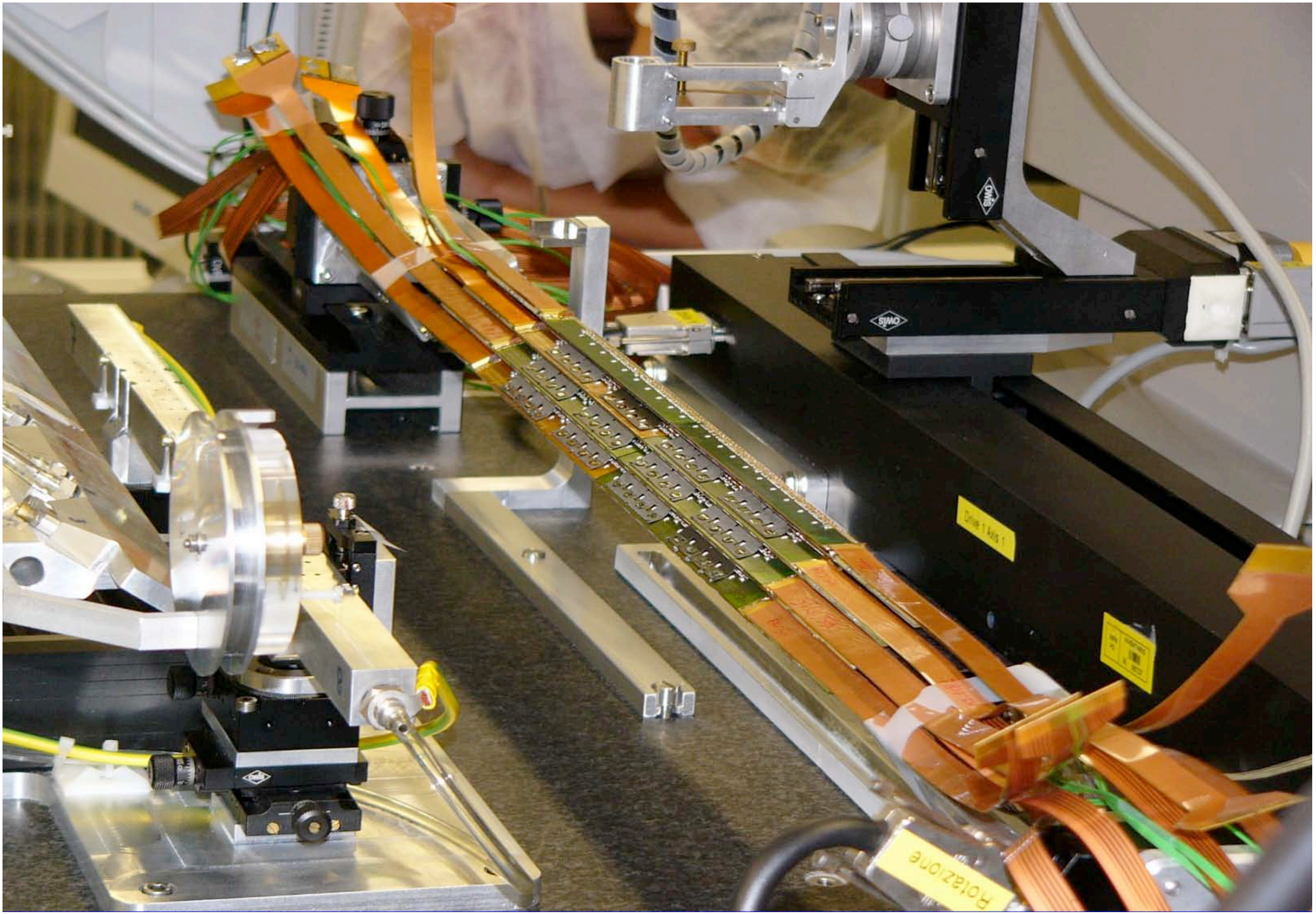
Half stave assembly

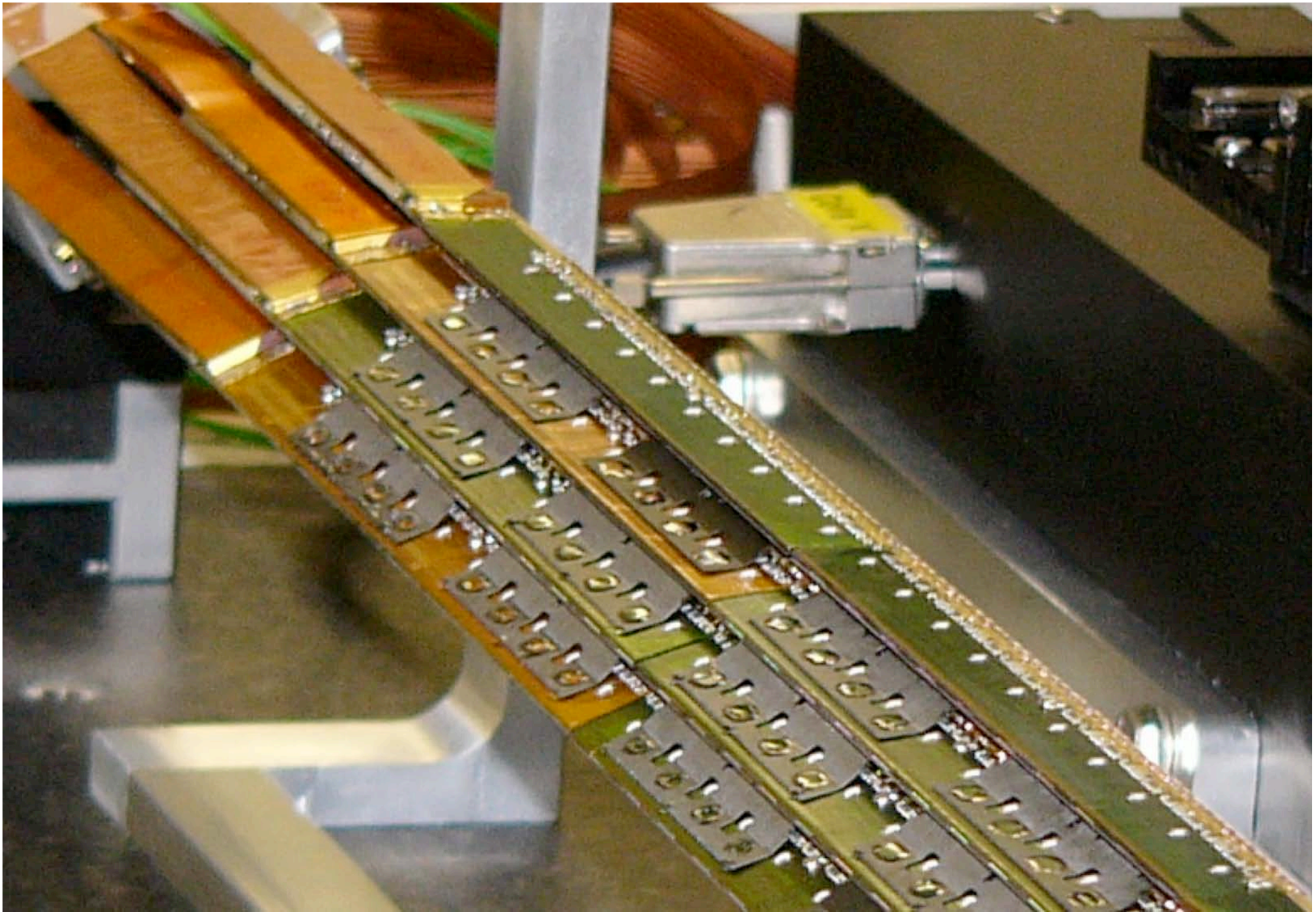
A. Kluge

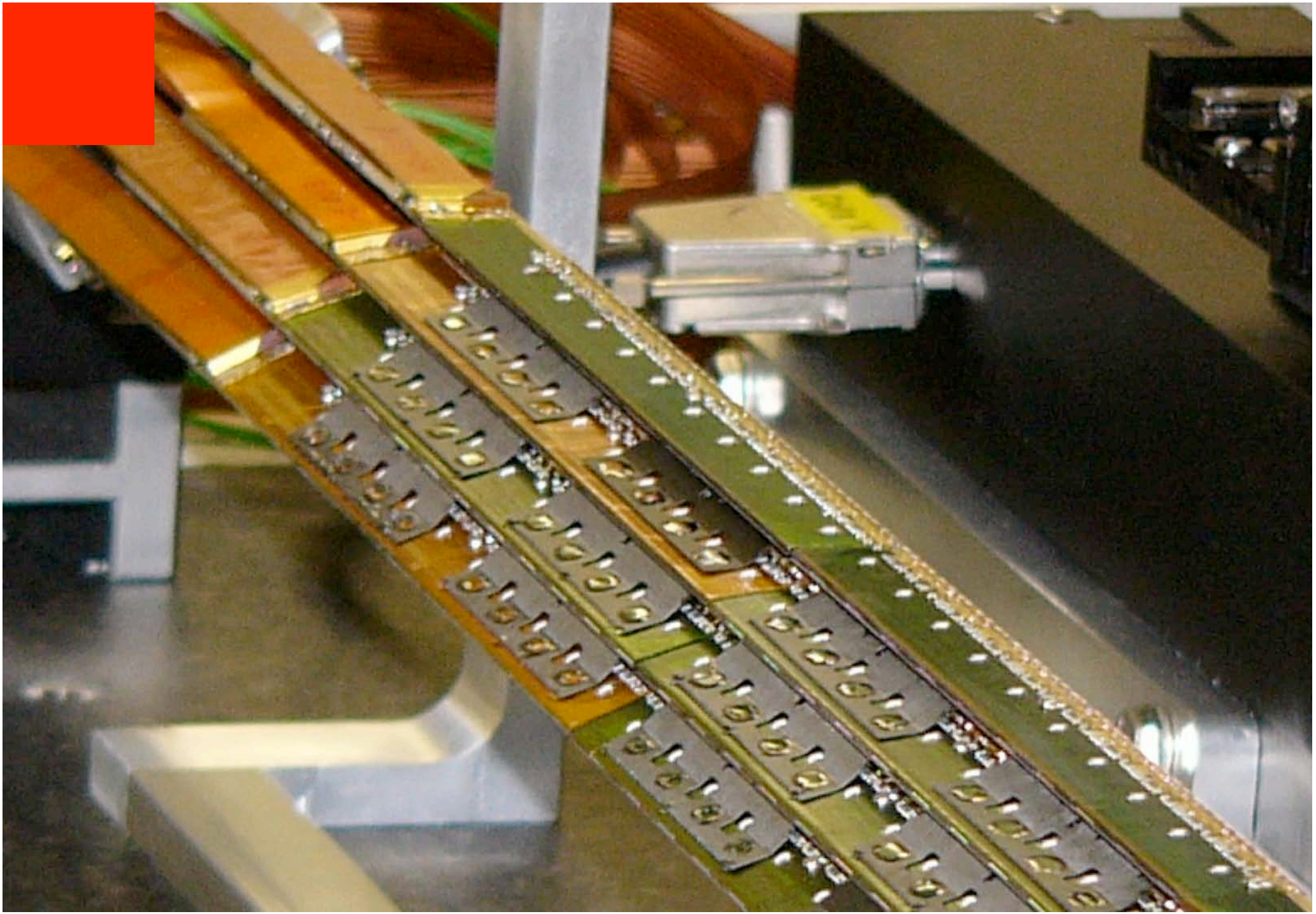
Half stave assembly station



Sector assembly

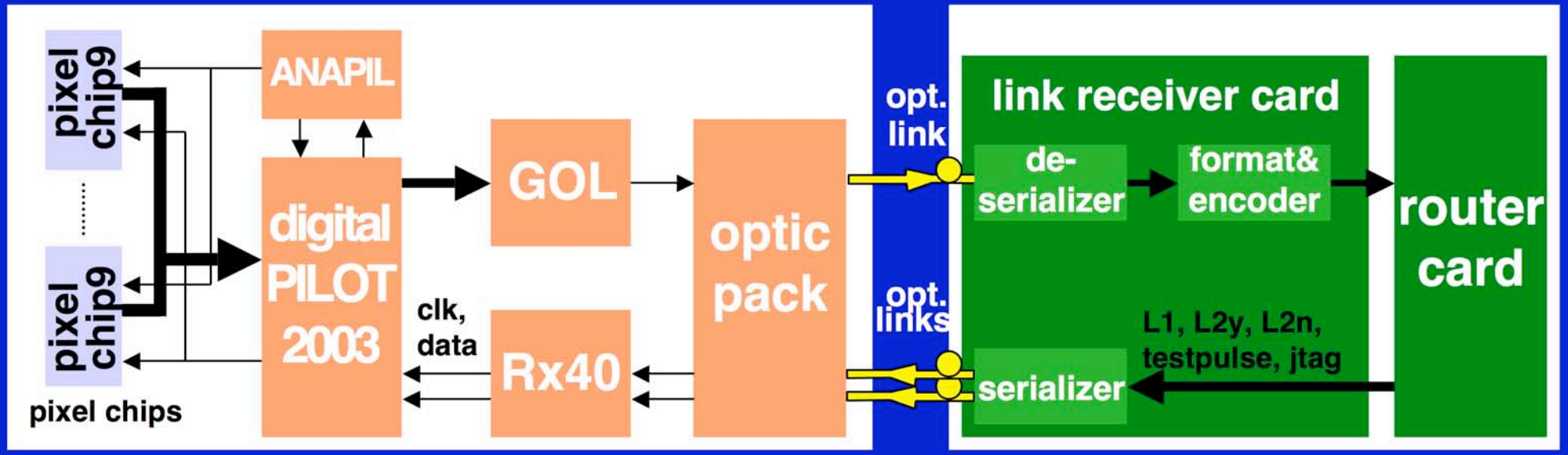

OMS
OMS
Drive 1 Axis 1
Rotazione



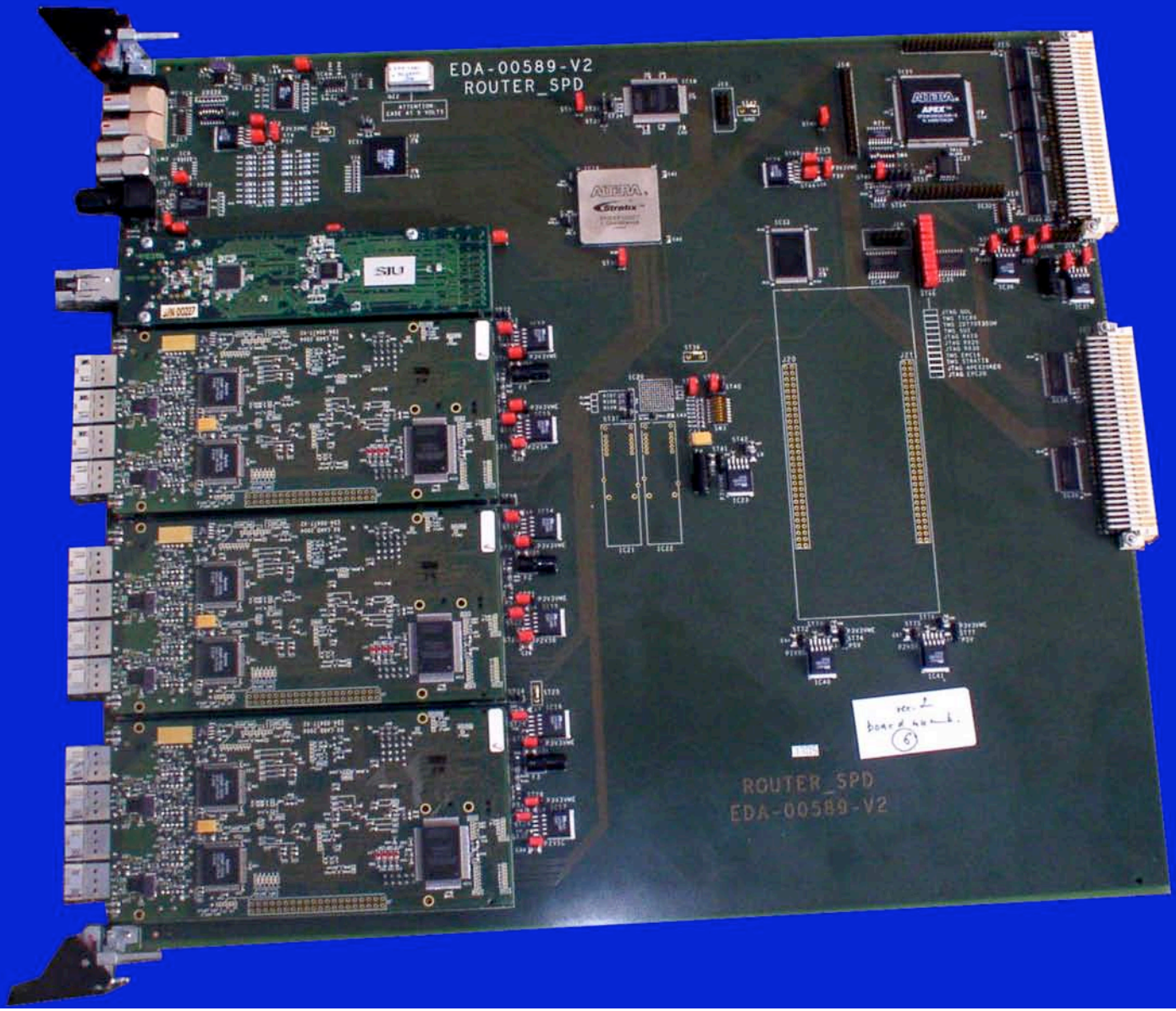


Off detector electronics

Off detector electronics



Off detector electronics



Installation & Integration in the SPD clean room

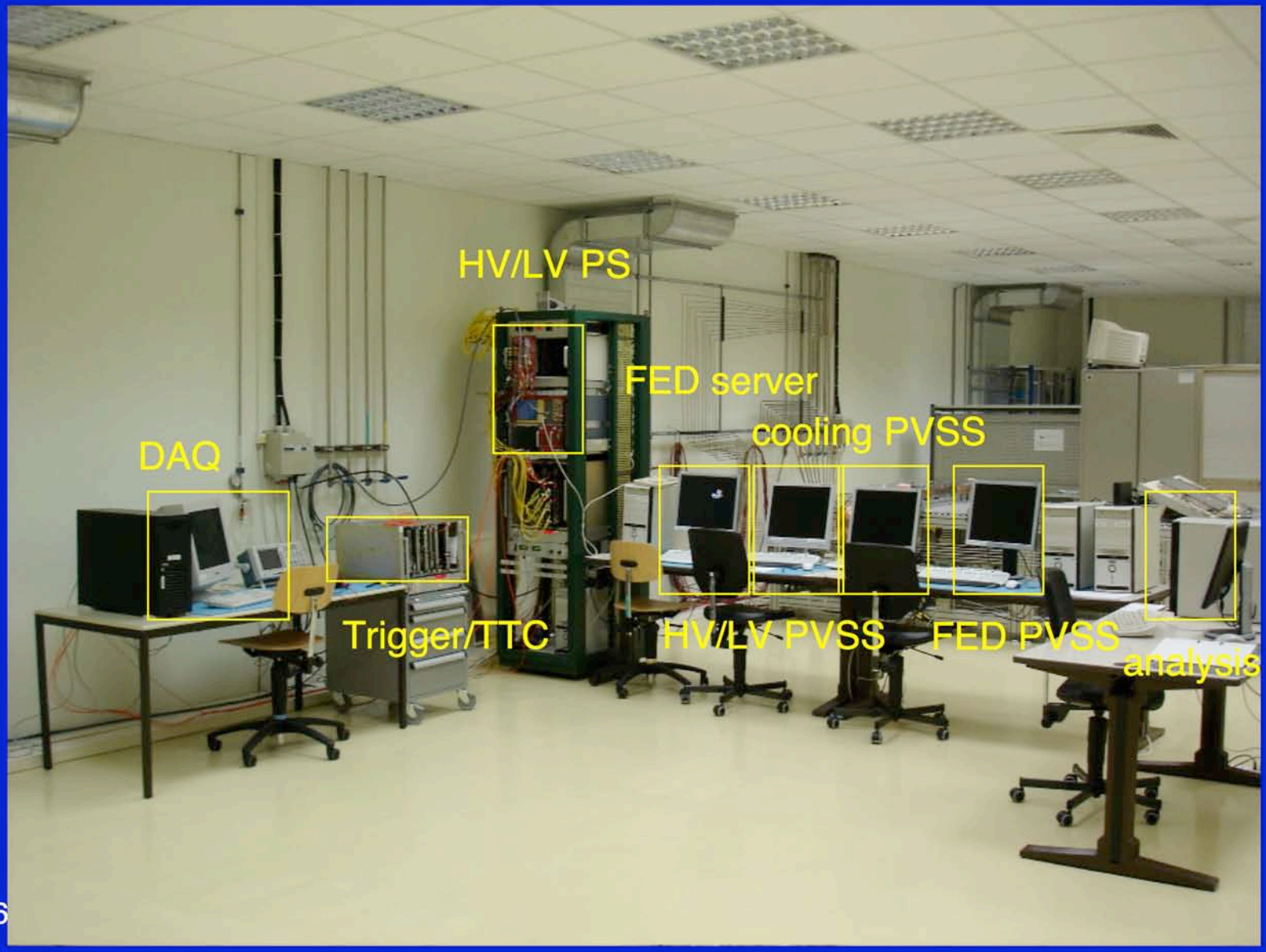
Sept 25-29, 2006

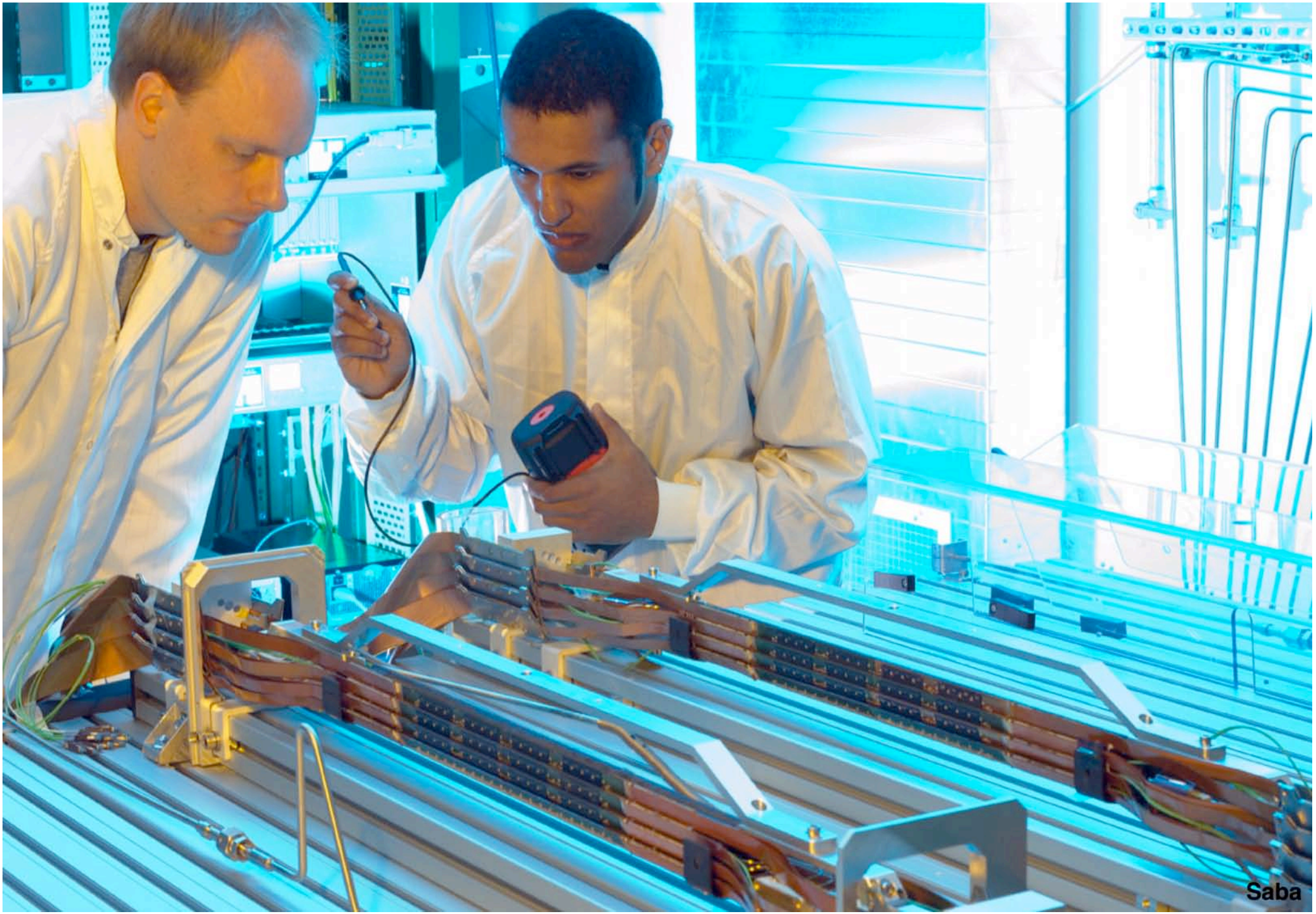
A. Kluge

System and Detector Integration

- ALICE SPD detector
- ALICE SPD DCS & DAQ
- ALICE SPD trigger interface
- ALICE SPD LV & HV system
- ALICE SPD cooling
- ALICE SPD cabling & patch panels

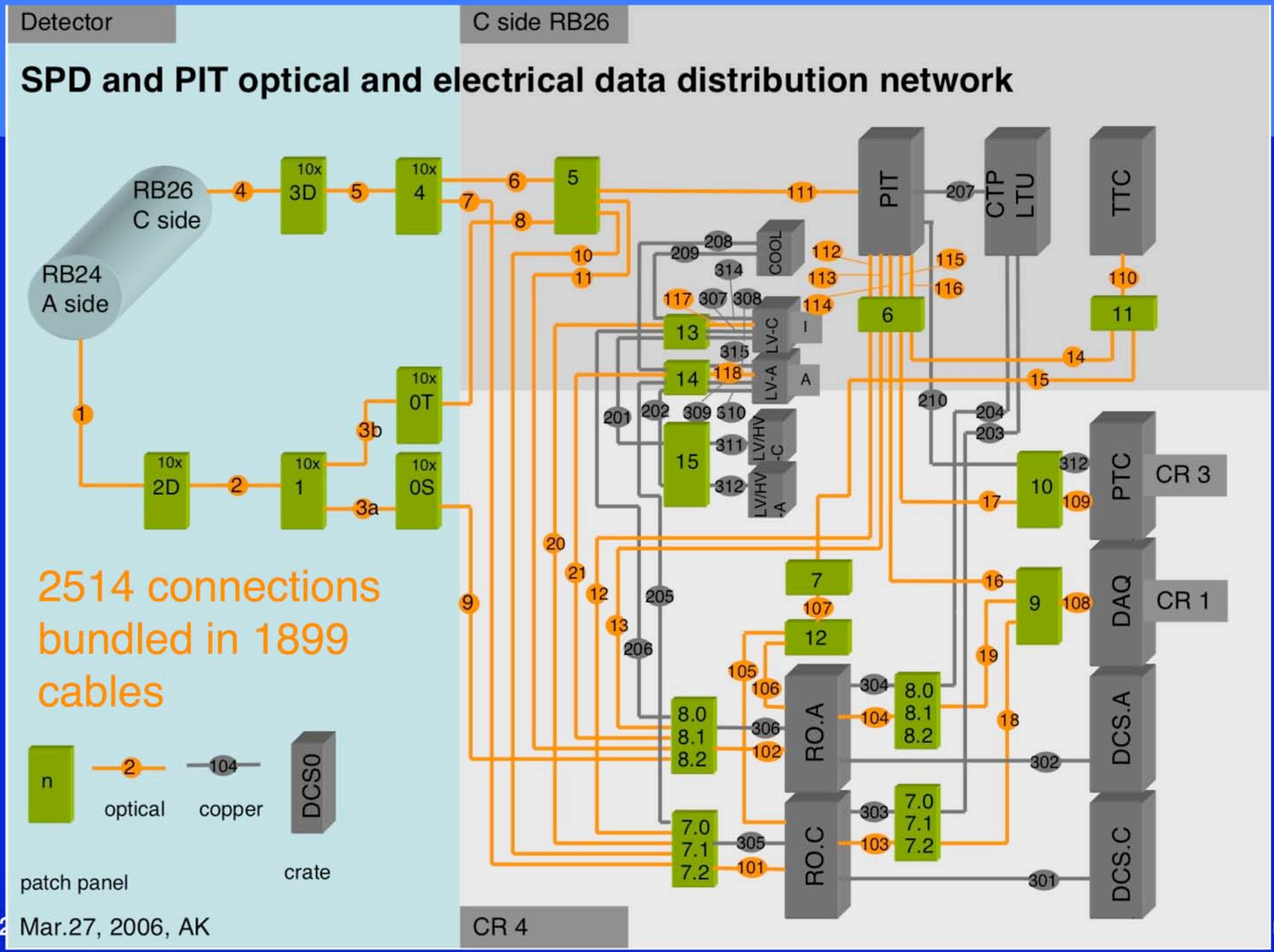
System and Detector Integration




Saba


Saba

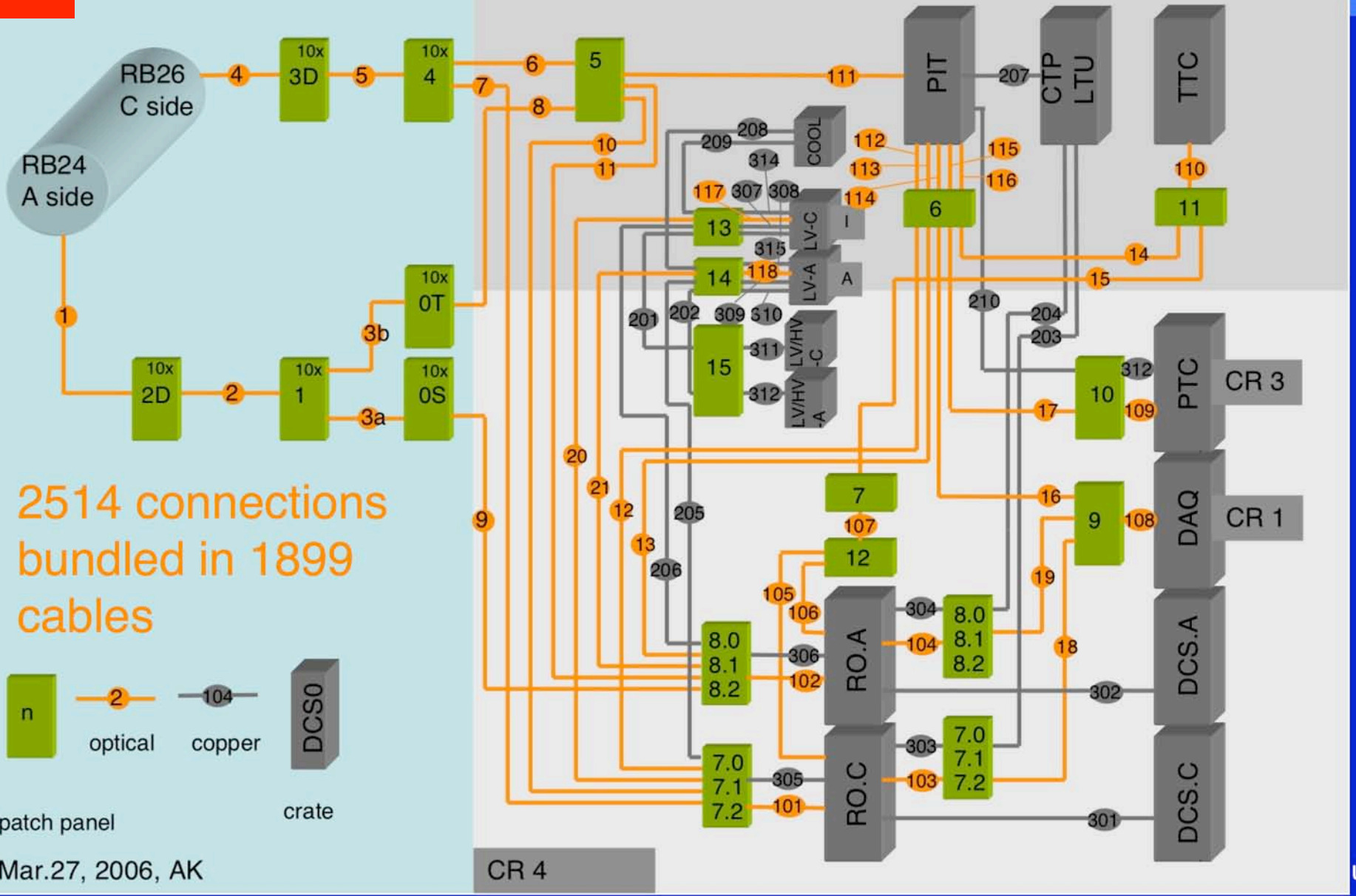
Infrastructure & Cabling


Detector
C side RB26
SPD and PIT optical and electrical data distribution network
RB26
C side
RB24
A side
10x
3D
10x
4
10x
2D
10x
1
10x
0T
10x
0S
PIT
CTP
LTU
TTC
COOL
LV-C
I
LV-A
A
LV/HV
-C
LV/HV
-A
PTC
CR 3
DAQ
CR 1
DCS.A
DCS.C
RO.A
RO.C
8.0
8.1
8.2
7.0
7.1
7.2
2514 connections
bundled in 1899
cables
n
optical
copper
DCS0
patch panel
crate
Mar.27, 2006, AK
CR 4

or

C side RB26

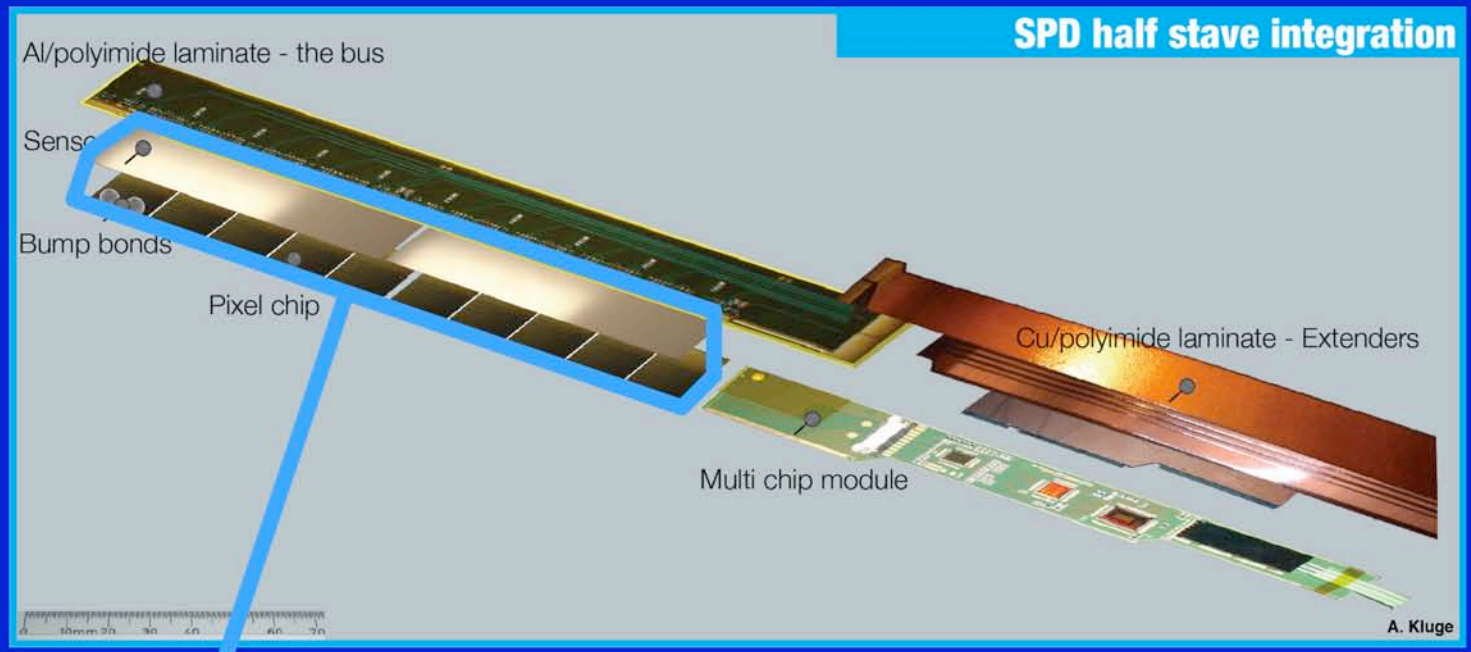
and PIT optical and electrical data distribution network



SPD component & integration status

A. Kluge

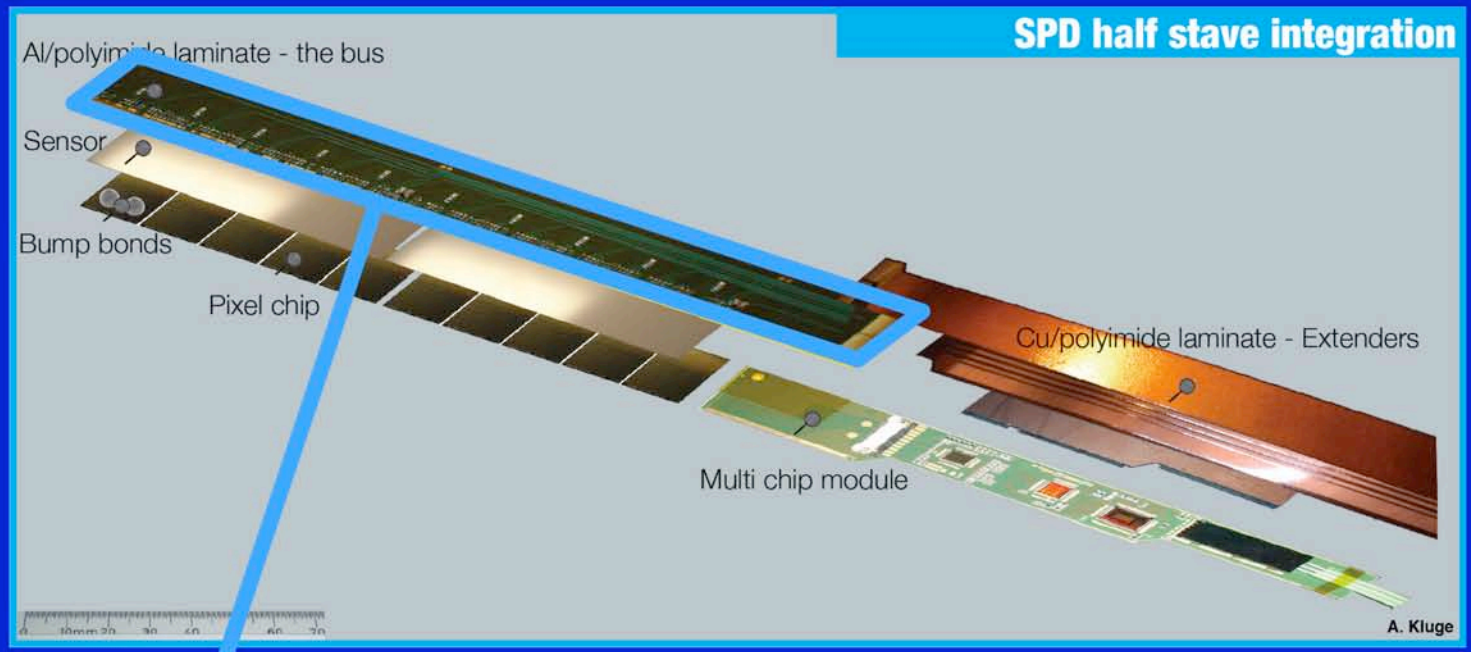
Component status



Detector ladders = sensors + 5 read out chips

Quantity required:	**240**	
Quantity produced:	**150**	**63%**

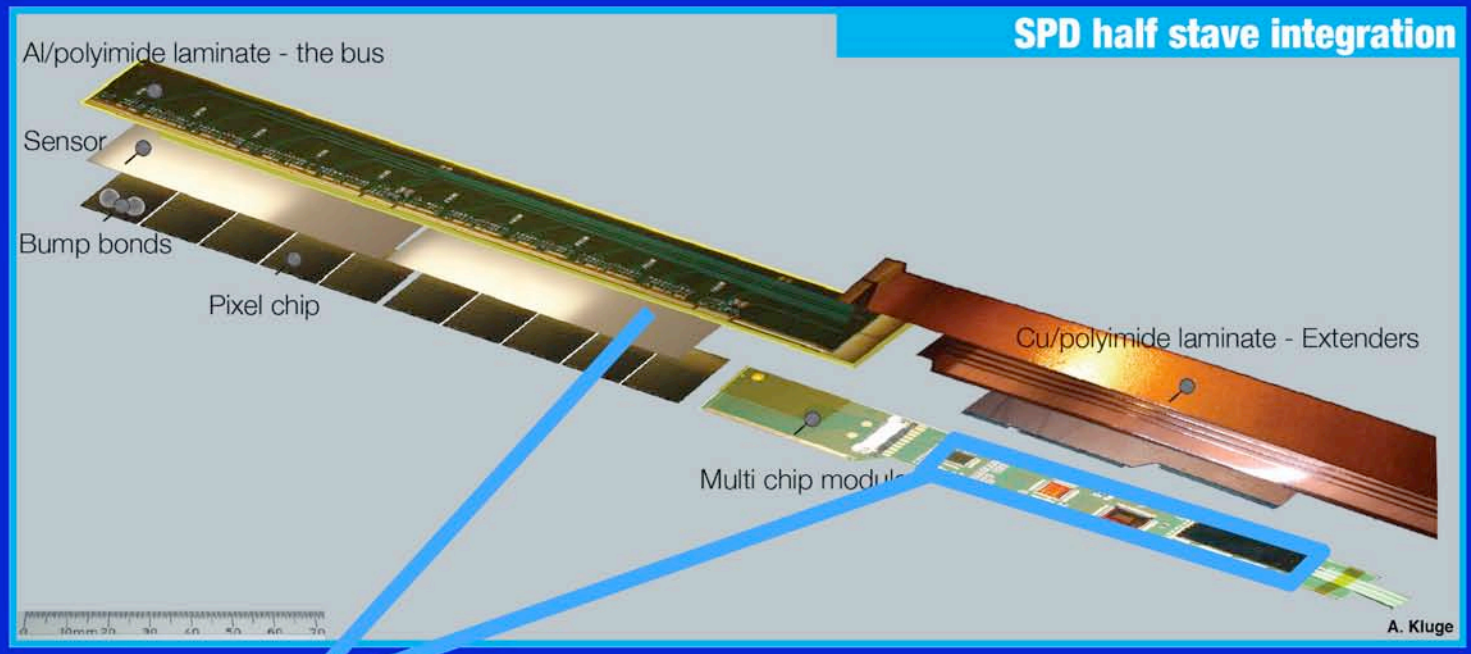
Component status



Pixel bus = high densitity interconnect

Quantity required:	**120**	
Quantity produced:	**100**	**83%**

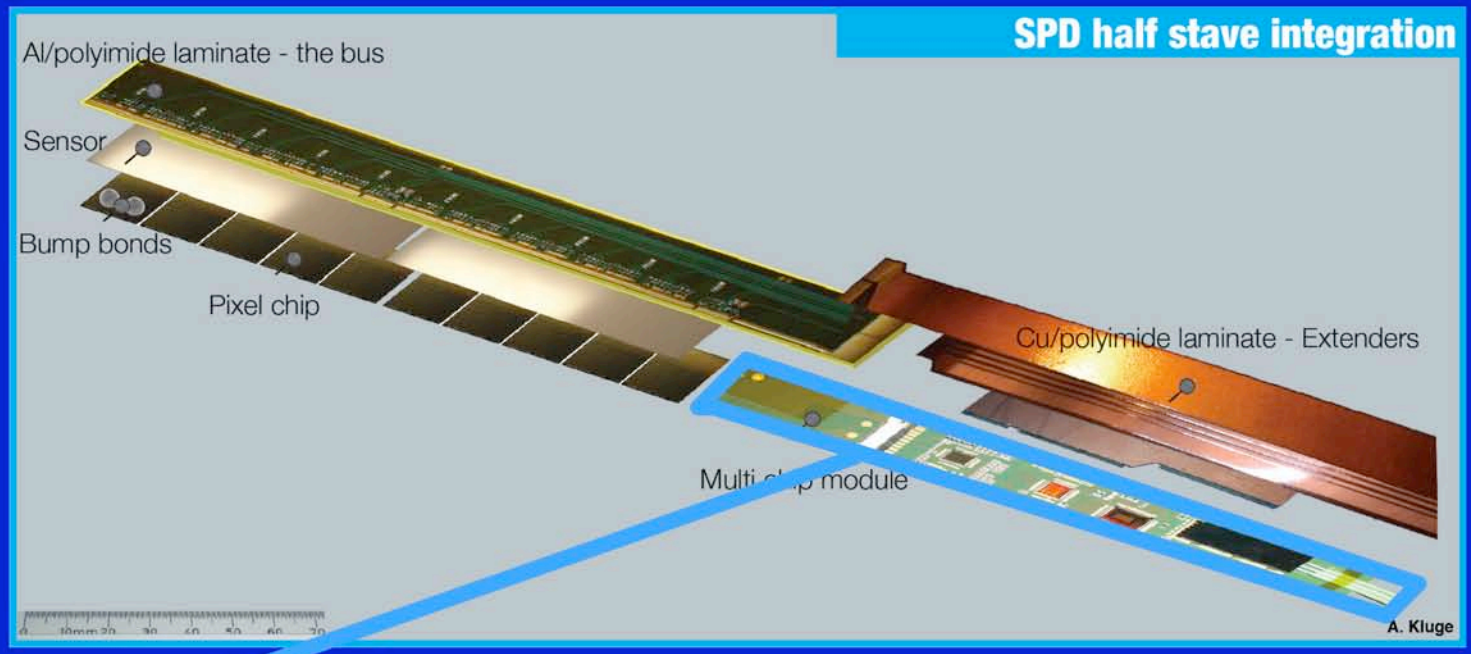
Component status



ASICs + optical component

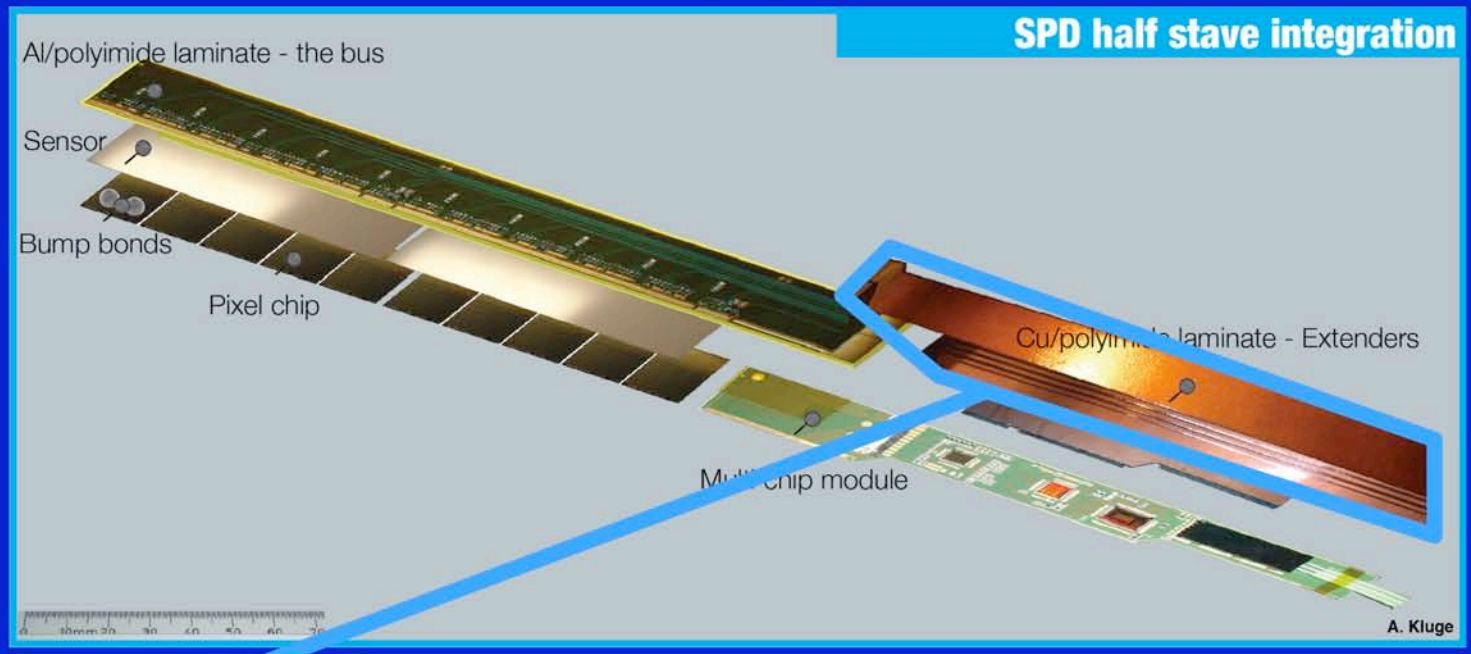
Quantity required:	**120**
Quantity produced:	**>144 100%**

Component status



Multi chip module mounted (~6 / week)		
Quantity required:	**120**	
Quantity produced:	**94**	**78 %**

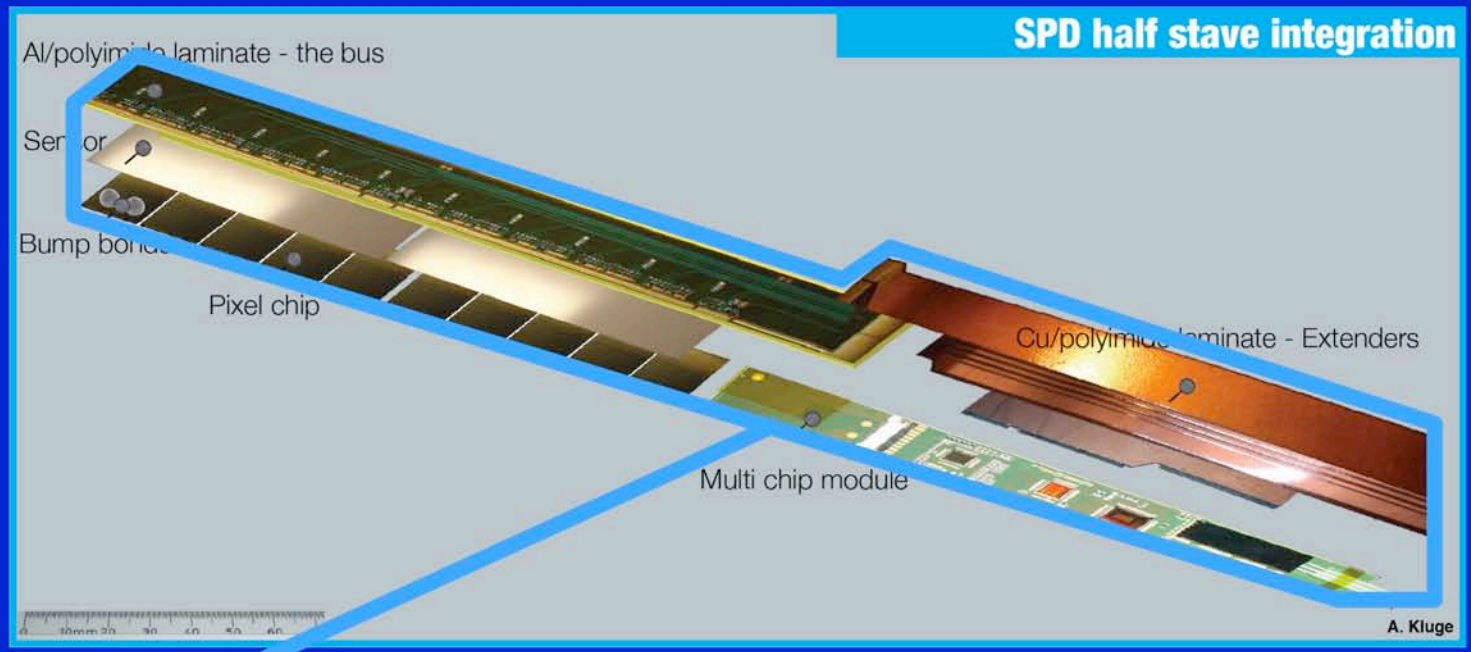
Component status



Cu-Kapton power flat cables

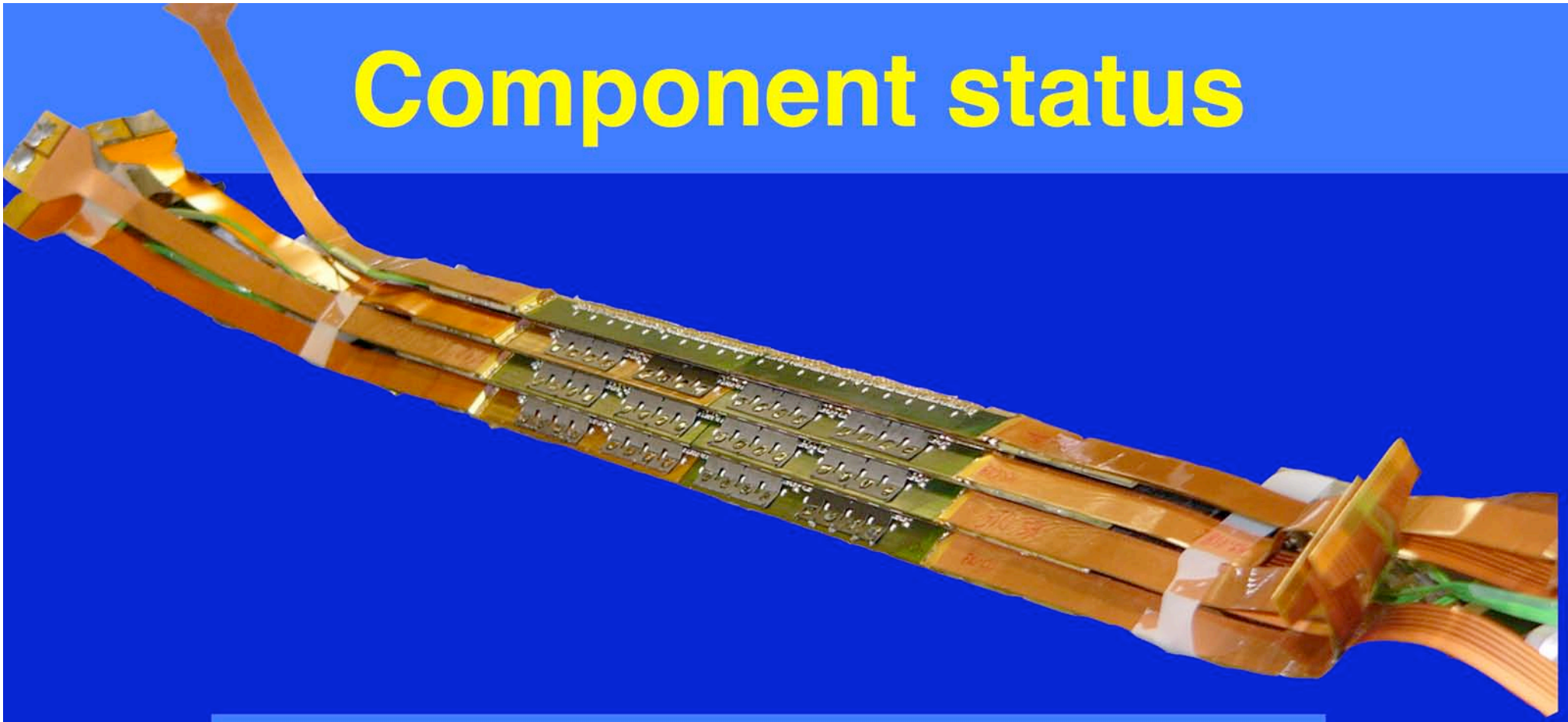
Quantity required:	**120**	
Quantity produced:	**144**	**100%**

Component status



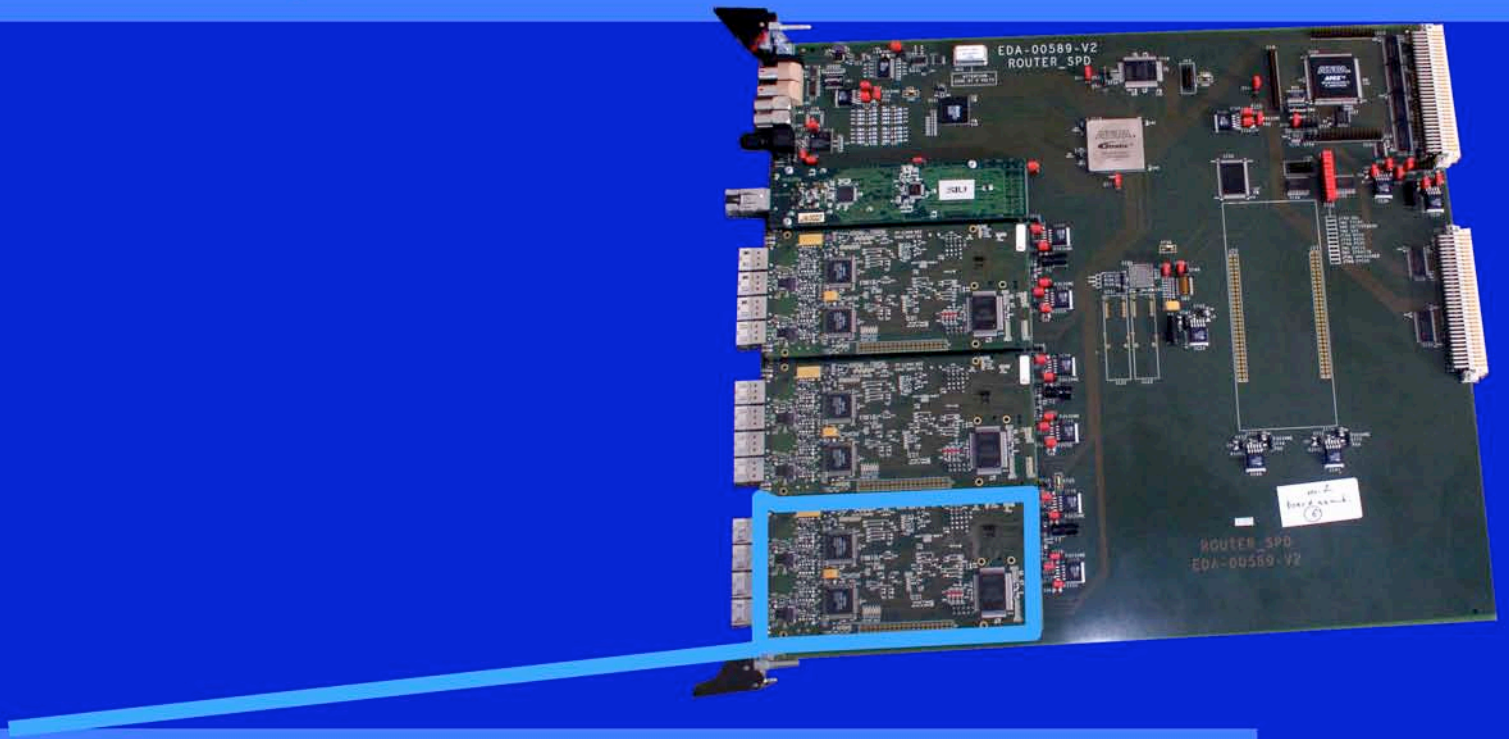
Half staves (max. 4/week)		
Quantity required:	**120**	
Quantity produced:	**69**	**58 %**

Component status



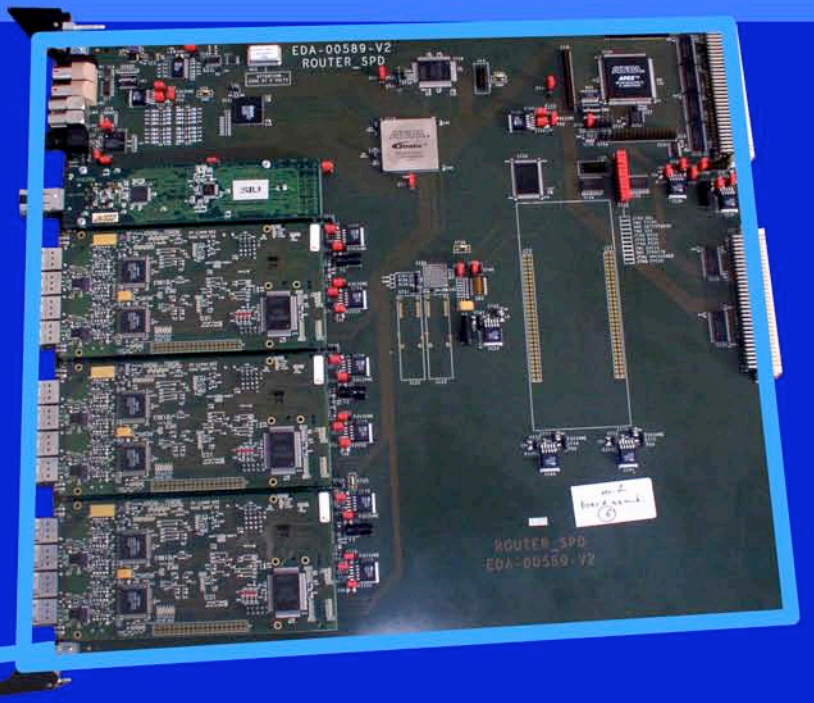
Sector (max 1 / month)		
Quantity required:	10	
Quantity produced:	5	50 %

Component status



Link receiver cards		
Quantity required:	**60**	
Quantity produced:	**75**	**100 %**

Component status



Routers		
Quantity required:	20	
Quantity produced:	25	100 %

Control & HW analysis & DAQ

Advanced: SPD can be controlled and configured with the final ALICE software

Installation

- Installation mid February
- ALICE tracker system is installed as first detector
- No access afterwards for 3 month
- No intervention possible

Installation

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- ALICE tracker system is installed as first detector
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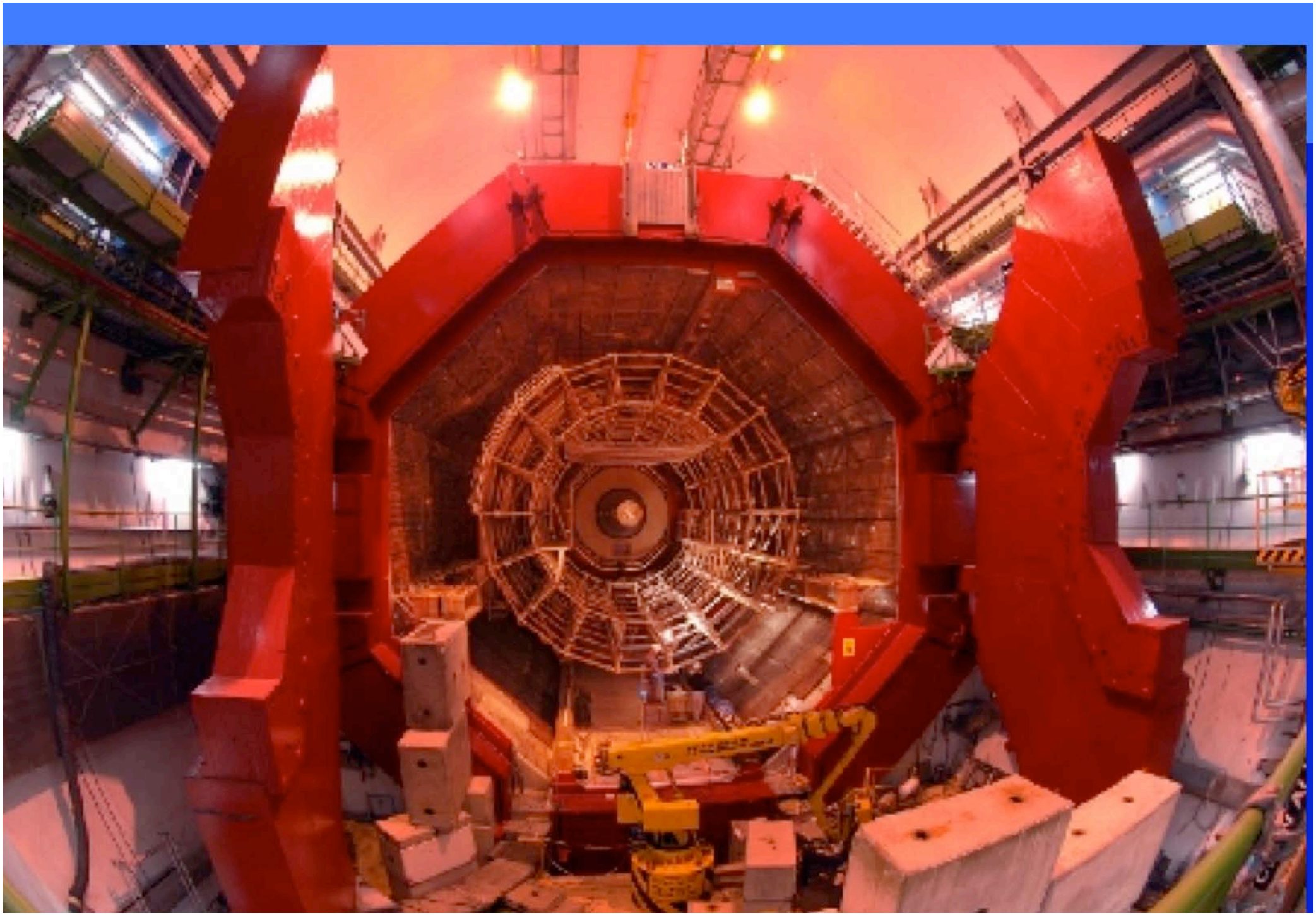
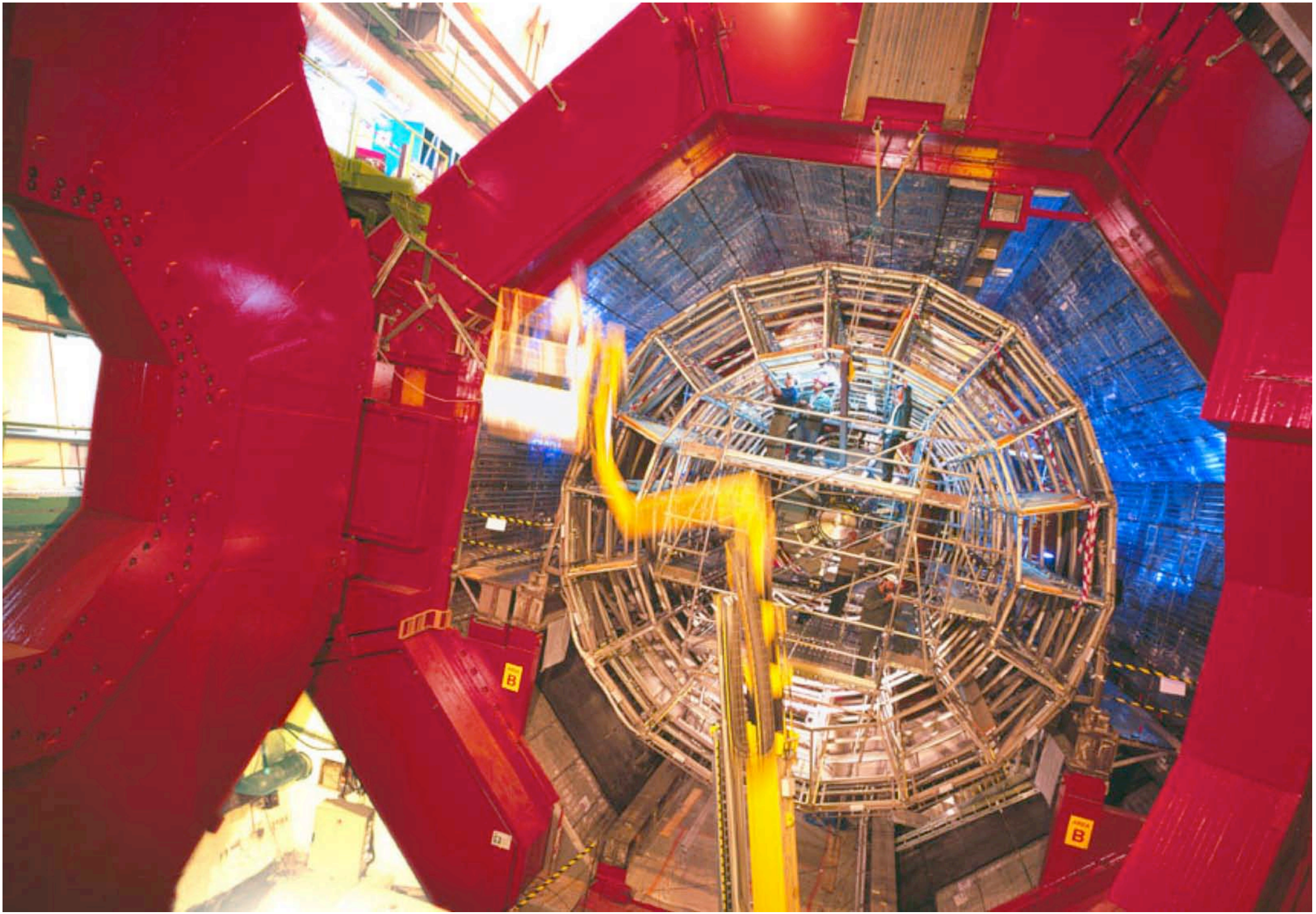
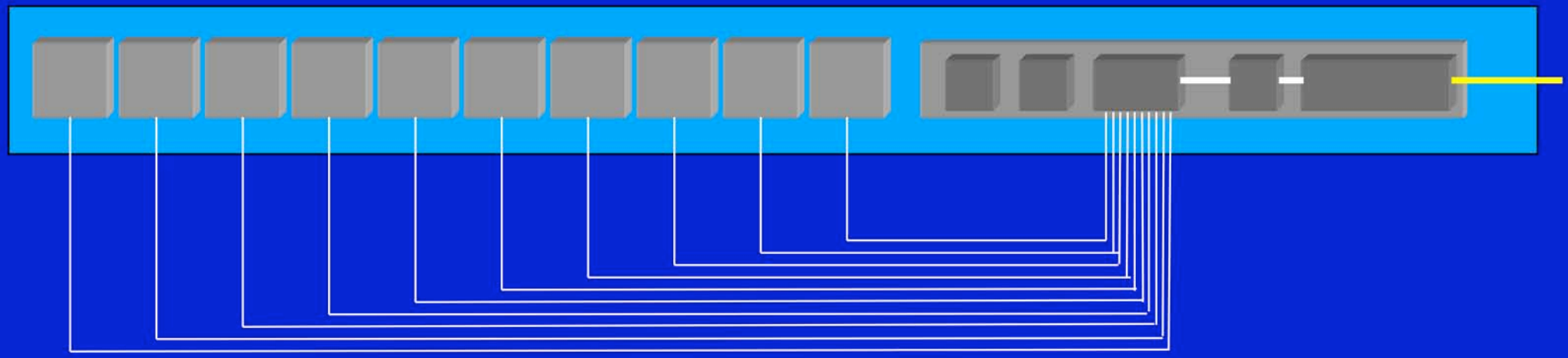




L0 pixel trigger

A. Kluge

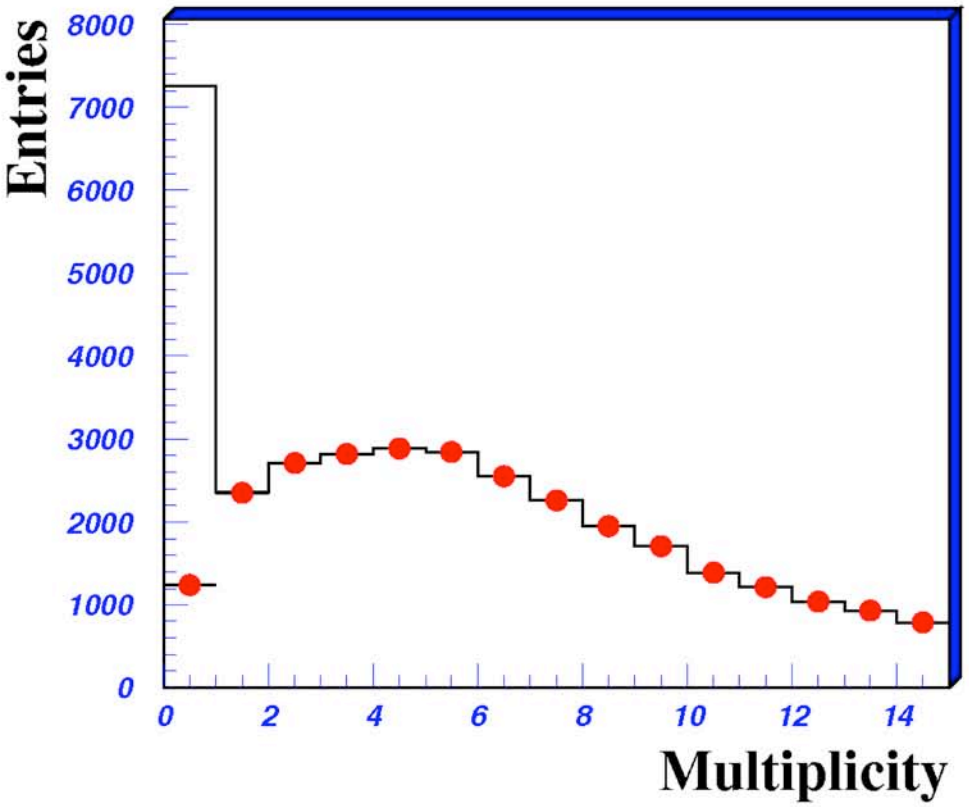
FastOr generation



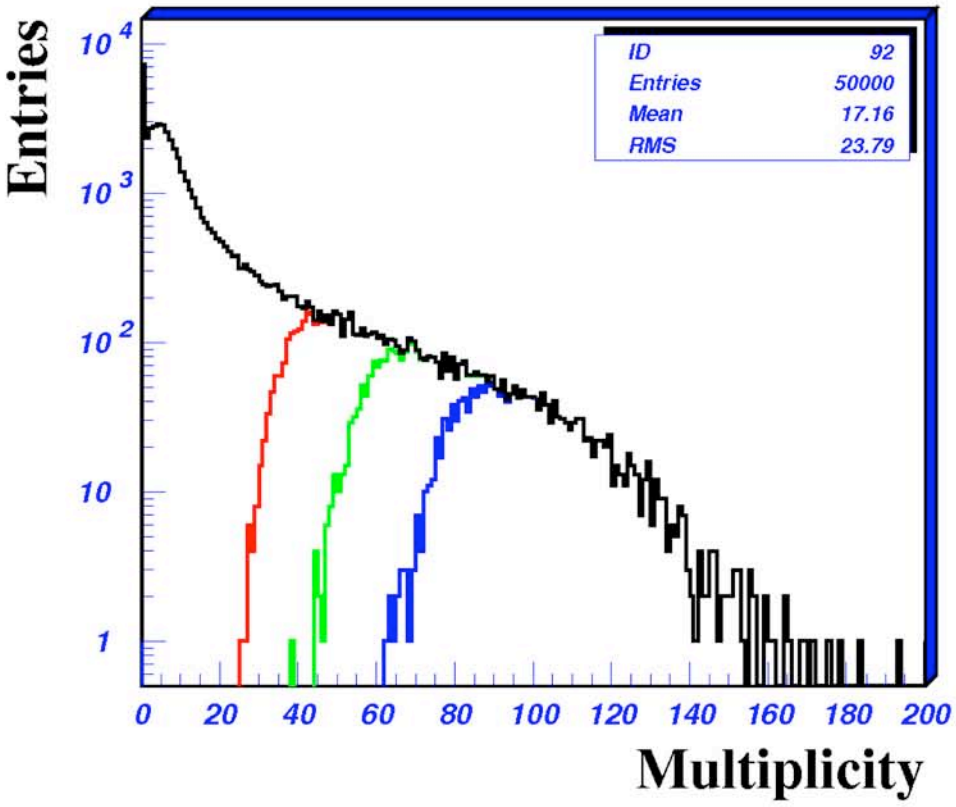
120 x half staves each 10 bit fastOr

Pixel trigger

Minimum bias

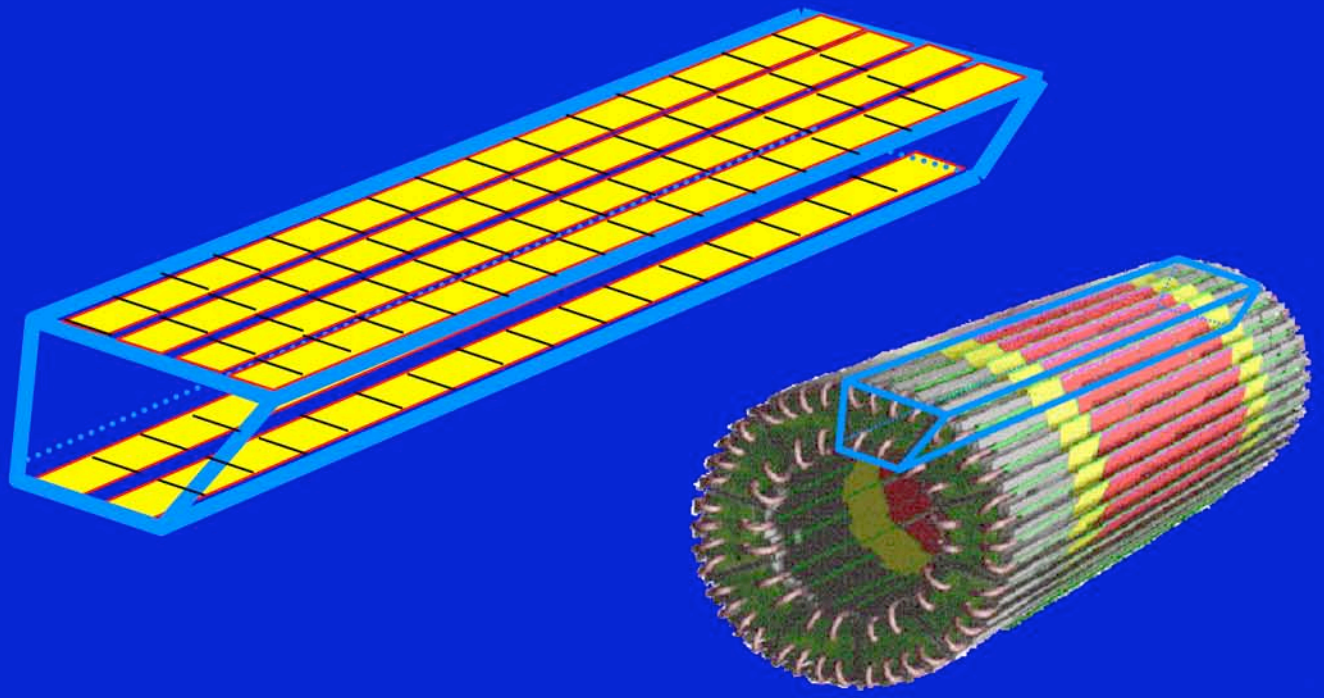


Multiplicity



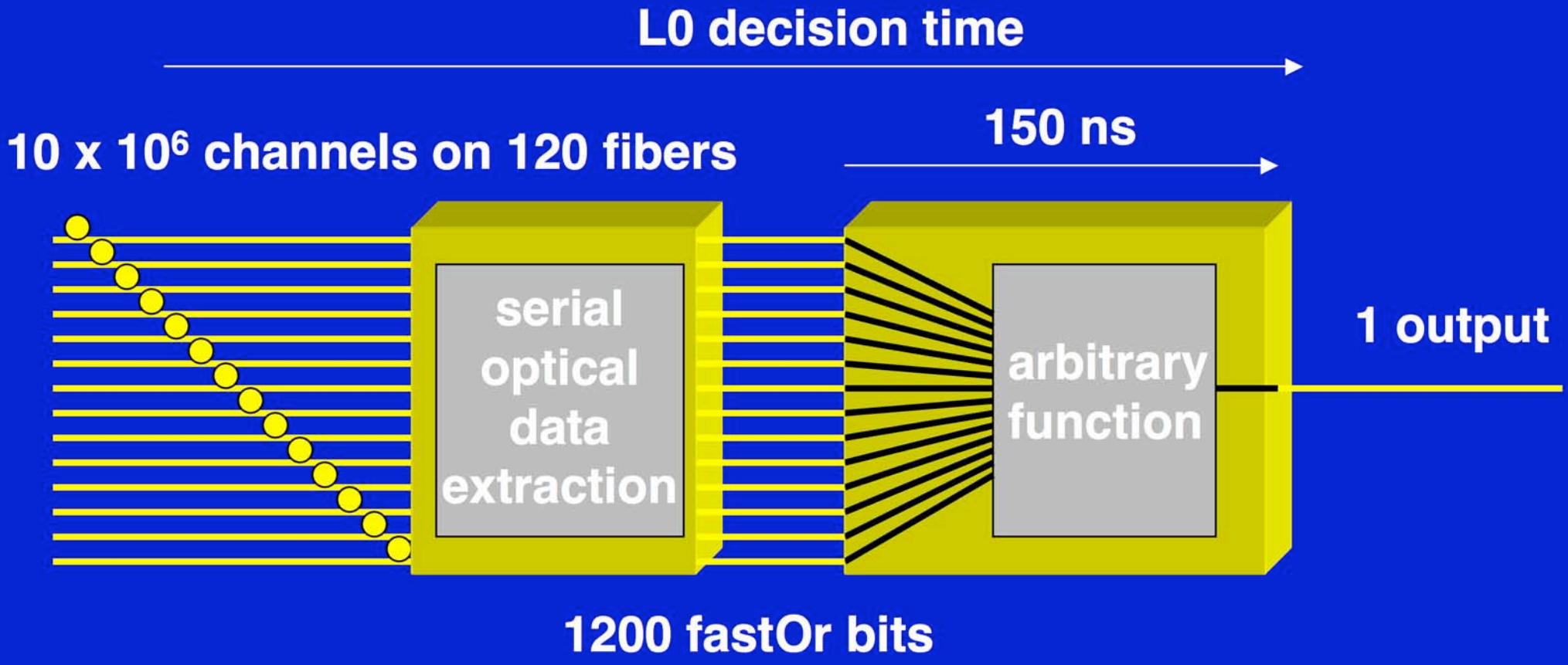
Example of algorithm

Layer
Sector
Half sector
Sliding Window
Vertex
Upper Cut
Topological

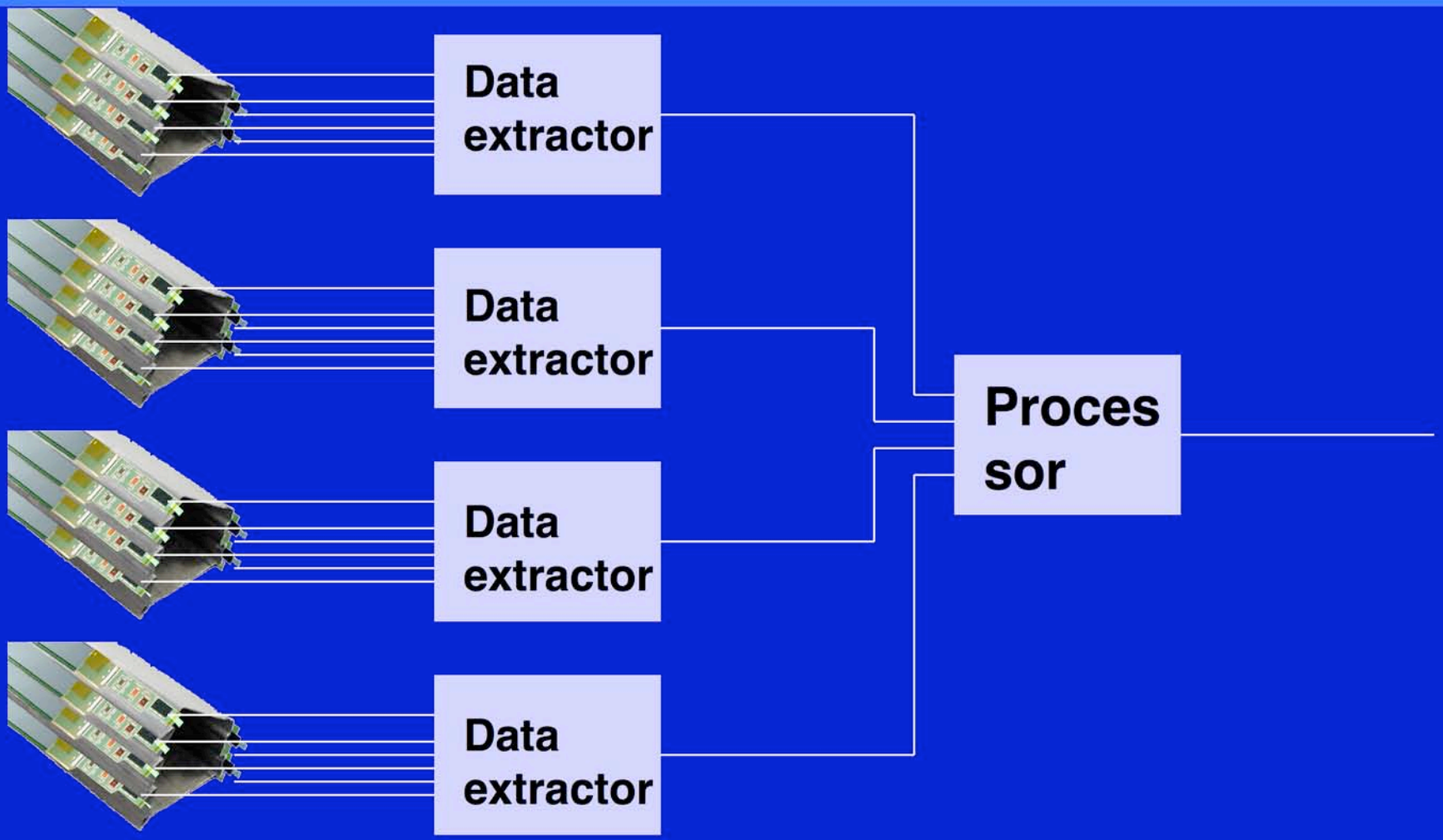


Implementation architecture does not limit the trigger algorithm

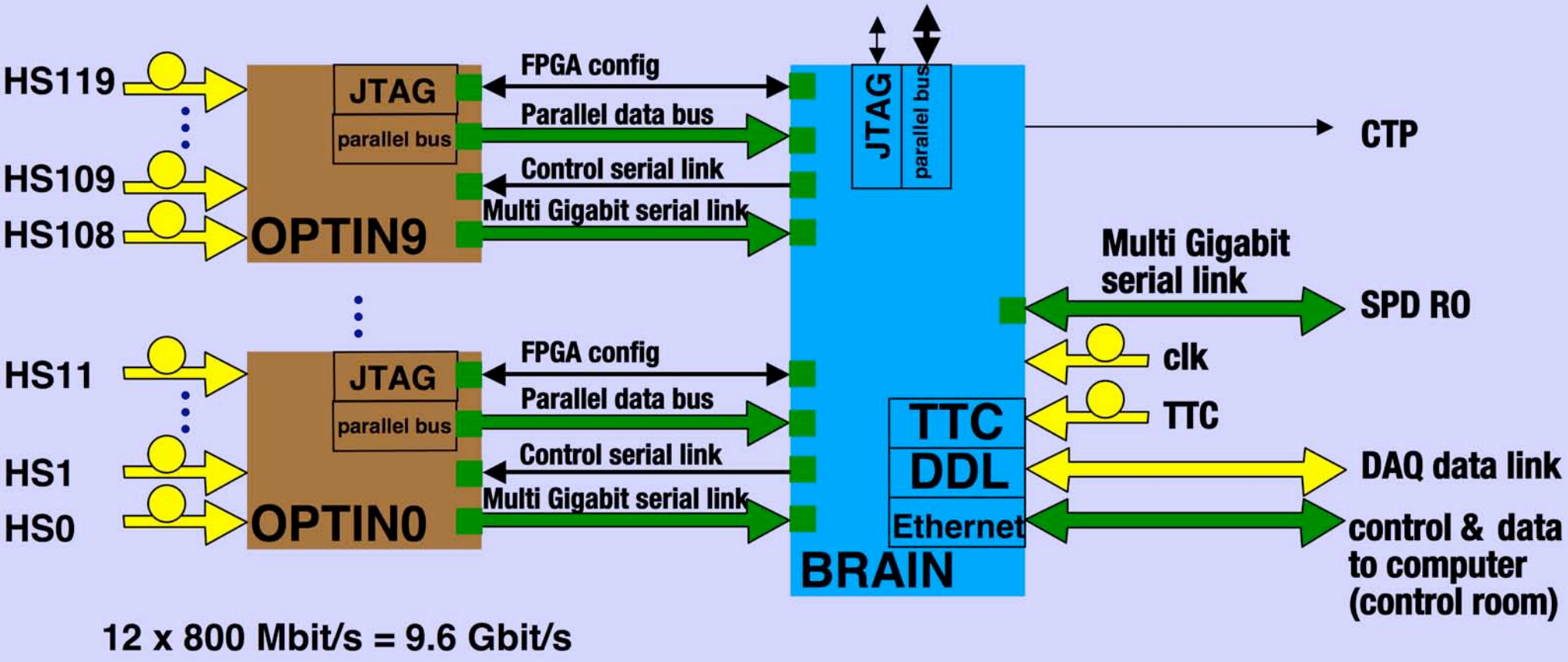
Pixel trigger



Architecture



ALICE pixel trigger processor



12 x 800 Mbit/s = 9.6 Gbit/s

Conclusion

- After a long R&D phase we know how to build the detector
- We have a complete detector system built up in the clean room
- 50% of the detector already is available