The ALICE Silicon Pixel Detector

A. Kluge[a,*], G. Aglieri Rinella[a], G. Anelli[a], F. Antinori[b], A. Badala[c], M. Burns[a], I.A. Cali[a,d], M. Campbell[a], M. Caselle[d], S. Ceresa[a], P. Chochula[a,e], R. Dima[b], D. Elias[d], D. Fabris[b], R.A. Fini[d], F. Formenti[a], M. Krivda[a,f], V. Lenti[d], F. Librizzi[c], V. Manzari[d], M. Morel[a], S. Moretto[b], F. Osmic[a], G.S. Pappalardo[c], A. Pepato[b], A. Pulvirenti[c], F. Riggi[c], L. Sandor[g], R. Santoro[d], F. Scarlassara[b], G. Stefanini[a], C. Torcato Matos[a], R. Turrisi[b], H. Tydesjo[a], G. Viesti[b]

[a] *CERN, Geneva, CH-1211 Geneva 23, Switzerland*
[b] *Dipartimento di Fisica dell'Universita' and Sezione INFN di Padova, Italy*
[c] *Dipartimento di Fisica dell'Universita' and Sezione INFN di Catania, Italy*
[d] *Dipartimento di Fisica dell'Universita' and Sezione INFN di Bari, Italy*
[e] *Comenius University, Bratislava, Slovakia*
[f] *Slovak Academy of Sciences, Kosice, Slovakia*

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Abstract

The ALICE Silicon Pixel Detector forms the two innermost layers of the ALICE inner tracker system. It contains 9.8 x 10^6 pixels with a material budget of less than 1 % per layer. It is based on hybrid pixel technology. The space and material budget constraints have severe impact on the design implementation. The ALICE detector system components are discussed.

Keywords: Hybrid pixel detector; ALICE

Detector configuration

The ALICE silicon pixel detector (SPD), which forms the two innermost layers of the inner tracker system (ITS), consists of 120 detector modules (half-staves) mounted on 10 carbon fiber support sectors [1]. In each sector, 8 half-staves are mounted on the outer layer and 4 on the inner layer. One half stave consists of two hybrid pixel sensor ladders, each with 5 pixel chips, bump-bonded to one sensor, and one multi chip module (MCM) for control and readout. The SPD contains 9.8 x 10^6 pixels in 1200 read-out chips covering a surface of 0.2 m^2 (see fig. 1).

* Corresponding author.
E-mail address: alexander.kluge@cern.ch

On-detector components

Pixel read-out chip

The ALICE pixel read-out chip has been designed in a 0.25 µm CMOS process. The chip contains a pixel matrix of 8192 cells organized in 256 rows and 32 columns. The pixels are 425 µm x 50 µm in dimension. The read-out chips are diced out of 200 mm diameter wafers that have been thinned down to 150 µm thickness after bump deposition. The average production yield of the chip is ~60% [2].

The operation principle is based on a fully binary read-out. Each pixel cell contains a delay element where the pixel hits are stored during the L1 decision

time of 6.5 µs. In case of a positive L1 trigger decision the hit data are moved into one out of four multi-event buffers. Upon reception of a positive L2 trigger signal the data in the corresponding multi-event buffer are stored in a read-out buffer from where they are sent sequentially to a 32 bit output bus [2].

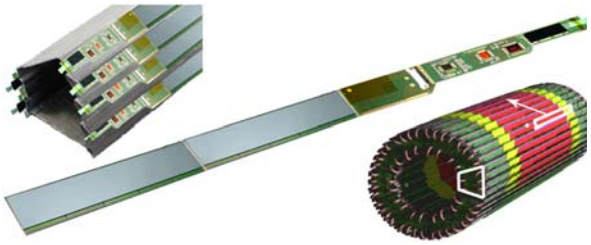

Fig. 1: Artistic view of the components in a half stave, of one sector and a CAD drawing of the SPD.

Sensor and Sn-Pb bump-bonding

For each half stave two p-in-n silicon sensor with dimensions of 72.72 mm x 13.92 mm and a thickness of 200 µm are used. 5 read-out chips are bump-bonded to one sensor with Sn-Pb bump bonds of 25 µm diameter to form a ladder (see fig. 2). The production yield of a ladder (dicing of tested chips of a wafer, bump bonding to a tested sensor element) is 64 % [2]. The failure modes of rejected modules are high leakage current (> 2 µA), more than 1% of bump connections missing (≥ 82 bumps) and damaged read-out chips .

Read-out multi chip module and read-out ASICs

The read-out, control and configuration is performed by a five layer Kapton-based on-detector multi-chip module (MCM) of 110 mm x 11 mm x 2 mm dimensions. Communication to the control room is established with 3 single mode 1310 nm optical fibers, two carrying configuration and trigger data and the clock and one carrying the read-out and monitoring data. The MCM contains 4 ASICs - the digital PILOT, ANAPIL, GOL, Rx40 - and an optical package containing two receiver diodes and one laser. All ASICs have been produced in a 0.25 µm CMOS technology with radiation hardening layout techniques [3]. The Rx40 converts the optical input signals to electrical signals. The PILOT chips receives the data stream from the Rx40 serial-parallel converts the data and forwards trigger and configuration commands to the 10 pixel chips. Furthermore it sends the pixel chip read-out data to the 800 Mbit/s G-link compatible GOL chip which is connected to the laser in the optical package.

All ASICs except the Rx40 are produced in multi-project-wafer runs and are delivered already diced. As testing diced chips is cumbersome and experience shows that the yield of the GOL is higher than 98% a similar yield for PILOT and ANAPIL was assumed. PILOT, ANAPIL and GOL are used as unpackaged dies and are wire bonded untested directly to the MCM substrate. The production yield of the MCM is 87 %. All MCMs are mounted and temporarily wirebonded to a test board which emulates the pixel chips and the off-detector electronics for an acceptance test and a burn-in procedure.

On-detector electronics integration

Each half stave is 12 mm wide and 3 mm thick. The material budget of each layer including support and cooling is 1% X_0. In order to achieve these parameters lightweight materials were applied as much as possible (carbon fiber, thinned silicon). Figure 3 shows all on-detector components. The pixel readout chips are connected to the power supply and the read-out MCM module employing a 5-layer aluminum-Kapton based flat cable - the pixel bus - and copper Kapton flat cables (extenders). The pixel chips and the MCMs are connected to the bus via wire bonds. In order to avoid vias between the layers for the power supply and

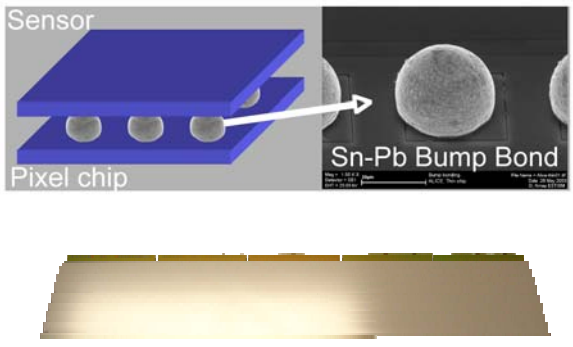

Fig. 2: Bump bond (top) and sensor ladder (bottom)

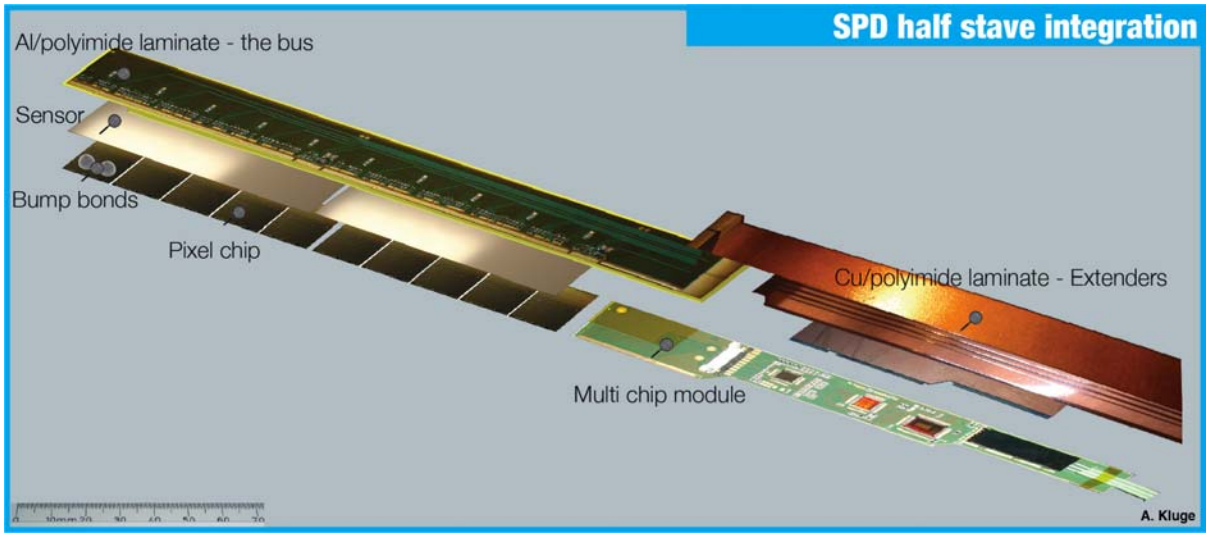

Fig. 3: Half stave components arranged in their order of assembly.

ground connections the internal layers are accessible for wire bonding from the outside employing a stair case like structure. Figure 4 illustrates the principle. The 80 µm wide Al-wire bonding pads are not compatible with standard printed circuit testers (flying probes). Thus each bus is temporarily bonded to a test card were all 800 wire bonds are connected to an FPGA based test station [5].

Half stave production

The assembly procedure is illustrated in fig. 3 and shows in order of assembly, the grounding foil acting as shield between the carbon fiber support and the electronics elements, the sensors with the pixel chips,

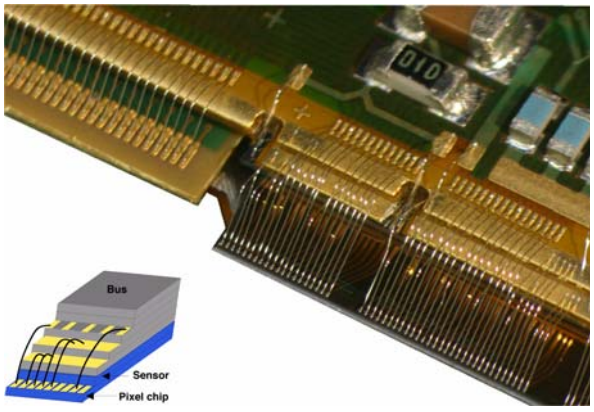

Fig. 4: Image of the wire bonds between the bus and the pixel chips (on the left) and the bus and the MCM (on the right).

the MCM with its protection lid, the optical fibers, the pixel bus with the wire bond connections and surface mounted passive components and the extender cables [5]. The half stave components are aligned and glued (Eccobond 45, [6]) using a coordinate measuring machine (Mitutoyo), equipped with dedicated tools and jigs and surveyed with a precision of 10 µm. Each half stave is tested in an automated way after production. The half stave production has an average yield of ~90 %.

Sector assembly

Half staves are mounted onto the carbon fiber sectors with carbon fiber clips and UV glue droplets to hold them in place. Thermal grease establishes the thermal contact between the half staves and cooling tubes embedded in the carbon fiber support. All half staves of each sector are connected to the cooling and tested individually. Thermal camera images of the assembled sectors verify the quality of the thermal contact. Figure 5 shows an assembled sector.

Off-detector components

Read-out electronics

VME and FPGA based electronics in the control room act as interface between the trigger data from the

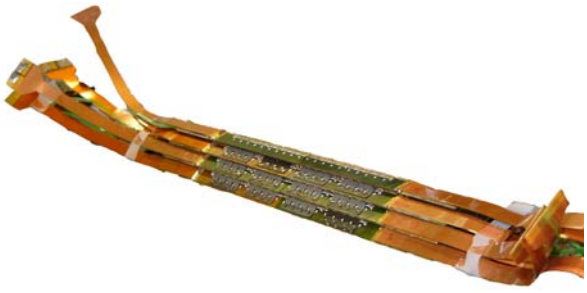

Fig. 5: Image of one SPD sector; power supply connections on the left and right; the eight outer layer half-staves visible in the middle.

ALICE central trigger processor system, the on-detector electronics and the computer based ALICE data acquisition system (DAQ). 20 9U-VME processor cards (router) which carry each three 2-channel plug-in type daughter cards (link receiver) are connected to the detector with optical fibers. Each router with its three link receiver cards is connected to one half sector (six half staves). The router and link receivers send the trigger and configuration data, receive the read-out data, perform zero-suppression and re-format the data before sending them to the ALICE DAQ via optical fibers (see fig 6). [7]

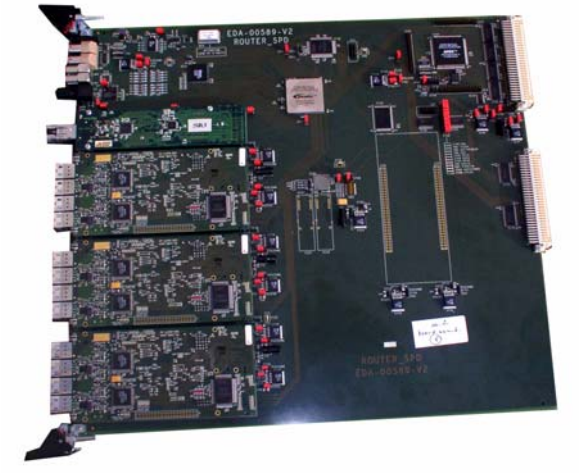

Fig. 6: One router card with three link receivers.

Detector control and configuration

The detector is controlled via the ALICE detector control system which accesses the router via the VME interface and the ALICE detector data link (DDL) interface on the routers. The hardware architecture allows access to data for monitoring and analysis while the read-out to the ALICE DAQ is active on the DDL. The SPD control system is based on a commercial Supervisory Control and data acquisition (SCADA) named PVSS. Five PVSS projects are running independently on different working nodes to control, the cooling system, the power supply system, the interlock and monitor system and the frontend electronics; the fifth project links together and monitors the 4 subsystem projects. An automated system is designed to allow fast calibration procedures even during the LHC fill time (~ 70 min.)[8].

Infrastructure, interlock and cabling

Although the detector occupies the volume of only 3 dm^3 considerable effort goes into planning and installation of cables and optical fibers. As the ALICE installation scheme foresees several break points with patch panels the number of cables for the SPD installation is with ~1800 relatively high. Low voltage power supply crates are located in some 40 m distance from the detector. No local voltage regulators are used. The high voltage power supply and the read-out electronics is located in the counting room with a distance of 115 m to the detector.

In order to protect the SPD from overheating in case of cooling failure or electronics malfunction temperature sensors are installed directly on the half staves, the MCM and the cooling pipes. The sensors can be read either by the optical links from the detectors or by wires. Three safety interlock systems work in parallel [8]. The software based detector control system monitors the temperature values and switches off the power supplies via software commands. In the second system the FPGA based control room located read-out system (router) compares the temperature values received via the optical links with thresholds and switches off the power supplies using the hardware interlock inputs of the power supplies. The last system reads the values using the wire-connection to the sensors using analog programmable logic controllers modules (PLC) which also directly act on the interlock inputs of the power supply modules.

Integration and installation

All assembled sectors are connected to the cooling circuit and tested on the surface in a clean room located at CERN before being integrated. 5 sectors are assembled to form one half barrel. In the clean room the final ALICE detector system including the final components such as half staves, off-detector read-out electronics, power supplies, optical fibers, interlock system, cooling system and cables with final cable length is built up.

The ALICE L0 pixel trigger system

The fastOr-output of the SPD pixel read-out chip indicates whether at least one out of the 8192 pixel has been activated during a 100 ns clock period. The fastOr signals of all 1200 read-out chips are transmitted to the pixel trigger system and processed to generate a ALICE L0 trigger input signal. Several trigger algorithms have been investigated [9] for implementation in the processor. A maximum processing latency of 800 ns including cable delays is targeted. Consequently the pixel trigger processor must be located in the ALICE cavern as close as possible to the ALICE central trigger processor as otherwise the cable delays would be too large. The fastOr signals of all 1200 read-out chips are transmitted via the optical links on MCMs of the 120 half staves off the detector. The optical path is split passively to the SPD read-out in the control room and to the pixel trigger processor in the ALICE cavern. The processor system consists of a main processor board (BRAIN) controlled via an optical link from the control room. The BRAIN processor has 10 plug-in slots for 12-channel optical receiver cards (OPTIN) which serial-parallel convert the data stream, extract the fastOr bits and forwards them to the BRAIN card The actual processing of the pixel trigger algorithm is performed in the BRAIN processor [10].

Summary

The ALICE SPD has a material budget of 1 % X_0 and and is built up in two layers at radii of 3.9 cm and 7.6 cm, respectively. 10 x 10^6 pixels with the dimensions of 50 μm x 425 μm are contained in 120 detector modules (half staves) organized in 10 sectors. All components of the SPD detector and the detector system have been qualified. Presently it is being built up in a clean room at CERN before finally being installed in ALICE.

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