Considerations for a SLHC Pixel Tracker

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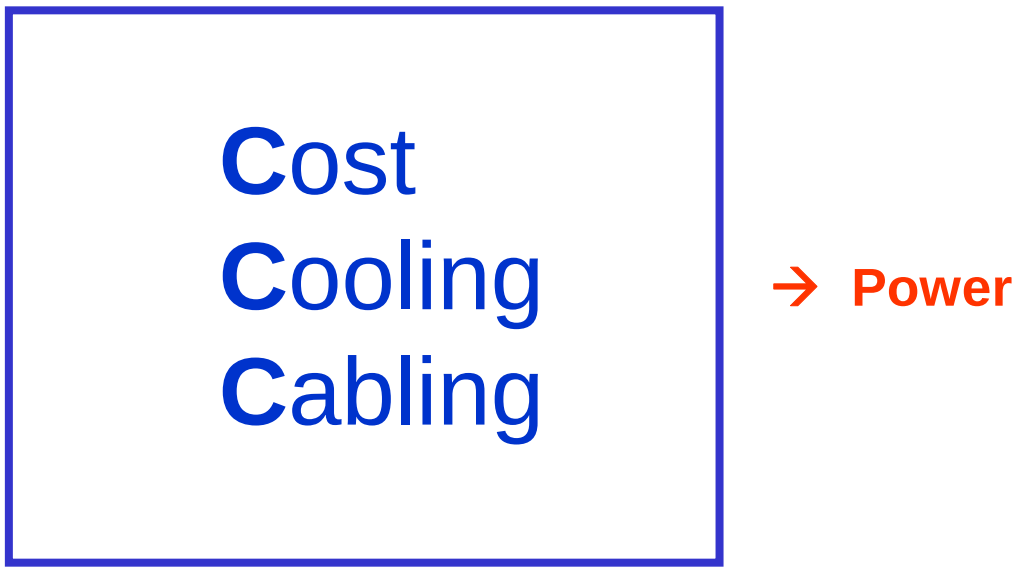

Cost
Cooling
Cabling
→ Power

• This talk is not about physics case of SLHC

• Benefits of 10 fold increase of luminosity may only be clear as real LHC data is analyzed and the Higgs/SUSY realization in nature becomes visible

however

• Detector upgrade in 2014 requires planning action already now ! (2006)

• 8 years not terribly much for :
- **Conception** of SLHC tracker
- **Basic R&D**
- **Protoyping**
- **Demonstators**
- **Production**
- **Installation & Commissioning**

• Should learn from current experience of LHC trackers !

• Many issues in this talk are valid for CMS & ATLAS as well.

- **LHC → SLHC** in phases:
  - phase 0/1 limited hardware upgrade → 3 - 5 x 10^{34} cm^{-2} sec^{-1}
  - phase 2 major hardware upgrade → 10 x 10^{34} cm^{-2} sec^{-1}

- No sharp step in Lumi → Running periods with CMS TOB still ok but TIB inadequate !

- Several years of LHC running
  - integrated rad. damage of present tracker reaches design limits
  - rates get too high

  → **Need a complete new tracker** !

- SLHC @ 10^{35} creates enormous problems with:
  - data rates
  - radiation damage
  - event selection

  → triggering with tracks ?

SLHC situation

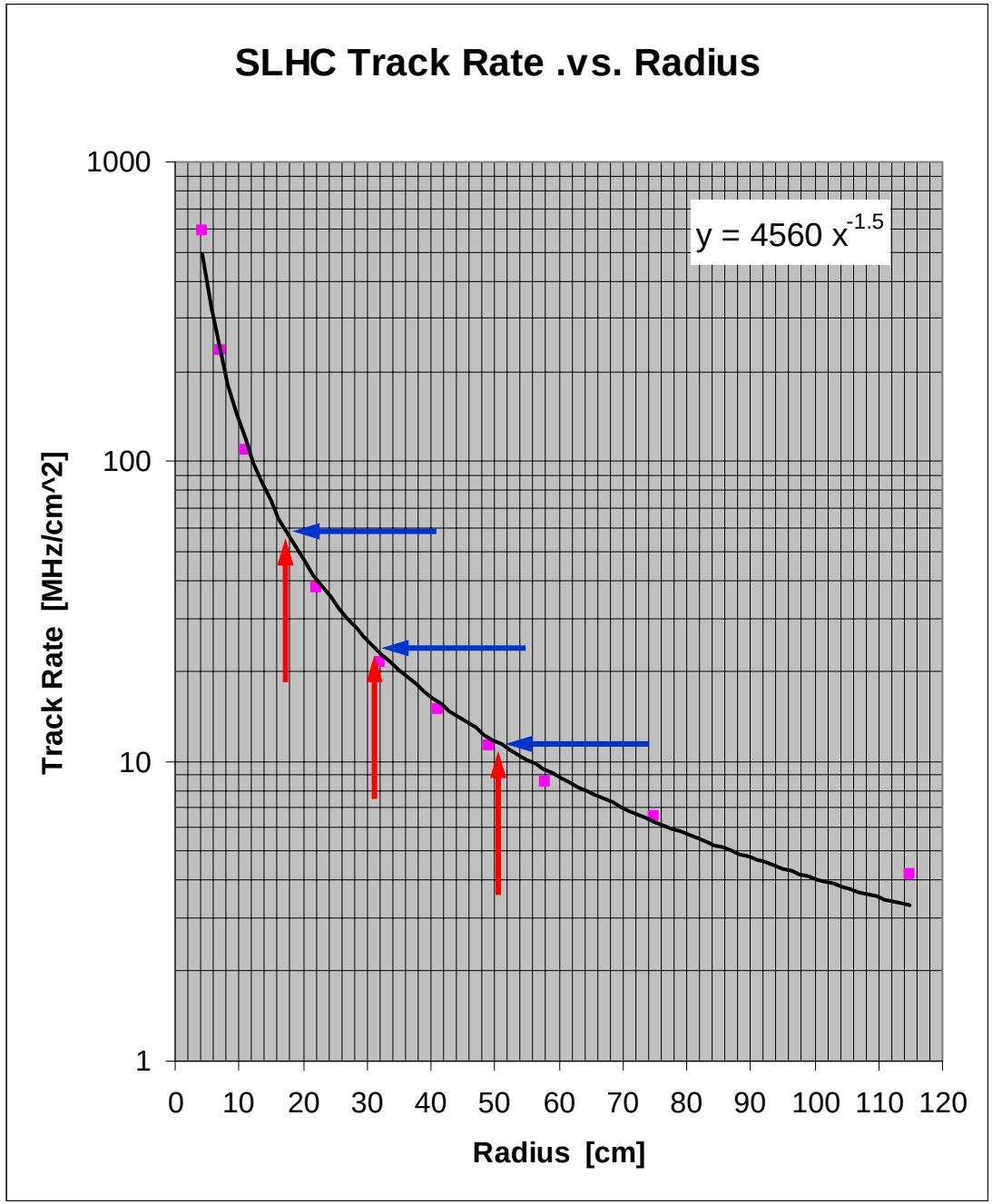
• Track rates at L = 10^{35} cm^{-2} sec^{-1}

•Technology already exists for SLHC tracking at radii > 20cm :

Silicon Pixels Detector

LHC Rates @10^{34}		SLHC Rates @10^{34}
r = 4cm	→	r = 18cm
r = 7cm	→	r = 30cm
r = 11cm	→	r = 50cm

• Performance of present pixels at SLHC?



SLHC rate tests of CMS Pixel Modules

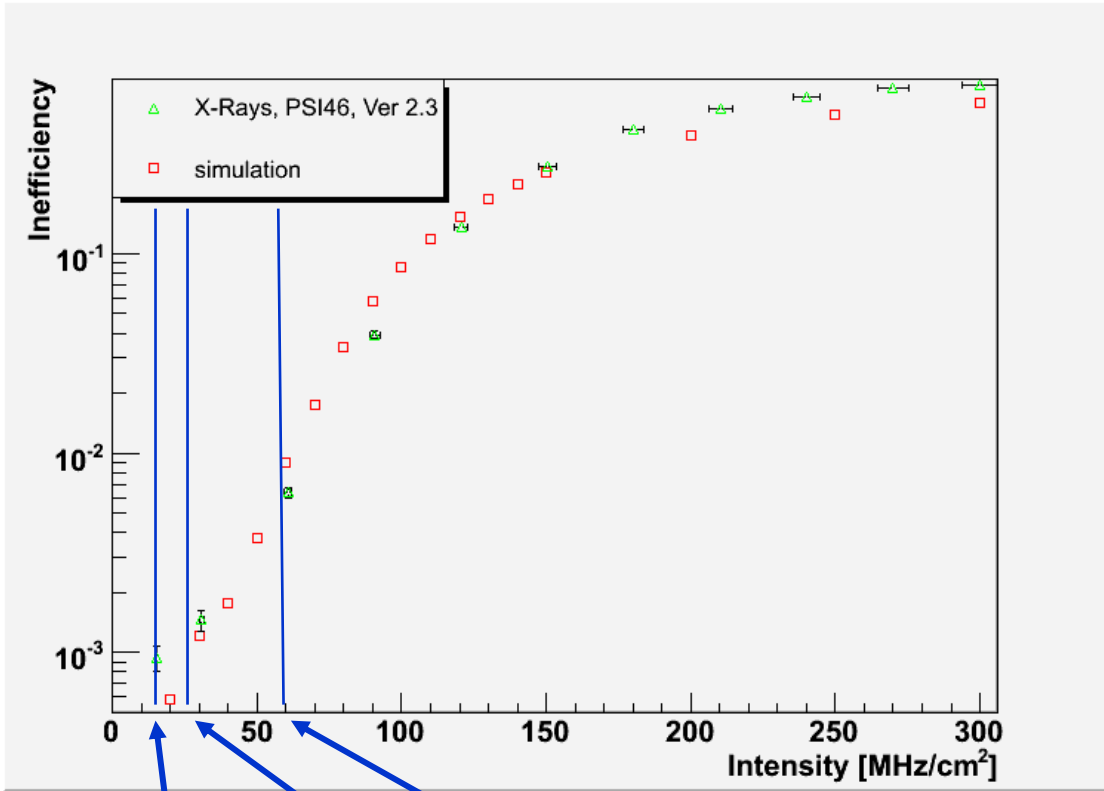
- High rate tests in X-ray box allows hit rates up to 300 MHz/cm^2

• Simulation of pixel read out chip (ROC) compares quite well with observed data loss

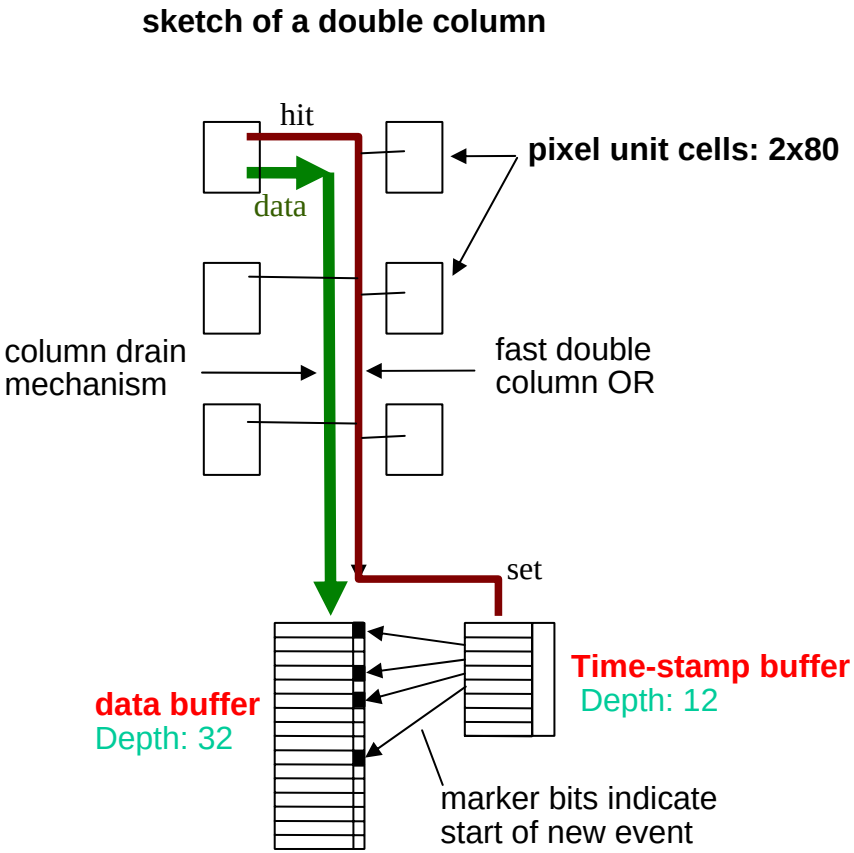
• We can identify the data loss mechanisms
  → finite data buffers
  → readout times

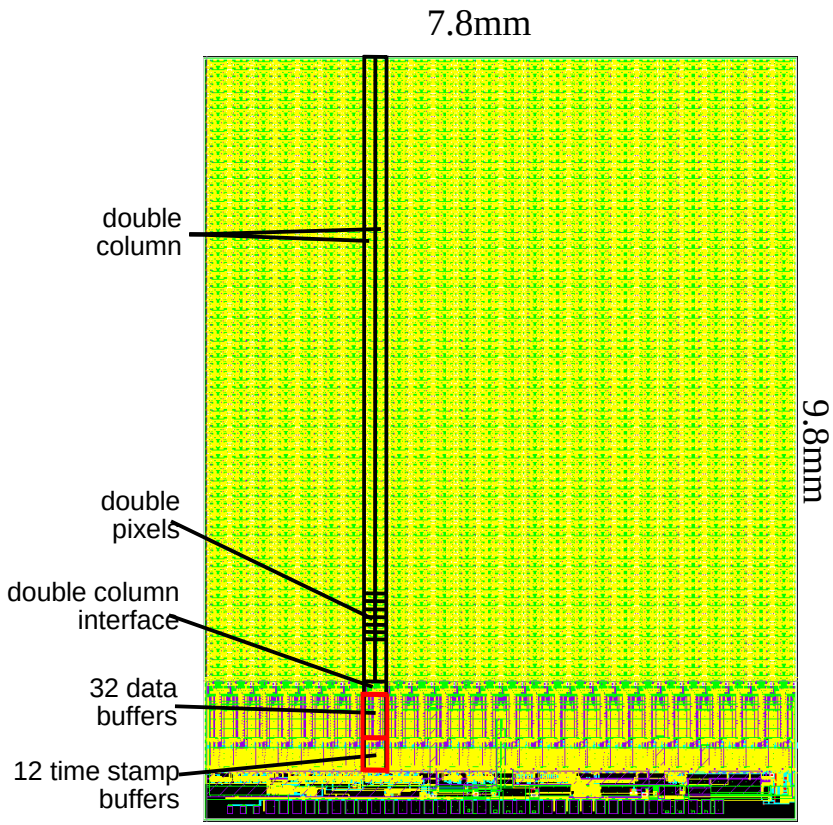
• For SEU studies and timewalk need to go to pion beam line at PSI

  → 150 MHz/cm^2
  → 20nsec bunch structure



CMS Pixel ROC: Column Drain Architecture





SLHC rate data losses dominated by finite buffer sizes !

→ **chip size !**

periphery bigger

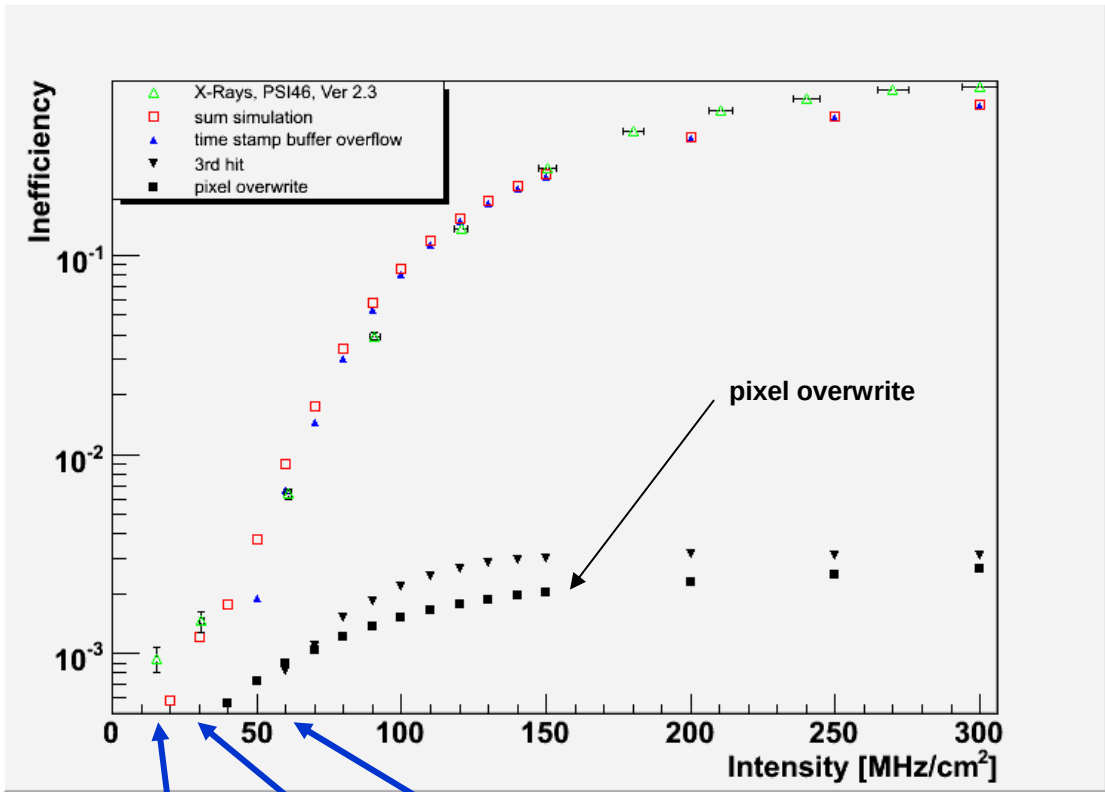
High rate data losses in x-ray test

- X-ray box (pix.mult.= 1)
  → timestamp buffer overflows dominant

- Pion beam (pix.mult.> 1)
  → data buffer overflow

- Loss due to pixel overwrite (~ pixel size) is not relevant

- Small pixels create large data traffic !

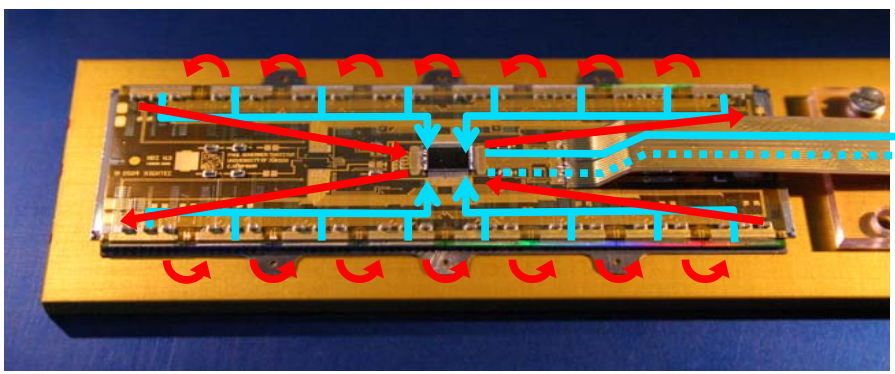


Evolutionary upgrade of CMS pixel modules

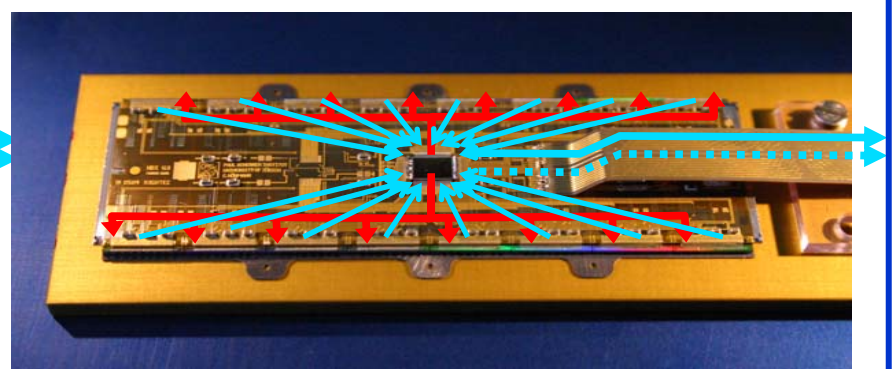
- CMS pixel modules need to be replaced. **(r=4cm every 2 years @ 10^{34})**
- LHC → SLHC has probably no sharp step in luminosity
- Can improve rate capability of present pixel modules by:
  - increase buffer size in ROC periphery **(2x in 0.25μm CMOS, 5x in 0.13μm)**
  - extra data buffer in redesigned TBM with parallel ROC read out scheme
- Replaced modules would be fully compatible with present system.

→ allows operation of present pixel system at L ~ 3x10 ^{34} cm^{-2} sec^{-1}

Present TBM Read Out Scheme



Future TBM Read Out Scheme



SLHC Pixel Tracking (zero suppressed readout)

- What are our priorities: - tracker for 10^{35} but same X/X_0 and resolution ?
  - reduce material budget (X/X_0) ?
  - improve resolution ($\Delta p/p$, impact parameter) ?
  - triggering (jet, track selection, impact parameter) ?

- Financial envelope for new Super LHC tracker ~ 115 – 120 MCHF

- How many technologies are radially needed to deal with

  - rates (wide range)
  - cost per unit area
  - minimal power per layer → minimal material budget (X/X_0)

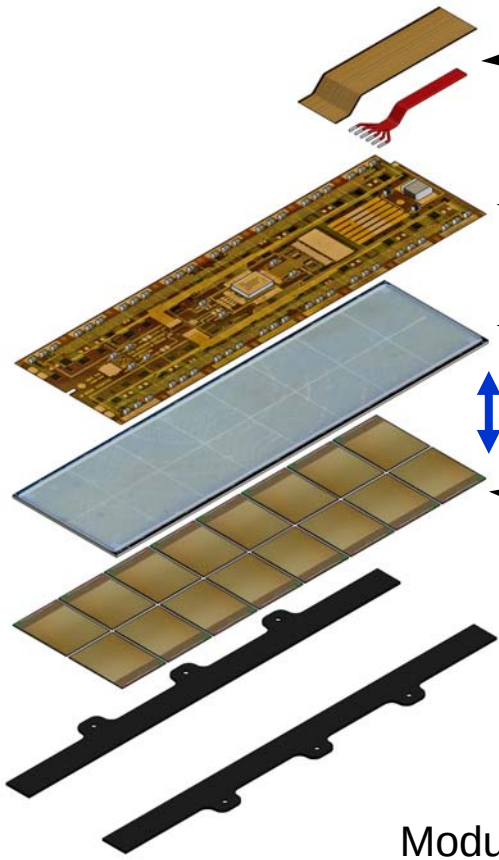
- Present Pixel System has radii : r = 4cm 7cm 11cm 15cm was to costly
  Layer cost go by area ~ r^2 = 16 49 121 225

- Present pixel works well under high rates but cannot be financed for r >18cm !

- Increasing layer radius r → cost per surface must scale **~ 1/ r^2** !

→ use cheaper technology, just adequate for rate at this layer radius !

Costs of a CMS Pixel Barrel Module



Cables (40cm) & TBM etc. 100 SFr

HDI (High Density Interconnect) 300 SFr

Sensor (DS, n^+ in n-Si) 800 SFr

Bump bonding 3200 SFr

16 Readout chips 0.25µ 250 SFr

(DMILL: 7200 SFr)

Baseplate (SiN) 50 SFr

Module of Area = 10cm2 Costs ~ 4700 SFr

Optical links, FED , FEC, Power supplies add +15% → ~550 SFr/cm2

Costing Speculations [CHF/cm^2]

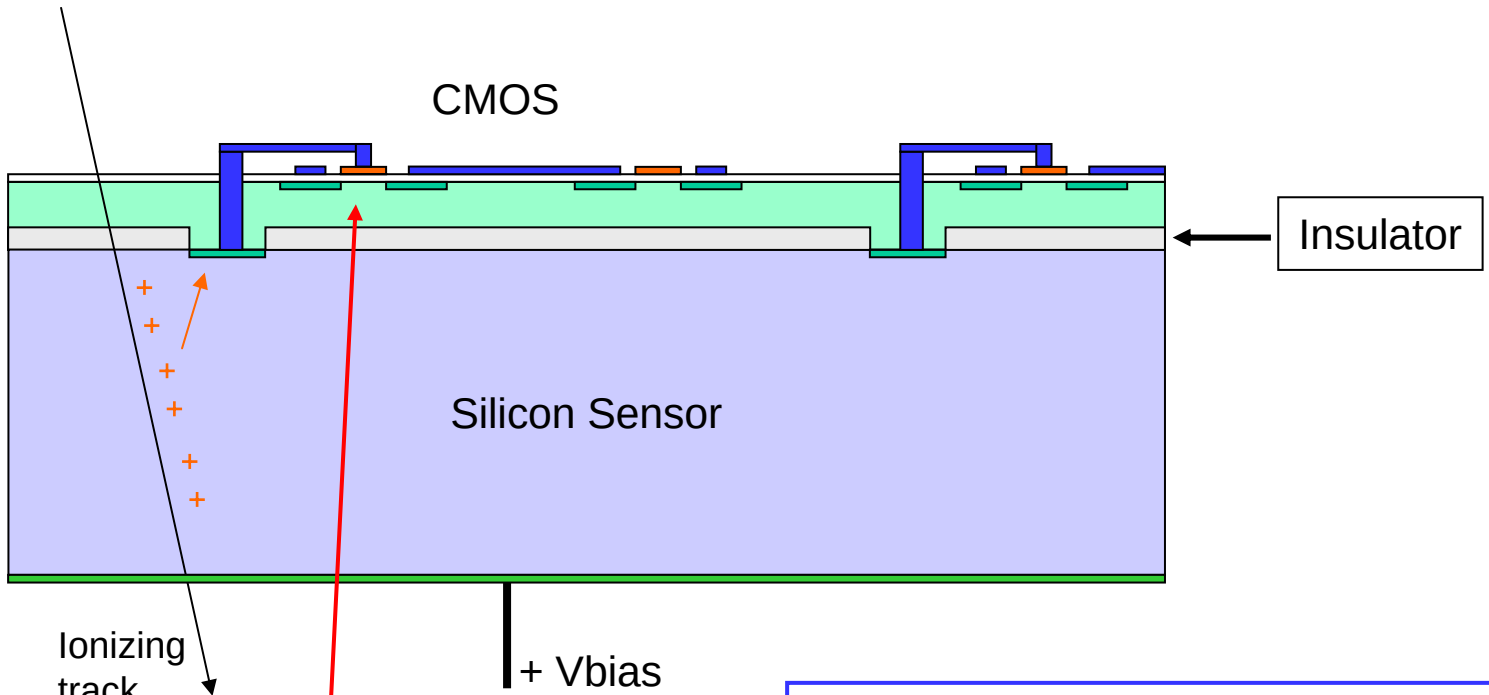
* = C4NP (IBM)

	Pixel (now)	Large pixels	Macropixels	MAPS	CMOS+Sensor
Pixel Area	0.015 mm^2	0.15 mm^2	1.5 mm^2	- - -	- - -
Sensor/ROC	1 / 1	1 / 1	10 / 1	0 / 1	1 / 1
Tiling unit	10 cm^2	40 cm^2	100 cm^2	4 cm^2	4 cm^2
Bumping	320	20*	2*	0	0
Sensors	80	10	10	0	10+10?(4)
ROC	25	50	2	50	200?(3)
HDI	30	30	3	30	30
Cables	8	8	0.8	8	8
Baseplate	5	5	0.5	5	5
Pitchadjust	0	0	15(2)	0	0
Optical Link (1)	32	6	0.6	6	32
pxFED	25	4	0.4	4	25
Total	**525**	**~130**	**~35**	**~105**	**~320?**

(1) ~ 320 CHF/channel
(2) ~ 0.02 CHF/cm fine pitch trace
(3) Yield speculations based on experience with DMILL SOI-wafers
(4) Extra cost for anodic wafer bonding or SOI wafer growth

CMOS+Sensor (Integrated)

Combine CMOS wafer with high resistive silicon sensor wafer in SOI technique !



E-fields of depleted sensor can disturbe CMOS FET's through back gate ! !

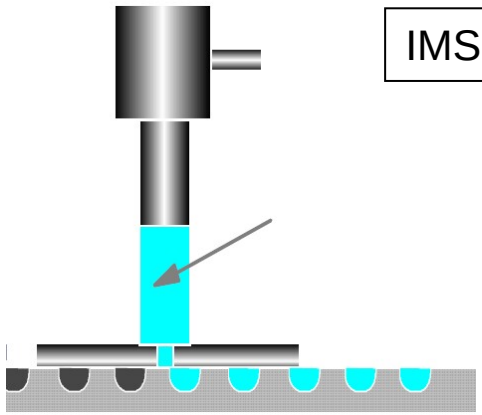
Historic case: DMILL (SOI-CMOS technology)

Yield (DMILL) ~ ¼ Yield (IBM 0.25μ)

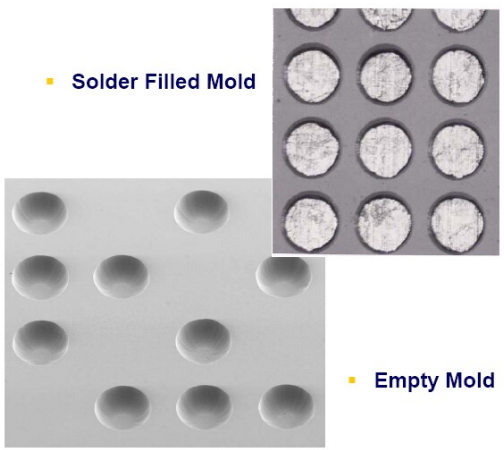
- SOI – defects on wafers (analog yield)
- low volume yield degradation (< 5k wafers)

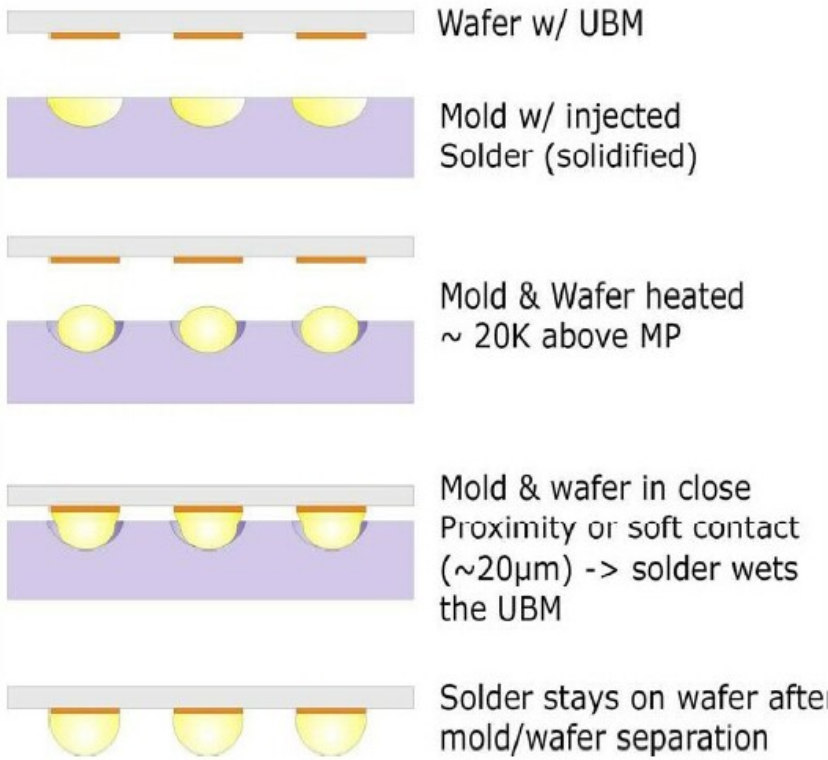
C4NP Low Cost Bumping Injection Molded Solder (IBM & Süss)

IMS Principle



Mold





- IMS allows bump 75µ size and pitch of 150µ
- 200µ thick wafers processed so far
- Wafer costs (300mm) ~ 150 $

Wafer Yield

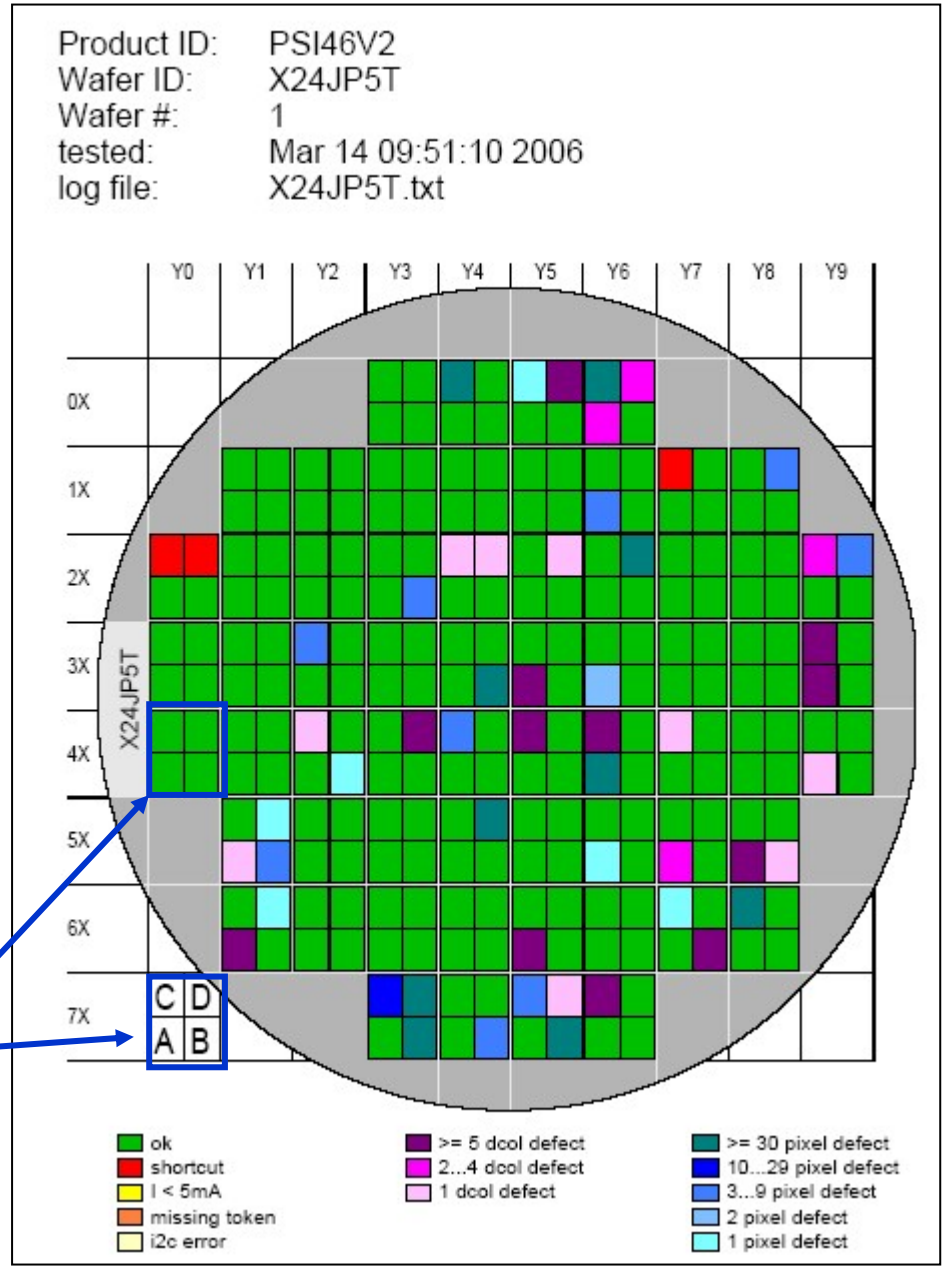
Example:

Present pixel ROC PSI46V2
Size : 8mmx10mm
Yield: ~ 80%

Future large pixel ROC
Size: 16mm x 20mm
Yield: 25/62 ~ 40% ~ $(0.8)^4$

(Average 5 wafer ~30%)

Chips arranged in blocks of 4
= 1 large chip (16mm x 20mm)



Cooling

Current Pixel Barrel System:

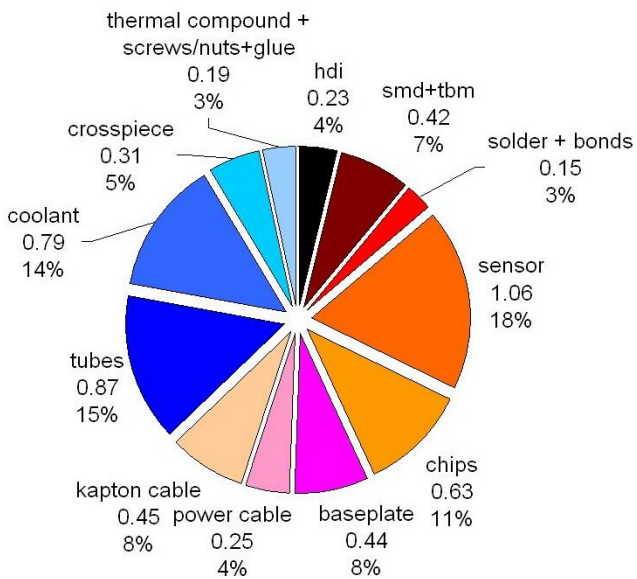
- Bring power in = 4%
  (On-Chip regulators,Al-wire)
- Take power out = 29%

Cooling is material budget driver !

Low mass cooling and/or

Reduce power consumption !

Material budget for 3 Layers at $\eta = 0$



X/X_0 = 5.79% for 3 barrel pixel layers

→ 1.93% / layer

Current consumption: Analog: Strips → reduce noise
Pixels → speed (timewalk) ! !

Digital: Information processing (data flow)

CMS ROC: I_D = 32mA no tracks
I_D = 40mA at 40MHz/cm² track rate

- Reduce power by :

  - Technology **CMOS 0.25μ → 0.13μ** → **Digital: local: YES global: NO**

    → **Analog: NO W.I.** → $g_m = \frac{I_{DS}}{n \cdot U_T}$

  - Architecture choice

		on chip regulators
Pixel ROC Power :	**ALICE 466 mW/cm²**	**no**
	ATLAS 335 mW/cm²	**no**
	CMS* 194 mW/cm²	**yes**
	CMS 142 mW/cm²	**no**

  - Custom protocols **TBM05 ~ 1/6 power of TBM03**

    abandon LVDS for 5cm distance → custom protocol LCDS (Low Current Differential Swing)

The next SLHC tracker must be very cautious and careful with power consumption !

Tracker Trigger (worry about **Cabling**)

- Present CMS System : Strip System → Zero suppression after L1 in FED
  Pixel System → Zero suppression before L1 in ROC

- Present Pixel System is only tracking system that could in principle participate in the L1 decision.

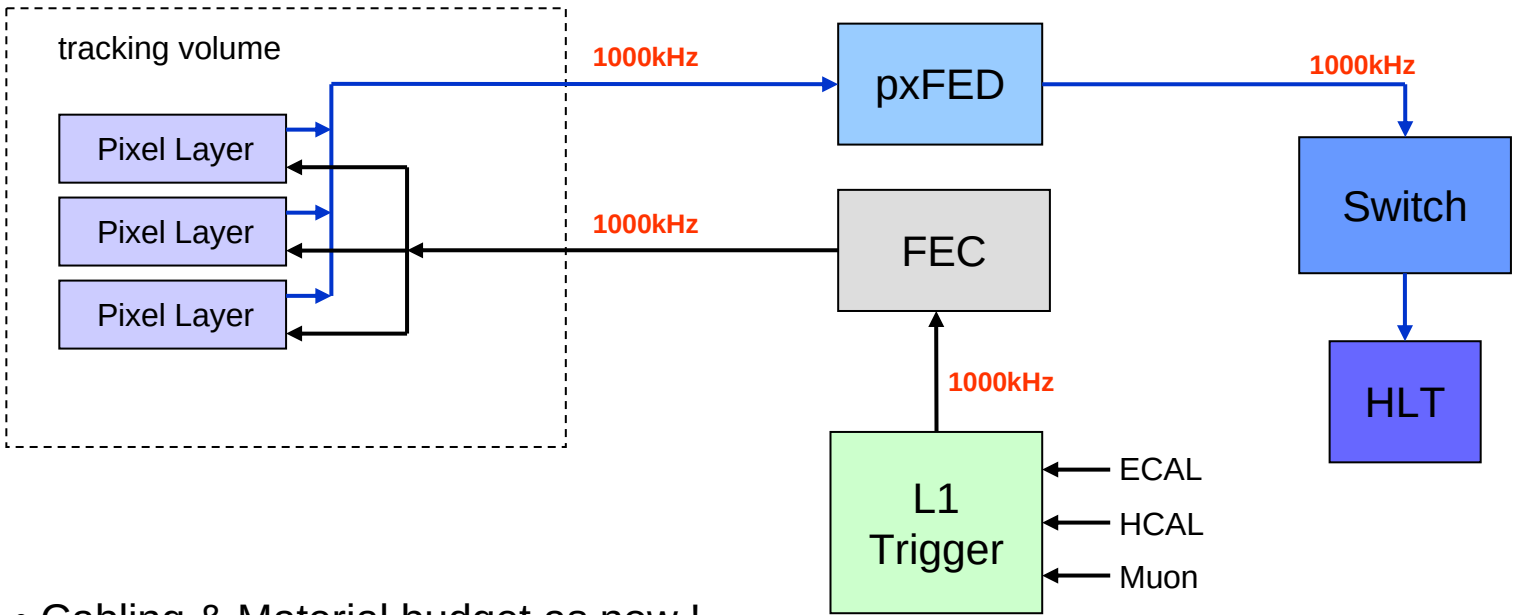
- Typical trigger concept relies on a quick and fast evaluation of (reduced) information for selection of valuable data for subsequent full event readout.

- SLHC tracker with 0-suppressed Pixel- / Strip-System could contribute to L1

→ What are our options ? e.g. CMS

Tracker Trigger (Option 0) → brute force solution

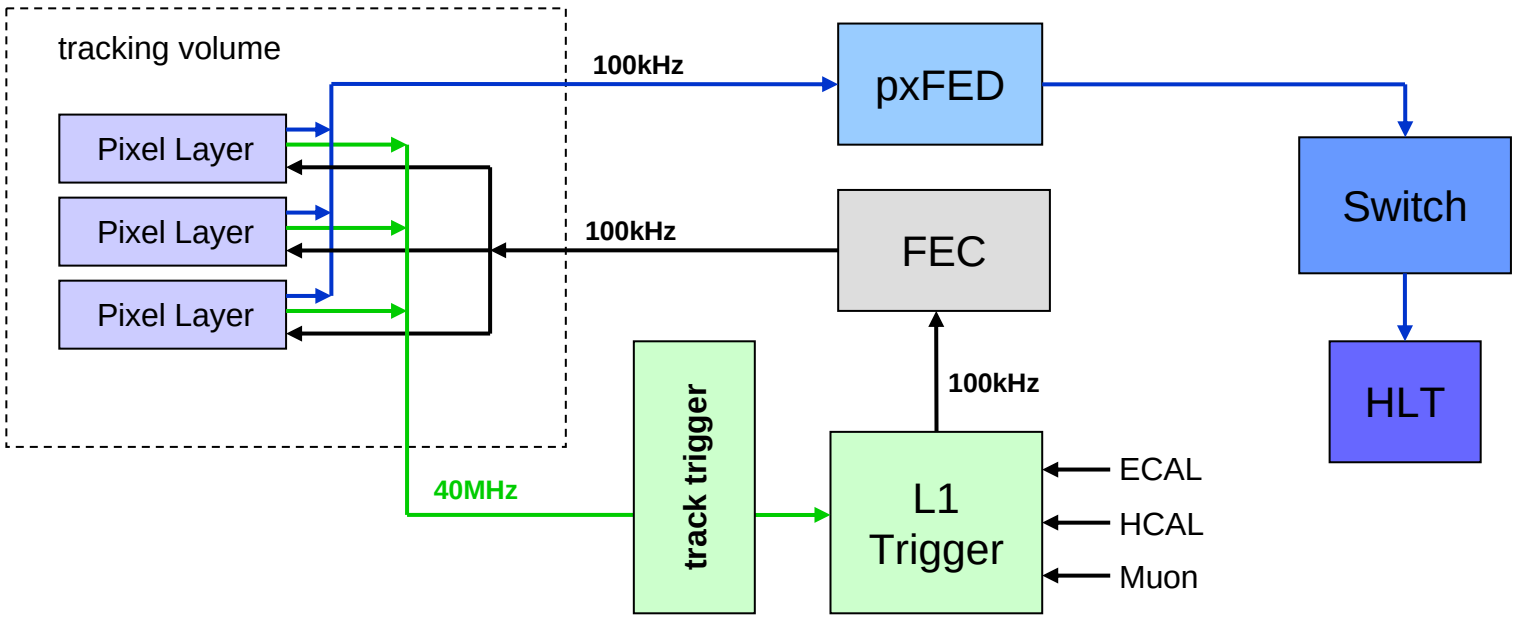
Keep present concept → Increase LT1 rate 100kHz → 1MHz !!



- Cabling & Material budget as now !
- Increase readout bandwidth by 10x , (rest of CMS as well) Costs !
- Increase Switch bandwidth for Tracker HLT decision ! → Affordable ?

Tracker Trigger (Option 1)

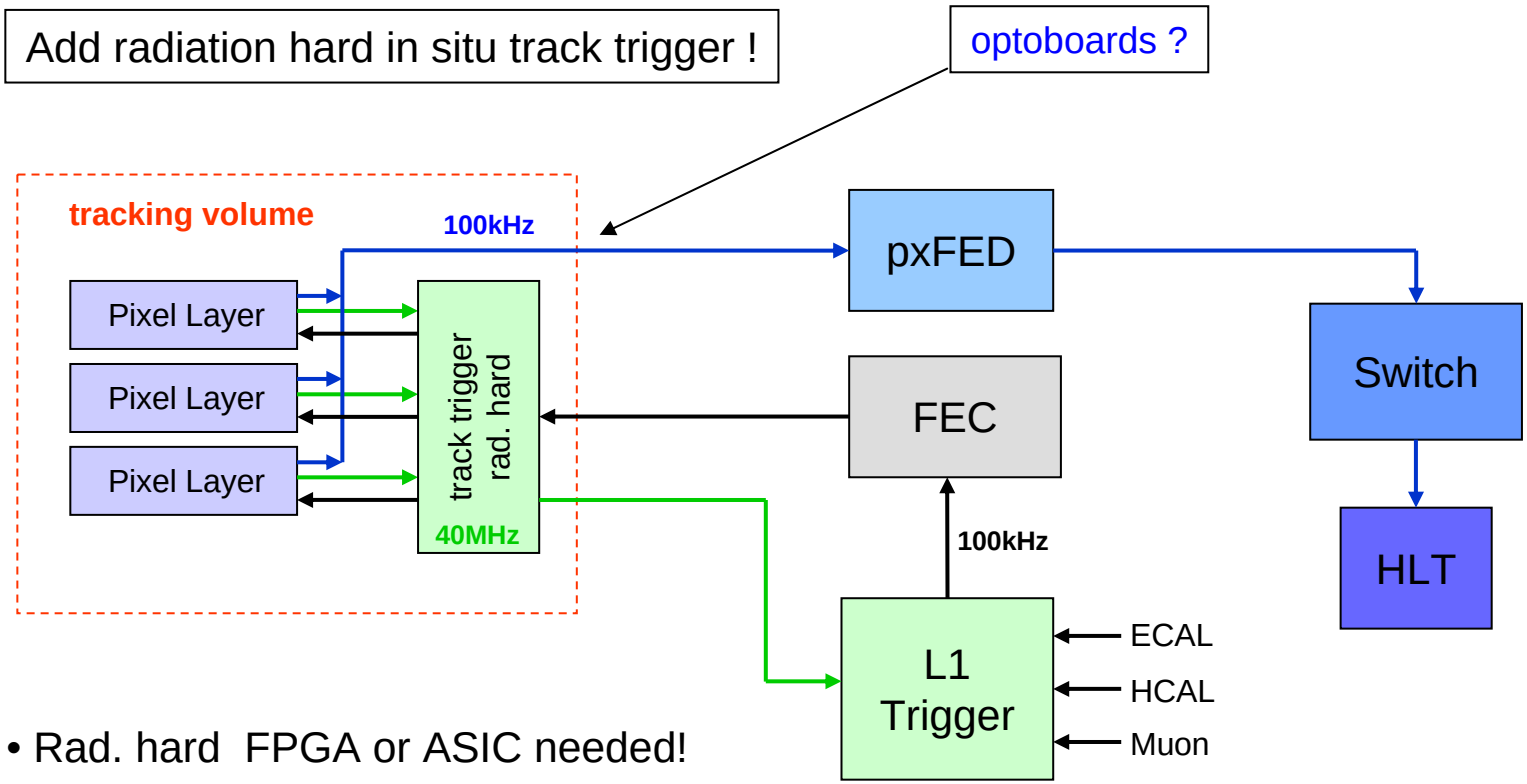
Add extra trigger fiber readout for external track trigger !



- Cabling & Material budget goes up !! (how many trigger fibers needed ?)
- Independent trigger & readout fiber system ? Affordable ?

Tracker Trigger (Option 2)

Add radiation hard in situ track trigger !



- Rad. hard FPGA or ASIC needed!
- Trigger signals in tracking volume electrical ?
- Track trigger boards inside tracking volume or outer surface? → X/X_0 !

Readout signals inside tracker volume electrical & optoconversion at surface ?

Conclusions

- Please think about cabling from the beginning → especially in view of triggering
  → in view of assembly & cost
  → in view of accessibility
- Reduce TTC, Program + Readout cabling to max → ring, star or p2p architecture?
- Costing and affordability of SLHC tracker is crucial ! → choice of technology
- Cooling is the dominant material budget driver ! → reduce power ! !
  → low mass cooling possible ?
- How is replacement of the present CMS Tracker happening ? → old cables?

C3 = Cost , Cooling, Cabling