HSE
Occupational Health & Safety
and Environmental Protection unit

Design and Formal Verification of the Ultra-Low Current Digitizer ASIC ACCURATE 2

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05/05/2022

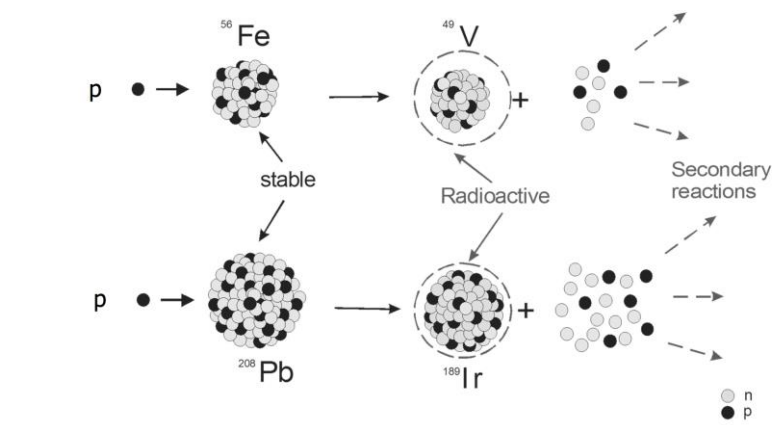
Context :

Why do we need Ultra-low current measurement in RP ?

Context

When Accelerators are in operation

The interaction beam-matter generates stray radiation



Context

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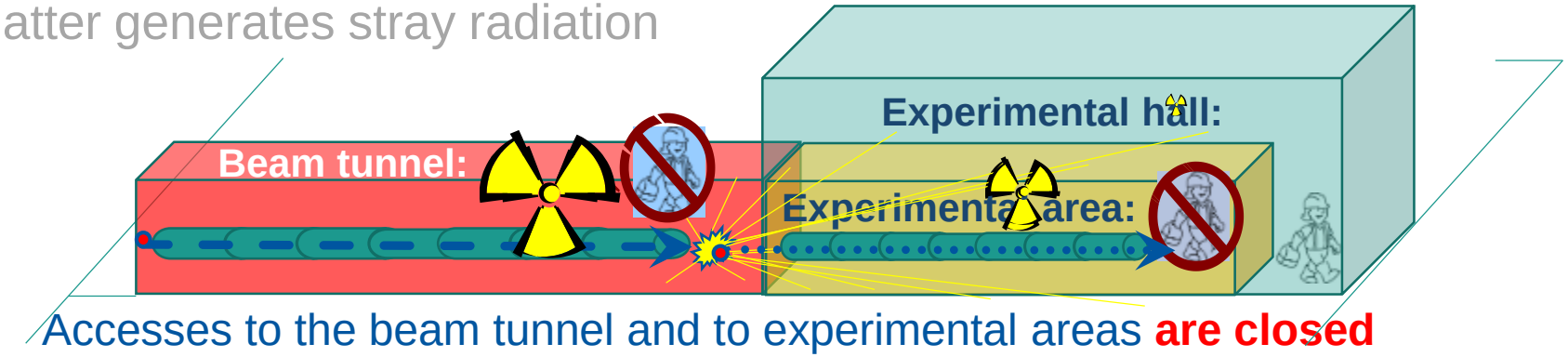


Accesses to the beam tunnel and to experimental areas **are closed**

When Accelerators are stopped

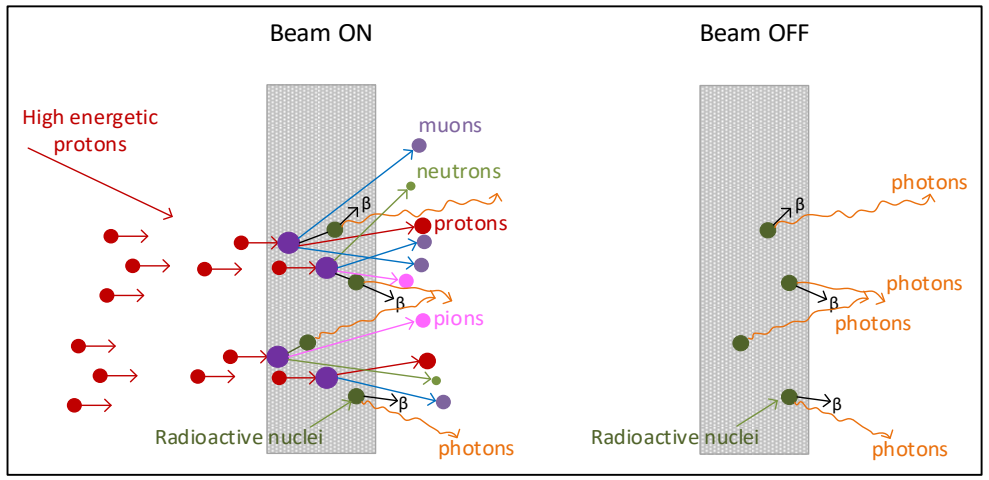
The interaction beam-matter has made the matter radioactive (activation)

Areas with risks due to ionizing radiation are classified and continually monitored

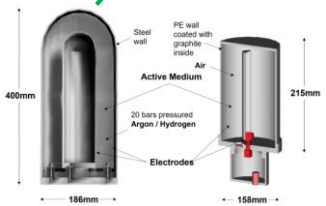
→

When the ambient dose rate is bellow the safety threshold and the survey is Ok : Accesses are re-opened

Context



Monitor type	Detector model	Measurement range	Typical conversion factor [A/Sv/h]	Output current range	Pulse charge at 90% saturation[7] (nominal HV)
AGM	CENTRONIC	50 nSv/h – 0.1 Sv/h	γ: 1.6 10^{-6}	80 fA – 160 nA	100 nC
AMF	CENTRONIC IG5-H20	**50** nSv/h[8] – 0.1 Sv/h	γ: 1.13 10^{-7} n: 4.0 10^{-8}	5.7 fA – 11.3 nA **2** fA – 4 nA	< 30 nC
XRM	IG5T-A15 CENTRONIC IG5T-N15	50 nSv/h – 0.1 Sv/h	γ: 6.83 10^{-7}	34 fA – 68 nA	unknown
	PTW T32006	0.5 µSv/h – **10** Sv/h	γ: 2.5 10^{-8}	12.5 fA – **250** nA	5 nC
TGM[9]	CENTRONIC IG5-A20	1 µSv/h – 0.1 Sv/h	γ: 1.6 10^{-6}	1.6 pA – 160 nA	100 nC
	CENTRONIC IG32-A3.1	1 µSv /h – 1 Sv/h	γ: 1.13 10^{-7}	113 fA – 113 nA	**500** nC
TMF[9]	CENTRONIC	1 µSv/h – 1 Sv/h	γ: 1.13 10^{-7}	113 fA – 113 nA	< 30 nC
IAM[9]	PTW T32006	1 µSv/h – **10** Sv/h	γ: 2.5 10^{-8}	25 fA – **250** nA	5 nC



When Accelerators are stopped

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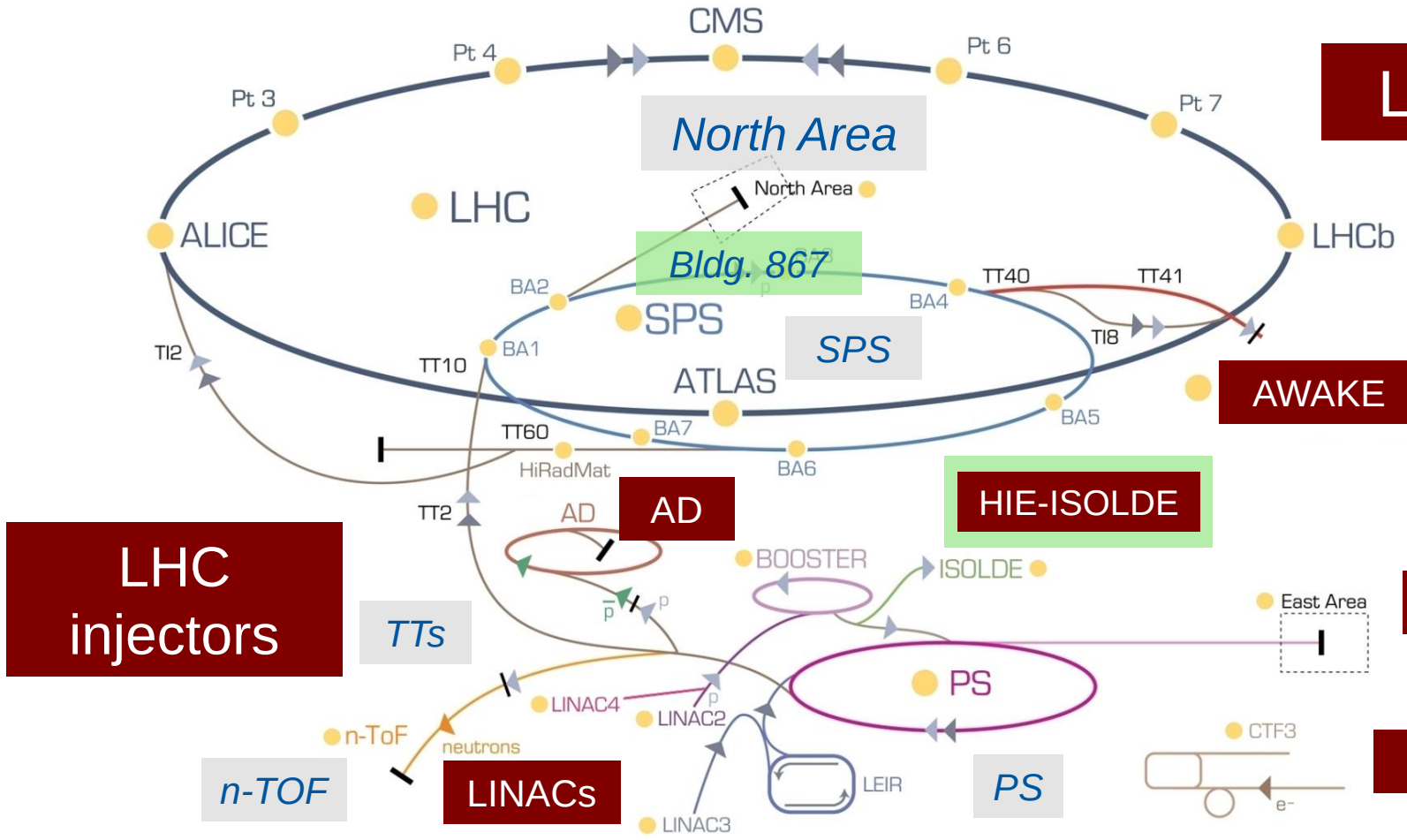
When the ambient dose rate is bellow the safety threshold and the survey is Ok : Accesses are re-opened

CERN - **R**adiation & **E**nvironmental **M**onitoring **S**ystem

864 Radiation Protection channels & **523** Environmental channels

GRAMS	2012
ARCON → CROME	**LS2** 2021
RAMSES → CROME	**LS3** 2028
CROME + Accurate	**LS4** 2030



LHC

LHC injectors

East Area

CTF3

n-TOF

LINACs

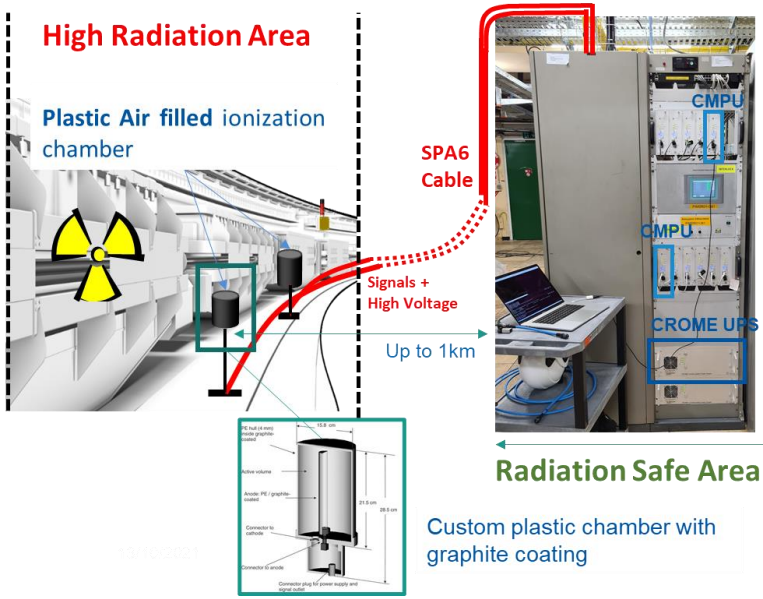
PS

CERN - **R**adiation & **E**nvironmental **M**onitoring **S**ystem

CROME Radiation Protection Channels Configuration

CROME Rack Version – High radiation Areas

CROME Rack-mount Version at CERN at the PS Booster



PS

SM18

SPS and more …

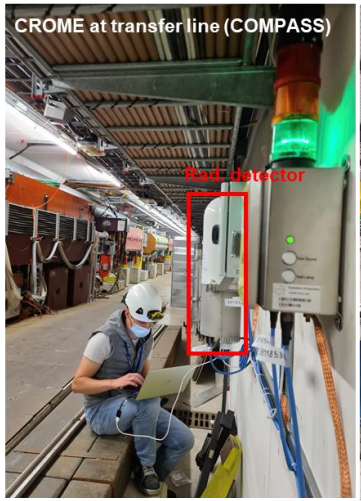
Radiation Safe Area

100 CMPUs Rack are in operation

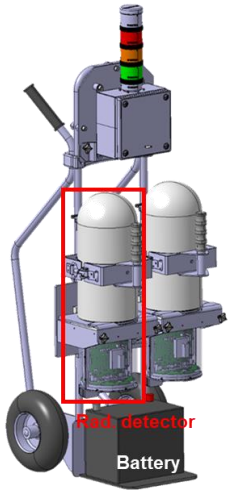
CMPU : Core Monitoring and Processing Unit

CROME Bulk Version – Low radiation Areas

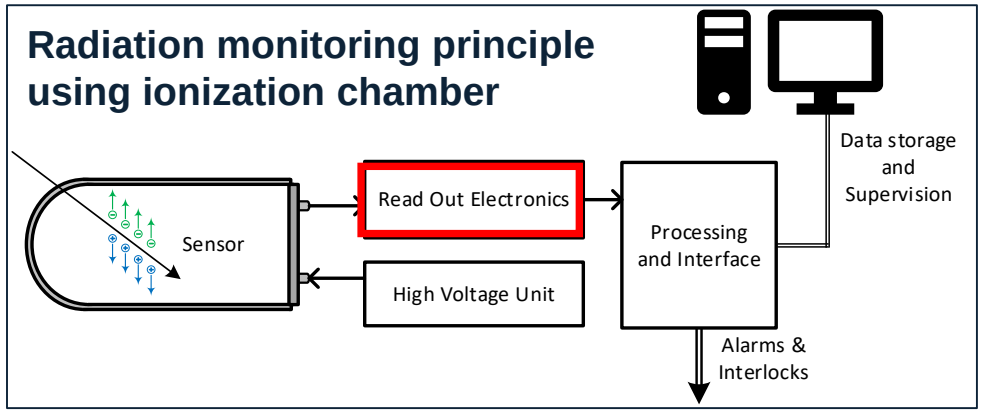
CROME Bulk - Wall-Mounted Version

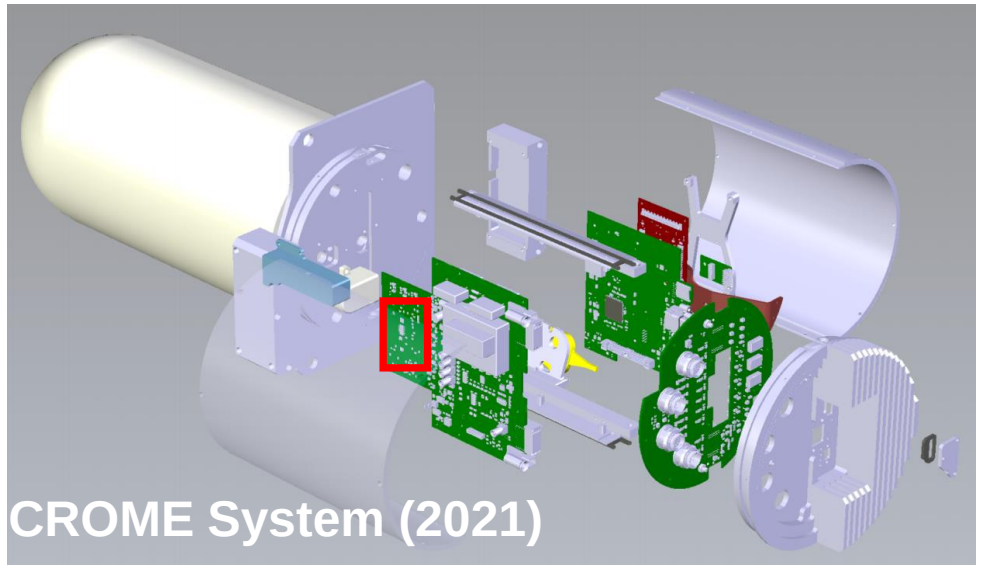


CROME Bulk - Mobile Version

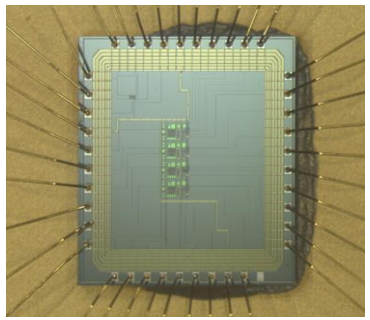


Motivation for new ASIC development

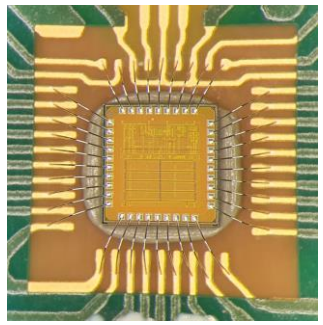




- Based on more than 3000 discrete components
- Difficulties in sourcing and mitigating obsolescence
- Complex assembly process
- Upgrade takes significant effort
- Dependent on critical components which are difficult to replace



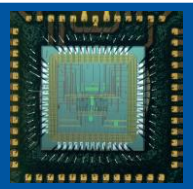
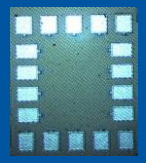
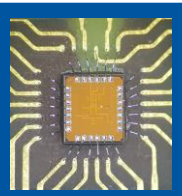
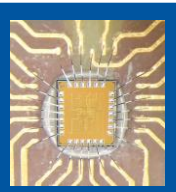
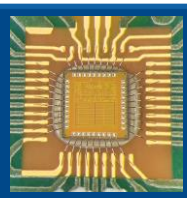
UTOPIA 1 (2014)



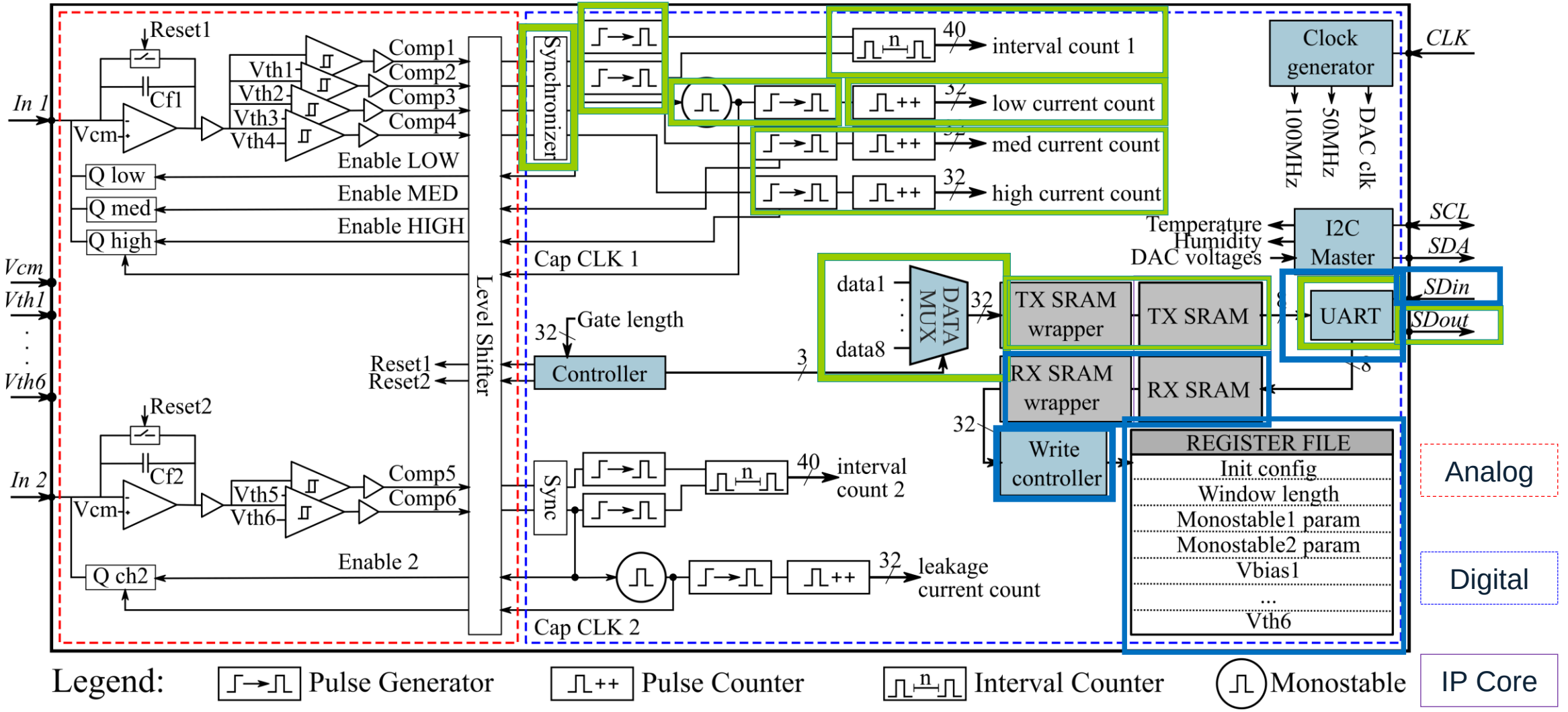
ACCURATE 2 (2021)

S. Kundumattathil Mohanan, H. Boukabache, V. Cruchet, D. Perrin, S. Roesler and U. R. Pfeiffer, "An Ultra Low Current Measurement Mixed-Signal ASIC for Radiation Monitoring Using Ionisation Chambers," in *IEEE Sensors Journal*, vol. 22, no. 3, pp. 2142-2150, 1 Feb.1, 2022, doi: 10.1109/JSEN.2021.3132498.

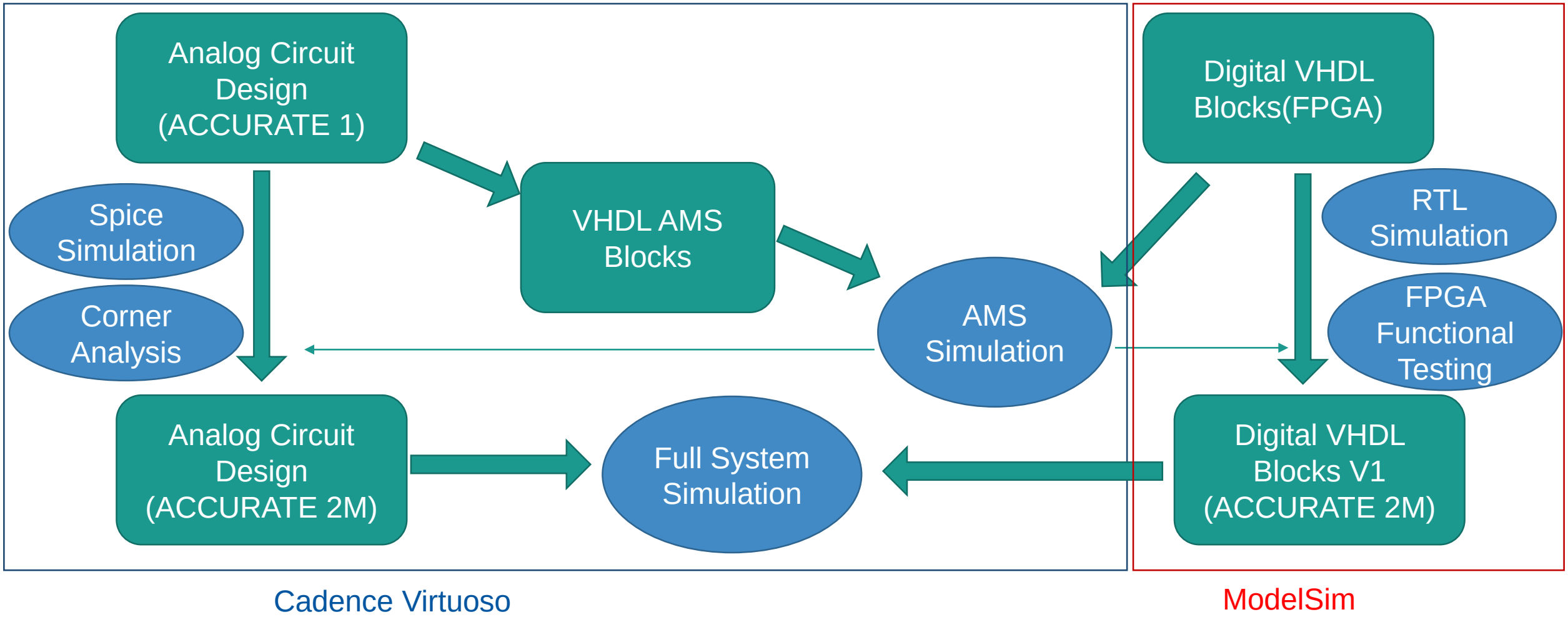
ASICs of RP

	 UTOPIA 2	 ACCURATE 0	 ACCURATE 1	 ACCURATE 2A	 ACCURATE 2M
Year	2016	2018	2019	2021	2021
Technology	350 nm	22 nm	130 nm	130 nm	130 nm
Min Current Resolution	1 fA	1 fA	1 fA	0.2 fA	0.2 fA
Max Current	5 µA	1 nA	1 µA	20 µA	20 µA
Area	7.56 mm^2	0.33 mm^2	1.95 mm^2	1.95 mm^2	3.52 mm^2
Power Supply	3.3 V	1.2 V	3.3 V	3.3 V	3.3 V, 1.2 V
Power Consumption	8.25 mW	0.93 mW	2.5 mW	3 mW	17.4 mW
Leakage Current	-50 fA	-240 fA	-7 fA	+6 fA	+6.5 fA
Number of Channels	2	3	1	1	2
Primary Objective	Current digitiser	Technology evaluation	Architectural comparisons, tech. evaluation	Current digitiser	Mixed signal current digitiser
Percentage of charge collected for 100 nC pulse	45%			61% 95%(with 50 MΩ)	

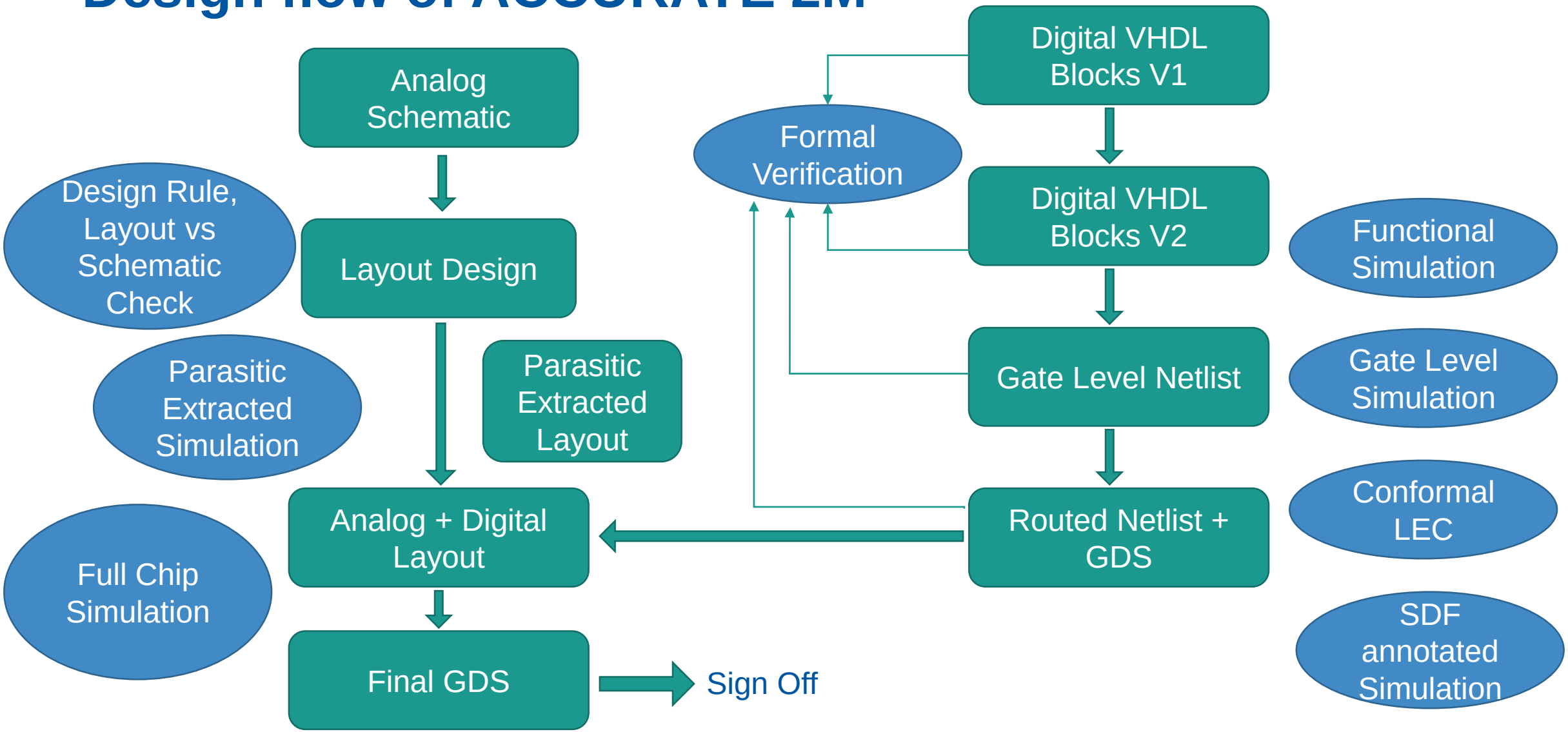
ACCURATE 2M system architecture



Design flow of ACCURATE 2M



Design flow of ACCURATE 2M



Formal Property Verification of Accurate 2

More details in:

Ceesay-Seitz, K., Kundumattathil Mohanan, S. Boukabache, H., Perrin, D.:
Formal Property Verification of the Digital Section of an Ultra-Low Current Digitizer ASIC.
Proceedings of Design and Verification Conference and Exhibition Europe, DVCon Europe,
Munich (2021)

http://cds.cern.ch/record/2789695/files/CeesaySeitz_DvCon2021_FormalPropertyVerification.pdf

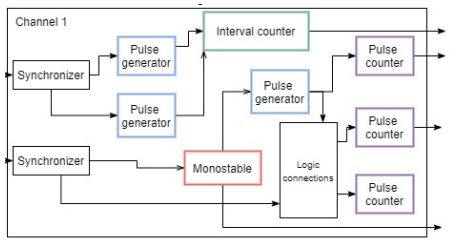
Formal Property Verification – Model Checking

Commercial tools:

- Cadence Jasper Gold
- **Siemens Questa Formal**
- Synopsis VC Formal
- …

Open-source tools:

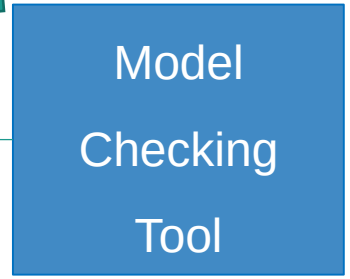
- SymbiYosys,
- EBMC, …



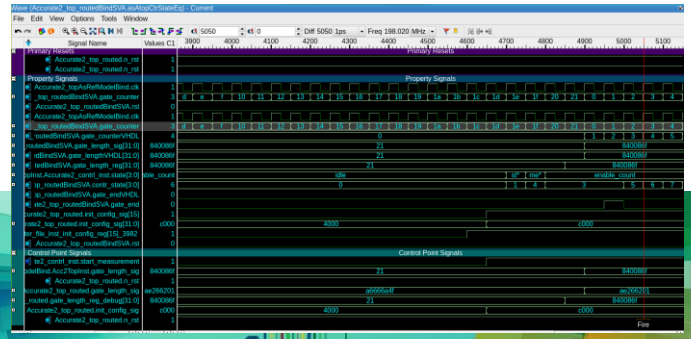

```
property pIntAlarmOn();
  (((mtValidxDI == 1) && $rose(intStartxDI))
   ##`nrCUntilCalcRdy
   ((alarmActivexDI == 1) &&
      (signed'(integralxDO) >= signed'(thresholdxDI))))
    |-> sIntAlarmOn();
endproperty

sequence sIntAlarmOn();
  ##`nrCyclesAlarmRdy (ALARMxDO == 1);
endsequence

assert property (pIntAlarmOn);
```



…routedBindSVA.asAtopCtrGateCntRestAfterGateLenVHDL	10	1s
…te2_top_routedBindSVA.asAtopGateLenSigRouted100ms	7	1s
Accurate2_top_routedBindSVA.asAtopCtrGateCntEq	10	2h 30m 9s
Accurate2_top_routedBindSVA.asAtopCtrGateEndEq	10	2h 31m 37s
Accurate2_top_routedBindSVA.aAtopCtrWeHighLength	10	1s
Accurate2_top_routedBindSVA.aAtopCtrWeHighTime	7	1s
…ChkCtrlNoUnexpectedRst.aNoUnexpectedCntRstSymbolic	7	12s



Formal Property Verification with SystemVerilog Assertions

Goal: Model checkers mathematically prove properties of design

+ Exhaustive proofs for all verification scenarios (within chosen constraints/assumptions)
+ Quick generation of counter examples (usually corner cases)
+ No test cases/bench, can get started quickly

- State space explosion (depending on size of data inputs and sequential depth)

SystemVerilog Properties and Sequences

Linear Temporal Logic (LTL) / Sequential regular expressions

Boolean logic operators: && (and), || (or), ! (not), …

LTL operators: always, eventually, nexttime, until, iff

Sequence operators: and, intersect, or, within

a **until** b

= (a)[*0:$] ##1 b

if a or b is not specified, it can have any value

Simple properties – enable / valid / resets

Prove that whenever enable is low, one clock cycle later all outputs are 0.

```
assert property (
      enable == 0
      |=>
      (output1 == 0 && output2 == 0)
);
```

A	B	Implication A |=> B
0	0	1
0	1	1
1	0	0
1	1	1

Simple properties – action caused by an event

Prove that for all 2^{32} possibilities of the target value and any combination with other input signals, any time when the counter equals the target value, the design generates a pulse.

```
assert property (
    counter == target_value
    |=>
    $rose(pulse)
);
```

Built-in in SystemVerilog:
$rose(), $fell(), $stable(), …

alternative to implication: iff (if pulse can only rise when counter == target_value)

Simple properties – action caused by an event

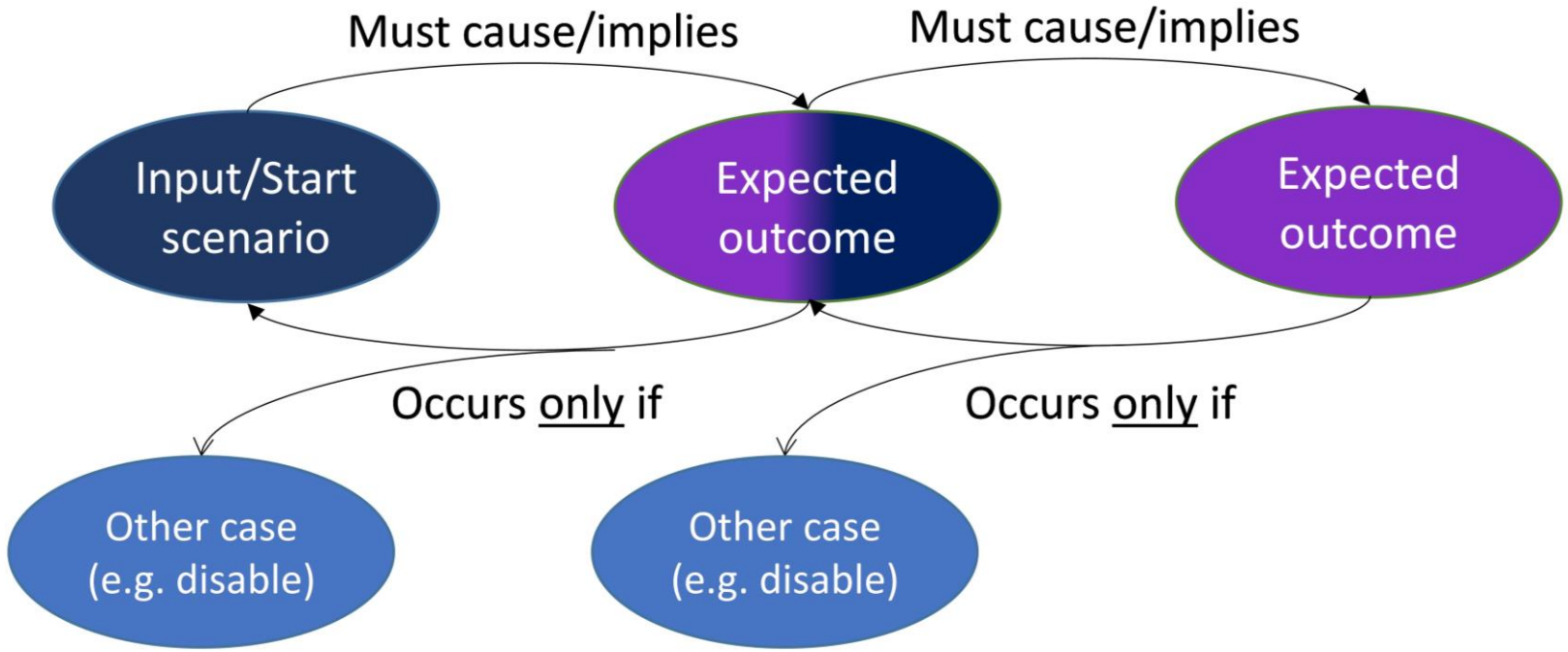
Prove that for **all** 2^{32} possibilities of the target value and **any combination** with other input signals, any time when the counter equals the target value, the design generates a pulse.

```
assert property (
      counter == target_value
      |=>
     $rose(pulse)
);
```

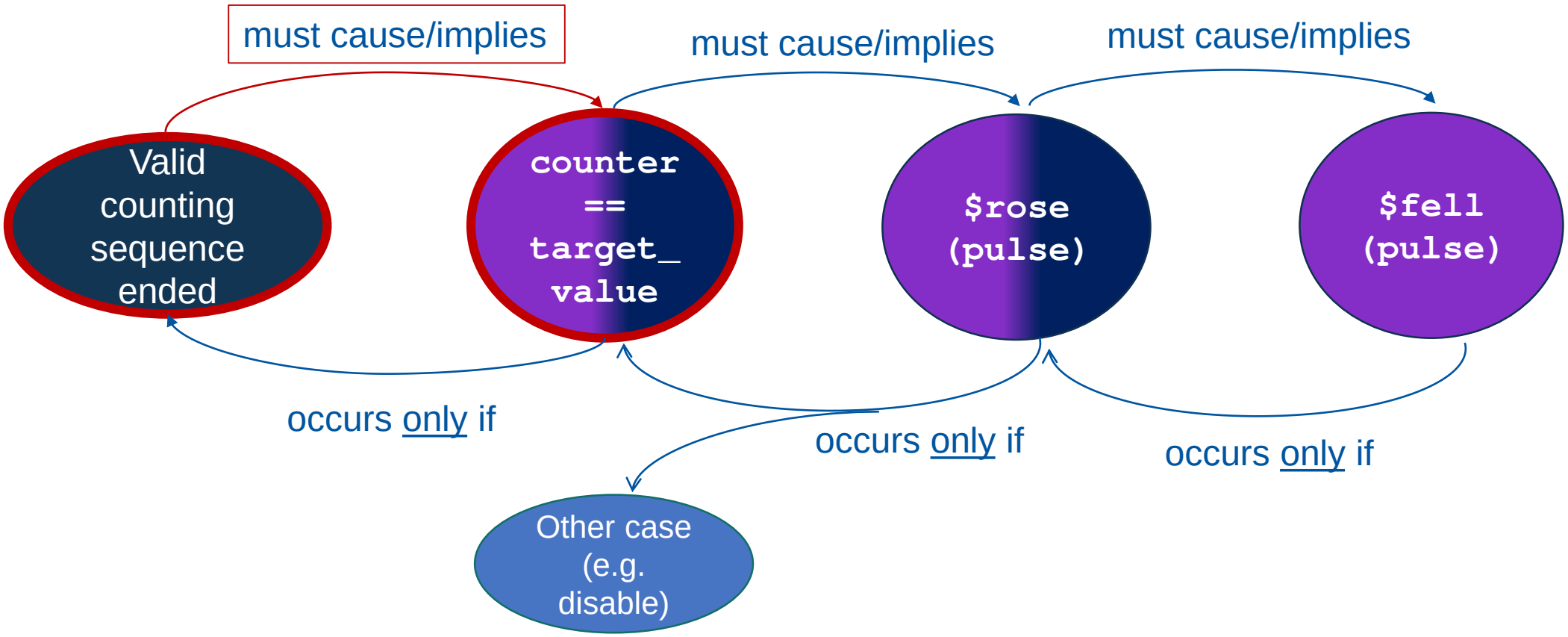
Proven for ALL value combinations of ALL signals that are not explicitly mentioned.

Chain of events

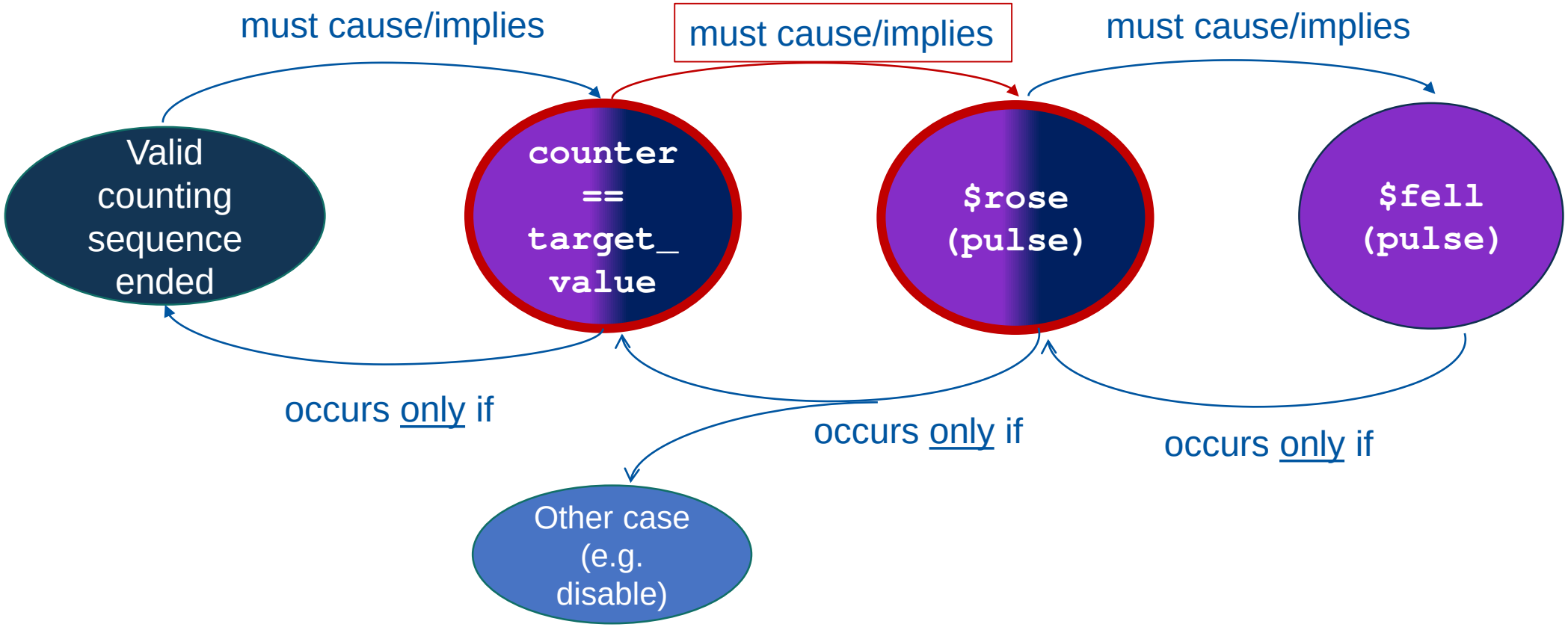
Partition the problem space into a set of consecutive events.



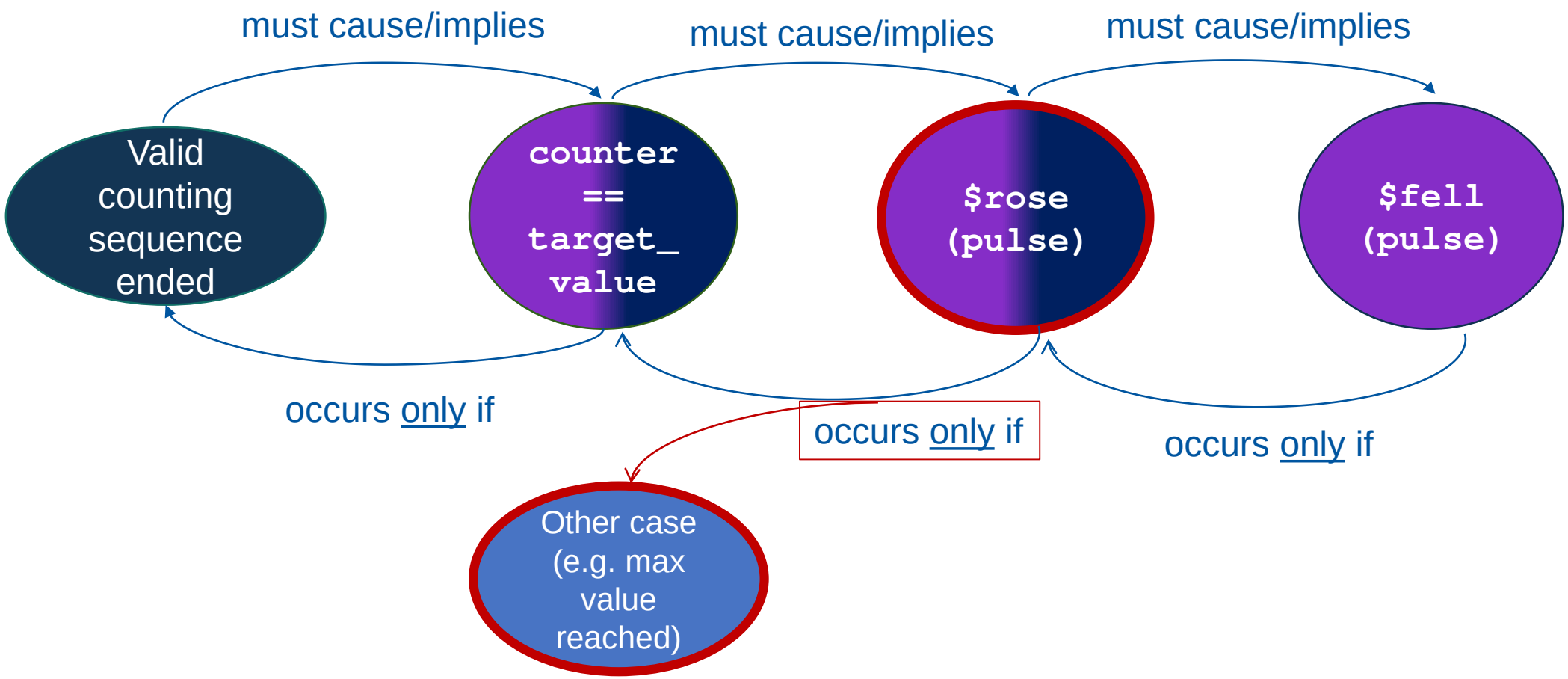
Chain of events



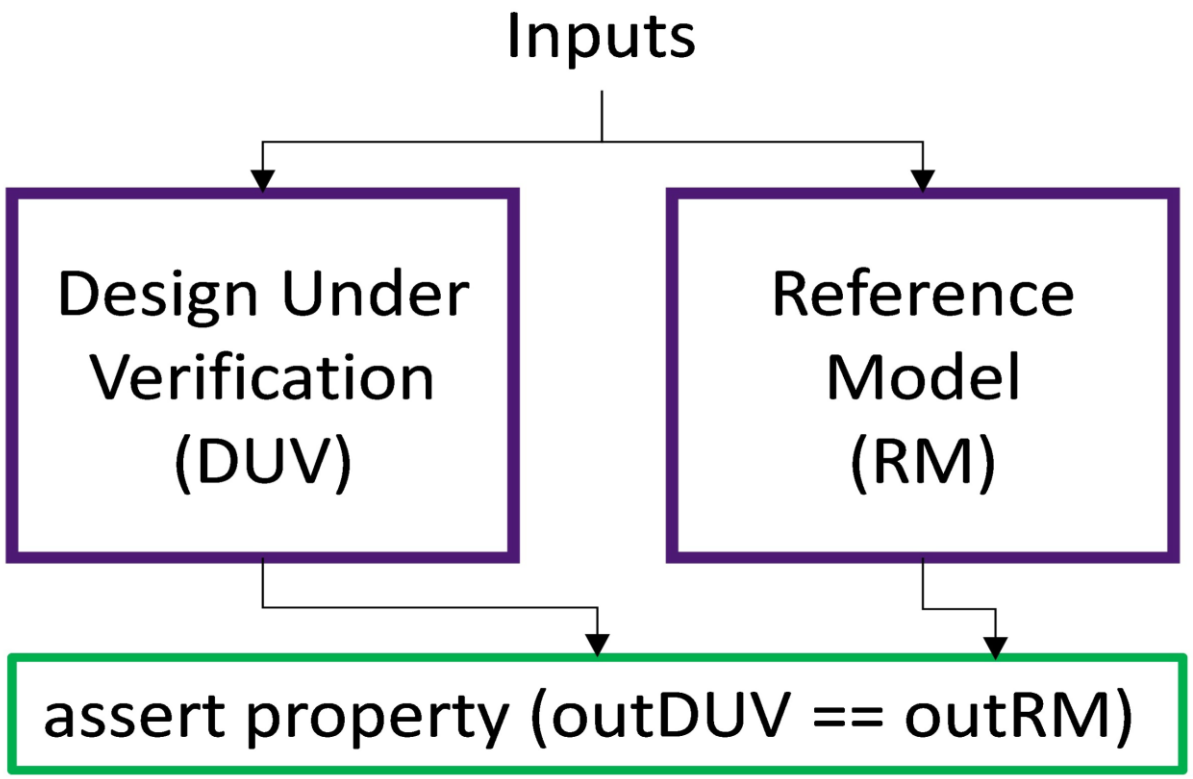
Chain of events



Chain of events



Proving with reference models



- Easy to write and maintain
- Does not always scale
  only for counters < 16 bits

- Cover properties
  - necessary for all interesting scenarios
  - associated to requirements for progress tracking

Counting with local variables

```
property pCounting();
  reg[`Bit_Width - 1:0] lCnt; // local counter
  (((cond1, lCnt = 1) or (cond2 or cond3, lCnt =
0))[*0:$]
    ##1
    ((cond4, lCnt++) or (cond5, lCnt = lCnt))[*0:$]
    ##1
    ((cond6, lCnt = lCnt) or (cond7, lCnt = 1)))
  |=> (lCnt == duvCnt);
endproperty
```

Counting with local variables

```
property pCounting();
  reg[`Bit_Width - 1:0] lCnt;
  (((cond1, lCnt = 1) or (cond2 or cond3, lCnt =
0))[*0:$] // initialize local counter
    ##1
    ((cond4, lCnt++) or (cond5, lCnt = lCnt))[*0:$]
    ##1
    ((cond6, lCnt = lCnt) or (cond7, lCnt = 1)))
  |=> (lCnt == duvCnt);
endproperty
```

Counting with local variables

```
property pCounting();
  reg[`Bit_Width - 1:0] lCnt;
  (((cond1, lCnt = 1) or (cond2 or cond3, lCnt =
0))[*0:$]
    ##1
    ((cond4, lCnt++) or (cond5, lCnt = lCnt))[*0:$]
 // count or keep value
    ##1
    ((cond6, lCnt = lCnt) or (cond7, lCnt = 1)))
  |=> (lCnt == duvCnt);
endproperty
```

Counting with local variables

```
property pCounting();
   reg[`Bit_Width - 1:0] lCnt;
   (((cond1, lCnt = 1) or (cond2 or cond3, lCnt =
0))[*0:$]
     ##1
     ((cond4, lCnt++) or (cond5, lCnt = lCnt))[*0:$]
     ##1
     ((cond6, lCnt = lCnt) or (cond7, lCnt = 1)))
// keep value or reset counter to 1
   |=> (lCnt == duvCnt);
endproperty
```

Counting with local variables

```
property pCounting();
  reg[`Bit_Width - 1:0] lCnt;
  (((cond1, lCnt = 1) or (cond2 or cond3, lCnt =
0))[*0:$]
    ##1
    ((cond4, lCnt++) or (cond5, lCnt = lCnt))[*0:$]
    ##1
    ((cond6, lCnt = lCnt) or (cond7, lCnt = 1)))
  |=> (lCnt == duvCnt); // local counter must equal
design under verification's counter output
endproperty
```

Reducing state space with assumptions (= constraints)

```
property pPcPulseInIsPulse();
    pulse_in == 1 |=> pulse_in == 0;
endproperty
assume property (pPcPulseInIsPulse);

property pCh1InComp1Rst();
    rst == 1 |-> comp1_out == 1;
endproperty
assume property (pCh1InComp1Rst);
```

Reducing state space

Abstractions - proof is also valid for original design

- Setting initial values of a signal to X (= all possible values)
- Removing / replacing logic that drives a signal

Reductions - proof is only valid for the chosen subset of the design state space

- Setting inputs to constant values
- Reducing bitwidth of a design via VHDL generics/SV parameters

X values in the design – Synthesis- vs. simulation-semantics

```
          X
if signal_in = '1' then
  other_signal <= '1'; ← formal/silicon
else
  other_signal <= '0'; ← simulation
end if;
```

Simulation: X means unknown, i.e. not ‘1’
Formal with synthesis-semantics / silicon: X can become 0 or 1 → first branch might be taken!

ACCURATE 2 Verification - Results

- **Exhaustively proved functionality of most blocks** end-to-end
  - Proved current measurement counters, although designs containing counters are often seen as “unsuitable” for formal verification
  - End-to-end proofs based on top-level inputs and outputs of full design were not feasible
- **Found and removed 30 bugs**:
  - 20 caused by ambiguous specification
  - 11 found by review of specification and natural language version of formal properties*

Block	Specification	Design	Verification requirement	Verification code	Total mismatch
Interval Counter	6	8	8	5	16
Pulse Counter	-	1	-	-	1
Pulse Generator	1	-	2	2	2
Synchronizer	1	-	-	1	1
Monostable	1	2	1	1	3
Channel2 Interface	1	1	2	2	2
TxSRAM Wrapper	1	1	3	3	3
Top Module	-	2	-	-	2
Total	**11**	**15**	**16**	**14**	**30**

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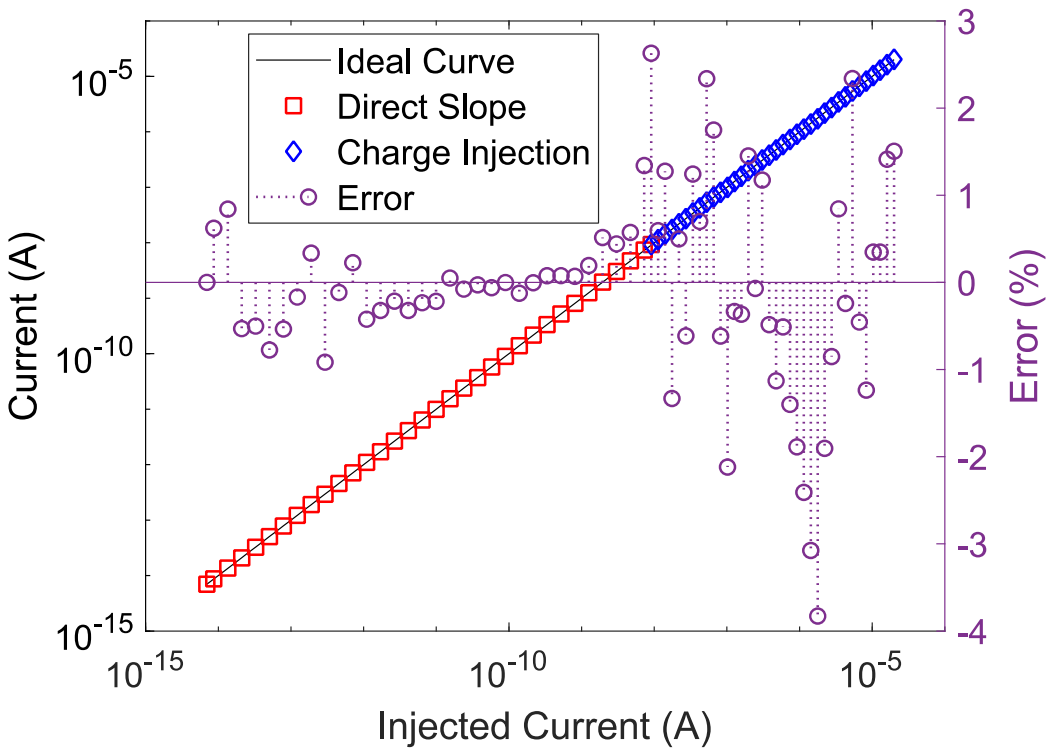
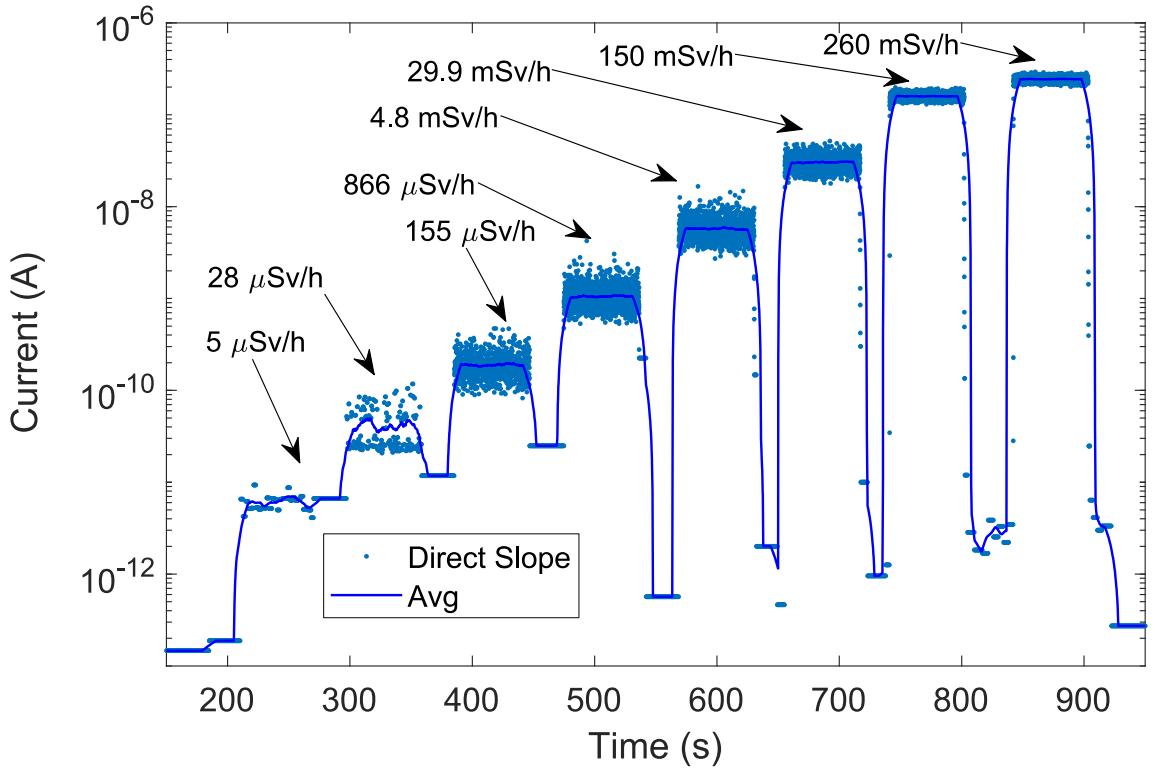
Formal Property Verification of the Digital Section of an Ultra-Low Current Digitizer ASIC.
Proceedings of Design and Verification Conference and Exhibition Europe, DVCon Europe, Munich (2021)

*Ceesay-Seitz, K., Boukabache, H., Perrin, D.: Semi-formal reformulation of requirements for formal property verification. In: Proceedings of Design and Verification Conference and Exhibition Europe, DVCon Europe, Munich (2019)

ACCURATE 2 Characterization - Results



Current measured by ACCURATE 2M for injected current from -7 fA to -20 uA



Current measured by ACCURATE 2M with IG5 chamber for different dose rates

Conclusion and Outlook

Design:

- ACCURATE 2 meets the design requirements with state-of-the-art performance and was demonstrated in different application scenarios
- Verification was crucial in providing the confidence in an expensive ASIC tapeout

Formal Verification:

- Reviews and systematic identification of properties based on requirements increase quality
- Formal tool finds corner case bugs first and within seconds
- Formal properties verify larger design state space than simulation could in the same runtime
- Simulation needed additionally for top level verification

Conclusion and Outlook

Lessons learned and methodologies developed will pave the path for design and verification of next version of the ASIC.

Feel free to join the

Formal methods & verification interest group

e-group:

formal-methods-interest-group@cern.ch

Publications

1. S. K. Mohanan, H. Boukabache, D. Perrin, and U. Pfeiffer, "*Towards the next generation of CERN radiation monitoring front end ASICs*", in Topical Workshop on Electronics for Particle Physics (TWEPP), 2021

2. S. K. Mohanan, H. Boukabache, V.Cruchet, D. Perrin, S.roesler, and U. Pfeiffer, "*An Ultra Low Current Measurement Mixed-Signal ASIC for Radiation Monitoring Using Ionisation Chambers*", IEEE Sensors Journal,vol. 22,pp. 2142–2150, 2021

3. K.Ceesay-Seitz, S. K. Mohanan, H. Boukabache, and D. Perrin, "*Formal Property Verification of the Digital Section of an Ultra-Low Current Digitizer ASIC*", in The Design and Verification Conference and Exhibition Europe (DVCon Europe), 2021

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