Tracking at FCC experiments

- FCC-ee conceptual design proposals
- Technology R&D for precision, further challenges at FCC-hh
- French contribution's prospect

FCC meeting at IRFU, April 20/2022 D. Contardo, IP2I

FCC-ee conceptual designs today



Vertex Detector: MAPS

Wrap-up/Timing Layer: MAPS/Hybrids/AC-LGADs/SPADs/MicroMegas/µ-Rwell...

CLD and **IDEA** Vertex Detectors designs (superimposed)

MAPS with $\sigma_{hit} \simeq 3 \ \mu m$ and $\ X/X_0 \simeq 0.3\%$ / layer of Si

- CLD concept: double layers in Barrel/Endcap configuration
- IDEA concept: single closer layers in Long Barrel configuration



CLD and **IDEA** Vertex Detector, d₀ and z₀ precision

- Initial performance target is achieved with relatively close precision despite design differences
 - At first glance IDEA wins for precision at low p_T (at small η) with less layers of Silicon
 - > Are these configurations two different asymptotes of σ_{hit} versus X/X₀, is there room for better hit precision?
 - > Do differences (over η/p_T range) matter for physics, motivate different configurations / sensor optimizations ?



F. Bedeschi https://indico.cern.ch/event/838435/contributions/3658345/attachments/1968063/3273039/Bedeschi_IDEA.pdf

More aggressive Vertex Detector designs ?



* ALICE ITS3 targets: 12" wafers - 20 μ m thick – 0.05% X/X₀ with gas flow cooling & cylindrical design

Vertex Detector readout architecture



- Up to x40 hits/BC at 365 vs 91 GeV
- But \simeq /4 <rates> due to much larger BC spacing
- Ballpark requirements
 - O(1-10) μs integration window*
 - O(50) MHz/cm² hit throughput



Figure of merit is the power consumption in the pixel matrix and at periphery vs impact on X/X_0

- GEANT + digitization + reconstruction simulation to provide
 - Hit rates to simulate power consumption of architecture options
 - Tracking efficiency & fake rates to set time integration window
 - RO w/o trigger appears possible wrt rates, impact on power and X/X₀ to be checked?
- Possibly different specifications/features according to radius/beam conditions ?

* Windows down to BC clock, O(20) ns at Z-peak, can be achieved with fast shaping, but benefit is not demonstrated:

- ex. further BIB rejection in VD to approach beam line and/or improve multiple vertices ID ?
- ex. 0.1 Z Pile-Up at Z-peak in 1 μs window, should be identified by total energy and reconstructed through vertex precision ?

CLD and **IDEA** Central Tracker designs (superimposed)



- Initial performance target achieved $(\sigma(p_T)/p_T^2 \leq 2 \times 10^{-5} \text{ GeV}^{-1})$
 - At first glance IDEA winning over full p_T range (low X/X₀ in DCH more critical than better hit precision in Si)
 - \blacktriangleright Full Si Central Tracker needs optimization, number of layers, σ_{hit} vs X/X₀*
- * Also possibly optimization of wrapping layers around DCH

R&D Vertex Detector: MAPS for position precision at low X/X_0

- CERN EP WP1.2 R&D in TJ 65nm stitched process on 12" wafers targeting ALICE ITS3
 - 1st Multi-Layer-Reticle end 2020, different designs and splits (process parameters)
 - Evaluation so far so good, depleted design preferred for less charge sharing higher/faster signal, not mandatory for NIEL O(10¹²) neq/cm² (TID O(1) MRad)
 - 2nd submission Engineering Run 1 May 2022, stitched process for yield
 - 3^{rd} submission Engineering Run 2 Oct. 2023, full ALICE sensor $\simeq 10 \times 28 \text{ cm}^2$?
- Toward FCC-ee: smaller pitch ? higher rates O(50) MHz
 - Architecture optimization to minimize power consumption

ER1: MOSS (ALPIDE/MIMOSIS*) architecture and MOST (MALTA**) w/o clock in matrix for lower power & high rates





MAPS option for position and precision at low X/X₀

- Transverse precision achieved for VD, can be released depending on X/X₀ achievements
- Pixels can be grouped in longitudinal direction to minimize power consumption
- Low X/X₀ is the challenge
- Proposal for 1st MAPS Central Tracking in ALICE-3 and LHCb-2 UT/MT in LS4 (2034-2035)*
- Low cost hybrid CMOS is a plausible alternative
 - Less favorable for low pitch and low X/X₀?
- Mechanics and services, X/X₀, mostly a system aspect*
 - > Design and prototyping of light systems with sensors built in 12" wafers
 - Study interfaces to beam pipes, and other systems

* See additional information slide 23

** See ex. of ALCIE additional information slide 24

- Drift Chambers*
 - Build large size detector with ultra-light wires
- TPC*
 - Control ion backflow distortion, ex. with pixel double MM meshes designs, low gain. High P
 - R&D studies driven by CEPC: H. Qi <u>https://indico.fnal.gov/event/46746/contributions/210382/</u>
 - IRFU contributions on MM readout, LCTPC (ILD/ILC), CLAS12 (JLAB) TPC
 - Simulation study of mixed CT configuration with Si and TPC at increased radii (inner/outer)?
- DCH and TPC: demonstrate PID performance with dE/dx and dN/dx
 - Potential to improve rΦ hit precision in DC exploiting cluster counting not yet investigated ?

• Scale from sub-BC clock O(<20) ns down to intra-BC precision O(<10) ps*

- Requires ToA and ToT implementation in the readout
- 4D-tracking means timing measurement in several (all) layers

• Motivation

- PID with ToF, ex. 1 hit with 10 ps precision at 2 m provides $3\sigma \pi/K$ separation up to 5 GeV**
- Enabling mass measurement of LLPs decaying in charged particles
- Ultra-pure track reconstruction (would need measurement in VD) ?
- Energy spread correction in head-head, middle-middle, tail-tail collisions, O(6) ps vertex precision

Simulations

- Demonstrate benefit for physics
- Define where the measurements should be implemented and with which precision per hit
- Define readout architecture & estimate power impact compatibility with low X/X₀ constraint

* Collision time spread in BC at Z-peak is O(40) ps

** See additional information slide 26, multiple scattering limit to be evaluated

Timing precision, technology considerations

 $\sigma_{t} = \sigma_{sign} \bigoplus \sigma_{elec} = \sigma_{sign} \bigoplus \sigma_{jitter} \bigoplus \sigma_{time-walk} \bigoplus \sigma_{TDC} \bigoplus \sigma_{clock}$

• Sensors w/o amplification

- Planar large electrodes, precision limited by S/N
- Planar small electrodes, precision limited by spread hit-electrode distance
- 3D limited by S/N (but no effect of Landau fluctuation on charge collection time)

• Sensors w/ low amplification

- LGADs limited by Landau fluctuation, but high S/N
- Sensors w/ avalanche amplification
 - SPADs minimal Landau fluctuation and high S/N (ultimate precision?)

Simulation to assess limits

- Differently depending on parameters, active thickness, pitch, electrode size, that compete in performance for different technologies
- No obvious path to reach $O(\leq 10)$ ps, (while maintaining sufficient rad. tol.)?



- Hybrid designs could be an alternative to MAPS for Central Tracker
 - Planar sensor
 - CMS diode tests show \leq 70 ps for S/N \geq 10 (asymptote \simeq 10 ps)
 - NA62 VD achieved \simeq 115 ps
 - Improvement with thicker sensors and/or lower noise electronics ?
 - Hybrid 3D sensors
 - TimeSpot TSMC 28 nm achieved \simeq 20 ps at 150 μm thickness and 50 μm pitch
 - Improvement with finer pitch and lower noise electronics ?
 - LGADS
 - ATLAS/CMS achieved \simeq 30 ps at 50 μ m thickness 1.3 mm² pads
 - > AC-LGADs, TI-LGAD to enable pixel pitch with thinner sensors ?

- MAPS large electrodes
 - ex. Cactus IRFU* LFoundry 150 nm, 1mm^2 pads, target $\simeq 60 \text{ ps}$ @ 100 μm thickness
 - Improvement with thicker sensors and/or lower noise electronics ?
- MAPS small electrodes
 - ex. FASTPIX TJ 180 nm, 20(10) μ m pitch, hexa. geo., adv. dop. prof., epi. \leq 30 μ m, achieved $\sigma_{t} \simeq$ 120(140) ps
 - > Optimize design in deeper node ex. TJ 65 nm
 - Consider imaging technologies with even lower nodes and 3D integration*
 - Ultra small pitch and ultra thin epi layer for ultimate hit, timing precision and low X/X₀
 - Issue can be radiation tolerance (although constraint is relatively low at FC-ee)
 - Commercial application (ex. for automotive...) now at high speed and high rates
- MAPS also candidates for 4D-shower tracking
 - HGCal with pads, UltraHGcal with pixels (possibly particle counting with charge from ToT)
 - Compactness to improve sampling fraction, no X/X₀ constraint, but power issue

FCC-hh tracking requirements

- New territory of operation conditions
 - $30 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ Collisions 30 GHz,1000 per BC 30 ab⁻¹ integrated, coverage up to $\eta = 6$
- Tracking requirements
 - <0.4> ps & <130> μ m between vertices
 - Track rates 30 GHz/cm² (r = 2.5 cm)
 - 4D-tracking for pile-up mitigation and reco. power
 - Granularity close to FC-ee
 - O(5) ps precision to recover HL-LHC like PU
 - Fluence 10¹⁸ neq/cm² and TID 30 GRad at 2.5 cm
- New paradigm needed for radiation tolerance
 - No present technologies can survive below R < 30 cm
 - ex. current MAPS and LGADS are marginally at level of radiation tolerance for outermost layers
- New paradigm needed for rates and data transfer
 - Deep technology node, 3D integration, photonics and/or wireless data transmission*



R&D for FCC-hh tracking

- Si-sensor NIEL tolerance
 - Unknown beyond 10¹⁷/cm² neq, models maybe too pessimistic, qualification itself is an issue
 - 3D & thin planar may approach needs
 - Other WBG semiconductors Diamond*, GaInP, GaAs, GaN, SiC** to be evaluated
- ASIC TID tolerance
 - > Not clear if finer technology nodes alone would provide substantial improvements
- New materials and 3D process could be a solution
 - Graphene, Carbon-based metamaterials, nanotubes...
 - ex. CVD-diamond semiconductor pixel sensors
 - New 3D design, laser graphitization for thin low ρ electrodes
 - In depth field optimization readout structures
 - Need scaling for production of large areas





ex. ASICs

- Higher dielectric thick oxide (multiple) gates
- Carbon based beyond CMOS, nanotube, graphene



ex. FinFET technology

* IN2P3 MP DIAMTEC - DIAMASIC in a different context of beam monitoring, ** CEA-IM2NP

Outlook on potential French contributions (personal view)

• Conceptual design simulations

- CLD-like with MAPS and HGCal technologies
 - Needs to solve PID issue without spoiling the PFLow benefit (ex. 4D-tracking TPC large radii)
 - Difficult to reconcile with high EM energy resolution
- IDEA and IDEA+EM with Noble Liquid or Scintillating mat., DCH or TPC
 - Best performance "on paper" so far based on DCH, Crystal Cal and DR Cal

Need to clarify sub-BC timing benefits and requirements

- MAPS R&D for MIP and EM-shower tracking
 - TJ 65 nm with stitching best candidate today to provide fine pitch, at low power & X/X_0
 - > Architecture for low power and higher rates (than ALICE ITS3) to be developed
 - > Exploitation of timing to be developed (current sensor designs target O(100) ps precision)
 - Longer term, but could start now
 - > Deeper nodes & process used for commercial imagers
 - Ultimate precision position & timing with ultra-fine pitch and 3D teers rad. tol. ?
 - Access to technology difficult and expensive

→ PEPR could be an opportunity to federate efforts and resources (with some autonomy wre CERN)

- TPC R&D for low backflow & improved PID
- Possible contributions to intermediate projects: ITS3 (LS3), ALICE-3 & LHC-b (LS4)
- > FCC-hh would need parallel dedicated investigations of new materials for radiation tolerance

Summary of french R&D areas in additional information slides 19 to 22 (may not be exhaustive)

Additional information

• MAPS for Vertex Detector - O(12) sensors in 12" wafers times number of experiments



• MAPS for Central Tracking – Medium production O(100) m²



Other alternative technologies 3D, LGAD, SPADs

* Today: CMOS hybrid same order of timing precision 100 ps as MAPS, 3D and LGADS O(30) ps ** 10 ps precision covers only p < 5 GeV, 1/Vn for n layers, also increased radius option; impact of MS to be estimated for ultimate requirements

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• MAPS for High Granularity Calorimetry - large production O(1000) m²

Improve sampling fraction

Digital calorimetry

> No dedicated

- 4D within shower w/ timing <10 ps
- No dedicated R&D: group pixels in pads
- No dedicated R&D: pixels granularity
- No dedicated R&D: similar as for TL
- Summary MAPS (more phase space in CLD-like design, maybe limited to VD in other designs)
 - Current effort addressing mostly impact precision and low X/X₀
 - First attempts at exploiting timing properties with current technologies O(100) ps
 - Strong justification to develop designs that could provide \lesssim 30 ps
 - System aspects (mechanics, cooling...) important for X/X₀
 - Large community with an IN2P3 platform C4PI at IPHC
 - Intermediate project interests ex. ALICE ITS3, BELLE 2, ALICE 3, LHCB 2
 - Proper time to define common orientations beyond current R&D activities
 - Should consider technology aspects but also detector target, Vertex/Central Tracking, HGCalorimetry
 - > PEPR proposal (J. Baudot) opportunity to open R&D perimeter and structure common effort
 - Large consortium: CPPM, IJCLab, IPHC, IP2I, IRFU, LLR, LP2I, LPNHE, LPSC, Subatech
 - > Opportunity of synergies with electronics R&D MP, ex. for timing implementation (including 3D integration)
 - MP Fastime ASIC < 10 ps precision, MP Lojic130 clock precision (IP2I + ...) in 130 nm TSMC
 - Requires substancial resources both funding and RH, also competitive international environment
 - Technology access complex for sensors (so far driven by CERN) no identified path towrd 3D integration



- Summary Calorimeters (fully Conceptual Design correlated)
 - Large community for HGC and Noble Liquid
 - HGC R&D still oriented toward ILC? possible synergy with MAPS R&D; Noble liquid fully dedicated to FCC
 - > Interest to follow-up other options for contribution in a high E-γ resolution and/or DRCAL Conceptual Design
 - PEPR proposal* related to scinti.- cerenkov "Chronography" (C. Morel) timing oriented (including medical application) CPPM, ILM, IJClab, IP2I, IRFU, LPCC, LPSC, Omega
 - Requires substancial resources both funding and RH, when reaching system design level
- * No dedicated PEPR proposals for calorimetry, other that could be related to FCC R&D?



- Interest to follow-up these developments and connect them to FCC-ee
 - Resource needs relatively limited at this stages
- General conclusion: maybe a good time to form dedicated FCC-ee MPs acknowledged by IN2P3 & IRFU
 - Common with ILC existing progams where relevant
 - Will need to consider implementation of DRD proposals under ECFA

LHCb post LS4: first large scale application 30 m²

UT upstream magnet 6 m^2 MT at low r within SciFi 20 m^2

- 50 x 150 100 x 300 pitch
- $\lesssim 5 \times 10^{14} \text{ neq/cm}^2$



Alice 3 (LS4) – MAPS 20 μ m pitch - BC timing 25 ns - 10¹³ neq/cm²



VD and Si Central Tracker: mechanical design and integration



ex. ALICE ITS3

Retractable concept to approach beam at 5 mm inside Beam Pipe



From C. Gargiulo ECFA R&D TF8 Symposia

In ALICE ITS2 0.36 % X/X₀ /layer of which: 15% Sensors, 50% Printed Circuit, 20% Cooling Circuit, 15% Support Structures

Central Tracker: Drift CHamber & TPC



Momentum resolution (B=3.5T)	$\delta(^{1}/p_{t} \approx 10^{-4}/GeV/c)$			
δ_{point} in $r\Phi$	<100 µm			
δ_{point} in rz	0.4-1.4 mm			
Inner radius	329 mm			
Outer radius	1800 mm			
Drift length	2350 mm			
TPC material budget	$\approx 0.05 X_0$ incl. field cage $< 0.25 X_0$ for readout endcap			
Pad pitch/no. padrows	$\approx 1 \text{ mm} \times (4 \sim 10 \text{ mm}) / \approx 200$			
2-hit resolution	$\approx 2 \text{ mm}$			
Efficiency	>97% for TPC only ($p_t > 1 GeV$) >99% all tracking ($p_t > 1 GeV$)			

track

end-plate

readout module

	Pixel TPC with double meshes	Triple or double GEMs	Resistive Micromegas	GEM+ Micromegas	Double meshes Micromegas	
	IHEP, Nikehf	KEK, DESY	Saclay	IHEP	USTC	
	Pad size: 55um-150um square	Pad size: 1mm×6mm	Pad size: 1mm×6mm	Pad size: 1mm×6mm	Pad size: 1mm×6mm (If resistive layer)	
	Advantage for TPC: Low gain: 2000 IBF×Gain: -1	Advantage for TPC: Gain: 5000-6000 IBF×Gain: <10	Advantage for TPC: Gain: 5000-6000 IBF×Gain: <10	Advantage for TPC: Gain:5000- 6000 IBF×Gain: <5	Advantage for TPC: High gain: 10^4 Gain: 5000-6000 IBF×Gain: 1-2	
	Electrons cluster size for FEE: About Ø200um	Electrons cluster size for FEE: About Ø5mm	Electrons cluster size for FEE: About Ø8mm	Electrons cluster size for FEE: About Ø6mm	Electrons cluster size for FEE: About Ø8mm	
	Integrated FEE in readout board Detector Gain: 2000	FEE gain: 20mV/fC Detector Gain: 5000-6000	FEE gain: 20mV/fC Detector Gain: 5000-6000	FEE gain: 20mV/fC Detector Gain: 5000-6000	FEE gain: 20mV/fC Detector Gain: 5000-6000	

Particle ID, broad-brush coverage of technology options



Commercial imager technologies



Samsung: 1.4 μm pixels in 65 nm & 14 nm Fin-FET (3D transistors) readout , wafer level stacking

* V. Re: <u>https://indico.cern.ch/event/999816/</u>

Sony(left) 3D layer thinned to 3 μm, DRAM for 960 fps Samsung (right) 1.2 μm pixel pitch, 2.5 μm TSV 6.3 μm pitch, 20 nm DRAM, 28 nm logic

Comparison of e-e collider beam parameters

Update to 100 - 5 x 10³⁴ cm⁻² s⁻¹ ?

Beam parameters	IL	.C		CLIC			FCC-ee		🖌 Ce	epC
Energy (TeV)	0.25	0.5	0.38	1.5	3	0.091	0. 24	0.36	0.091	0.24
Luminosity (x 10 ³⁴ cm ⁻² s ⁻¹)	1.35	1.8	1.5	3.7	5.9	230	8.5	1.7	32	2.93
Bunch train frequency (Hz)	5		50							
Bunch separation (ns)	554		0.5		20	994	3000	25	680	
Number of bunches / train - beam	1312		352	31	12	16640	393	48	12000	242
Integrated luminosity (ab-1)/years	2/+11	4/+22	1/8	2.5/8	5/8	150/4	15/5	1.7/5	16/2	5.6/8
Main SM process	ZH	tt, ttH	tt			Z	WW, ZH	tt	Z	WW,ZH
Beam size at IP σx/σy/σz (μm)	515/7.7/300	474/5.9/300	150/2.9/70	60/1.5/44	40/1/44					