Phase-II TilePPr Upgrade
What to consider from the TREX experience

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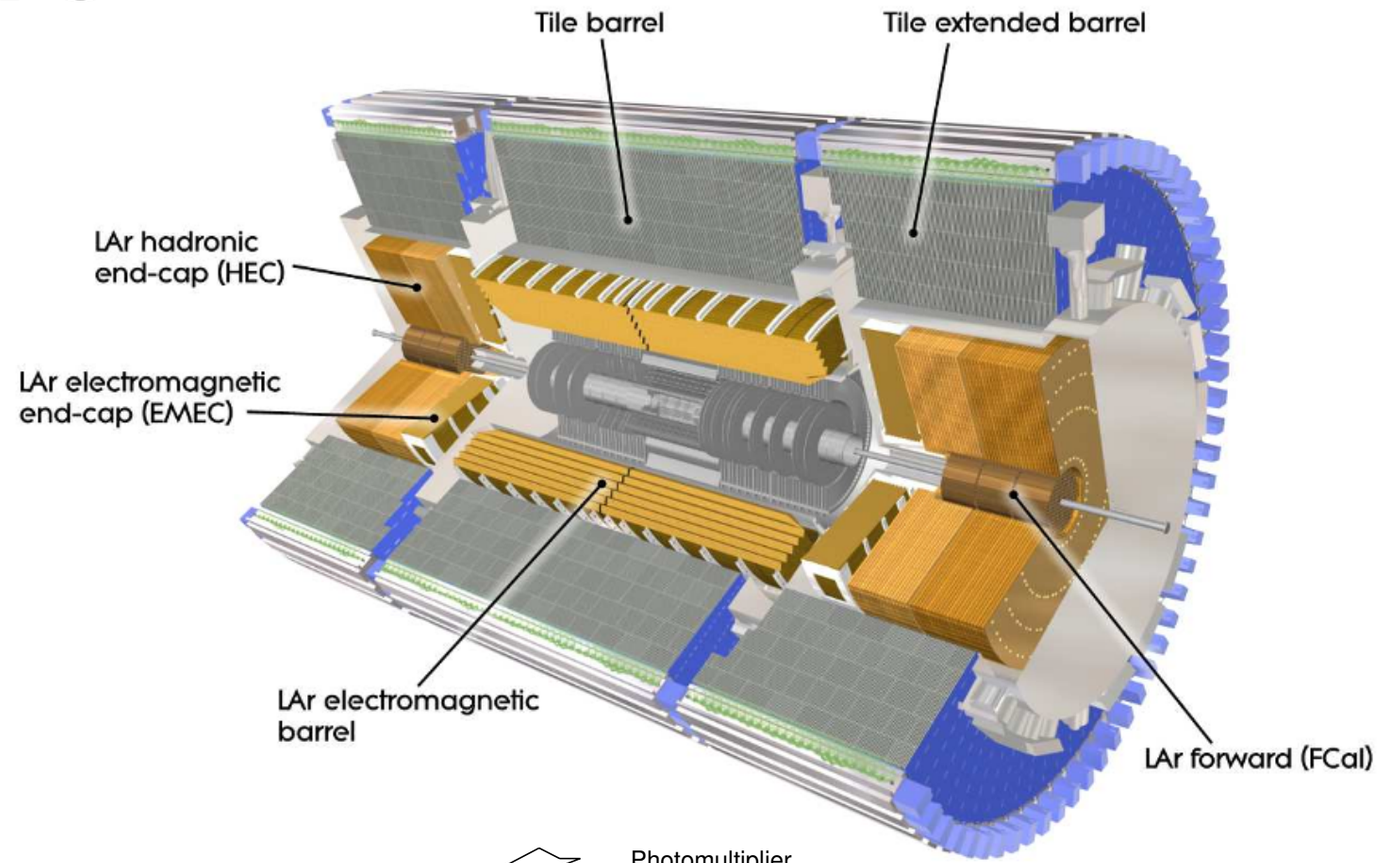
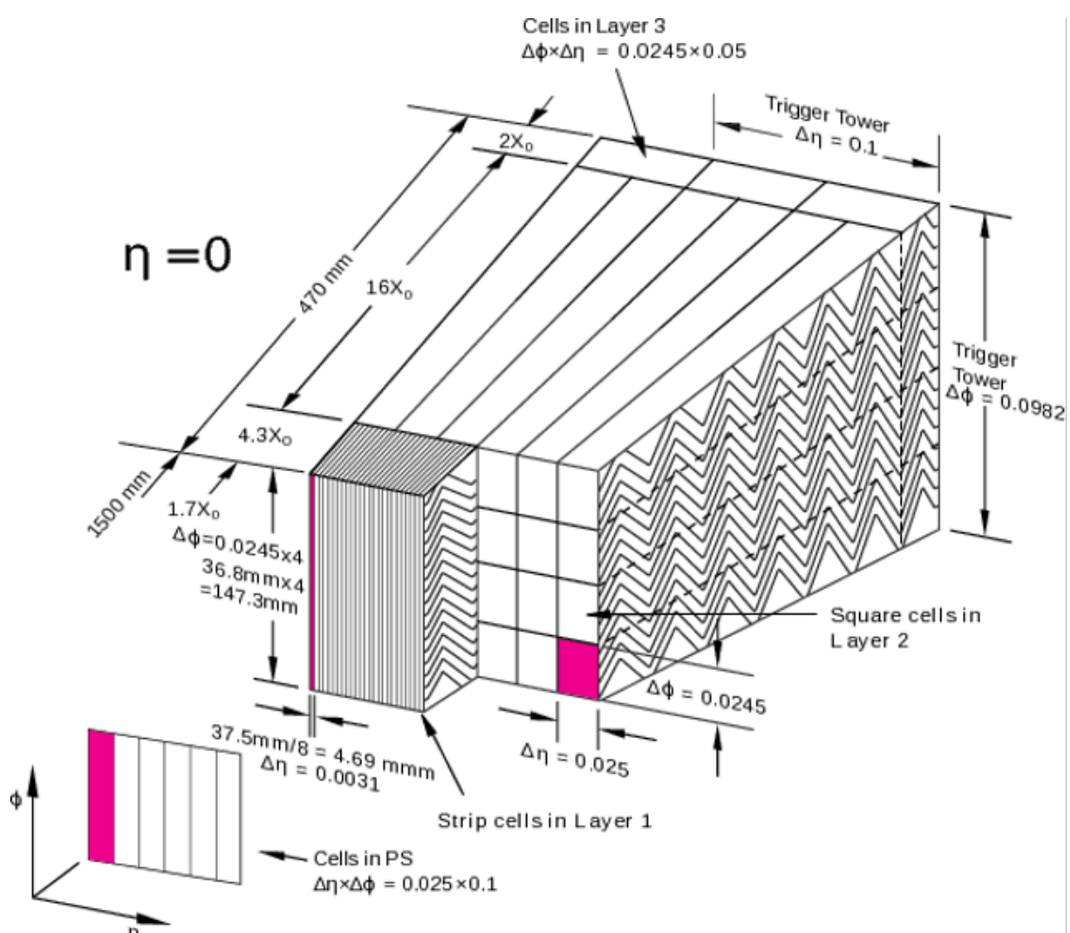
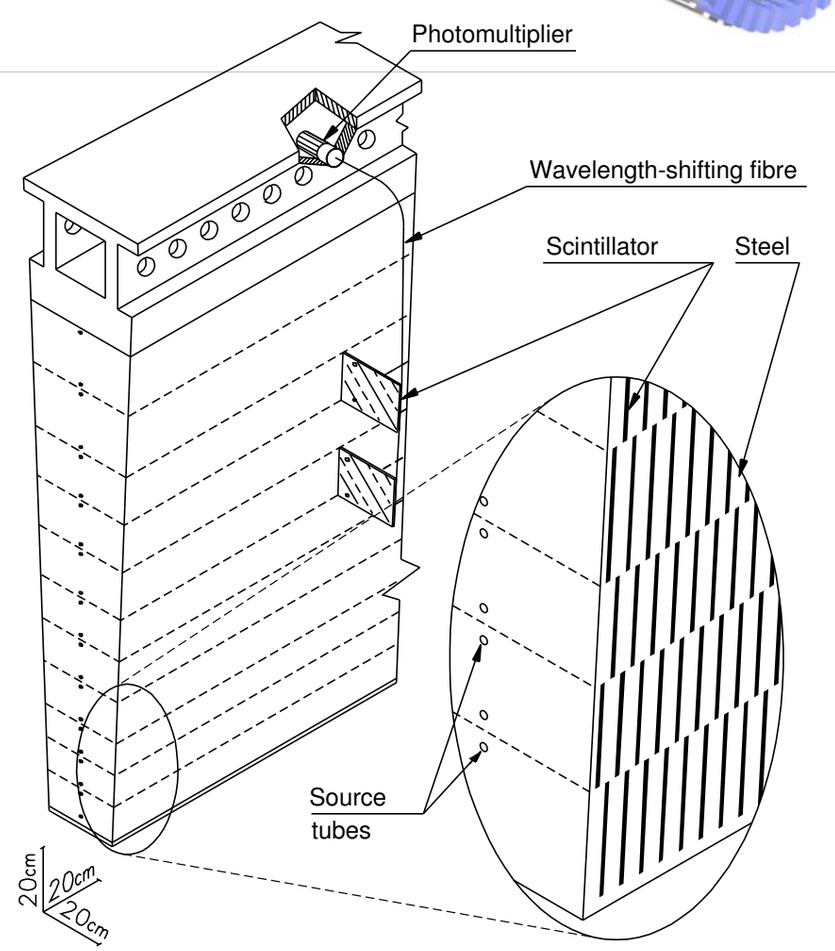
ATLAS Calorimeters

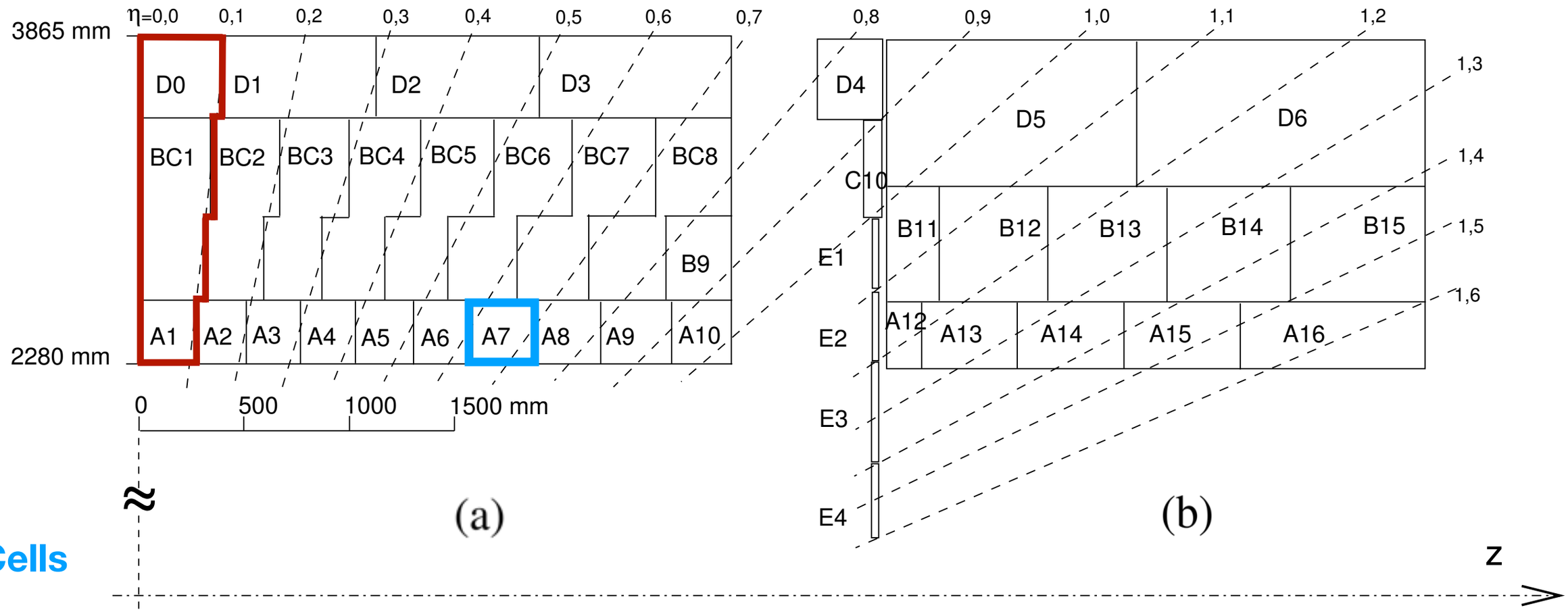
- Electromagnetic - **LAr**
- Hadronic - **Tile**
- Segmentation of $\Delta\eta \times \Delta\phi$
  - LAr: 0.025 x 0.025
  - Tile: 0.1 x 0.1





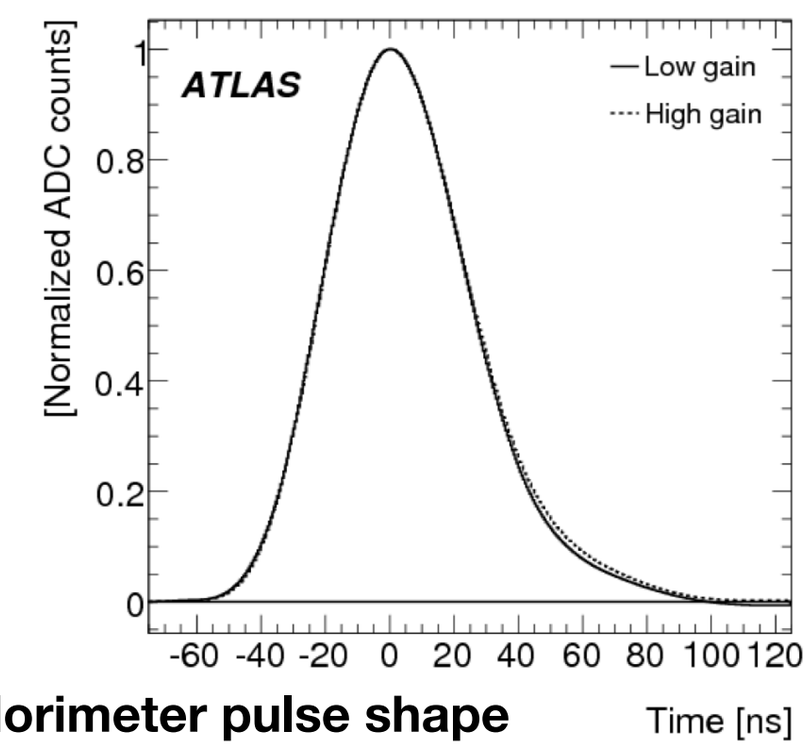


Tile Calorimeter



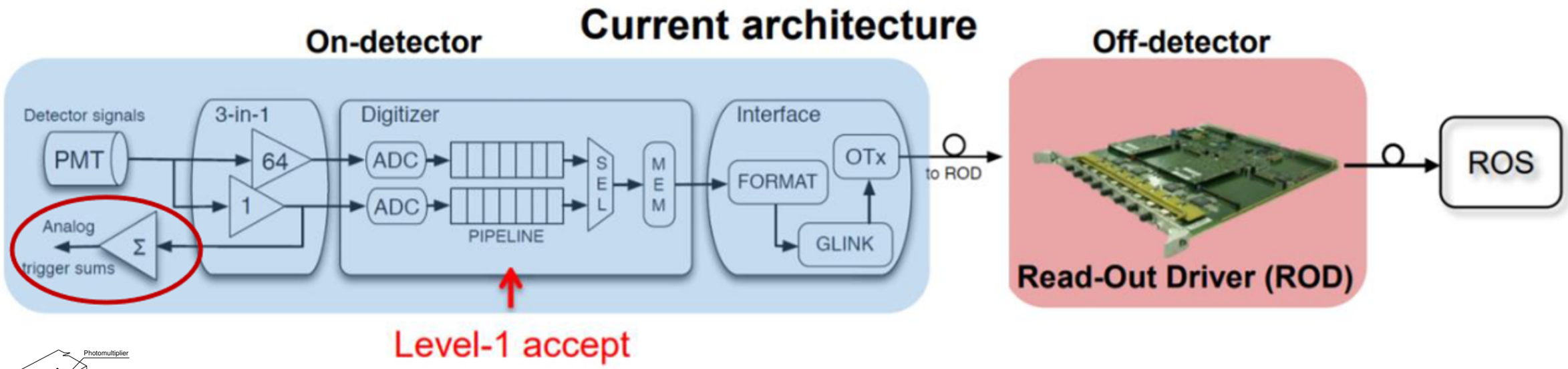
- **Cells**
- **Trigger Tower**

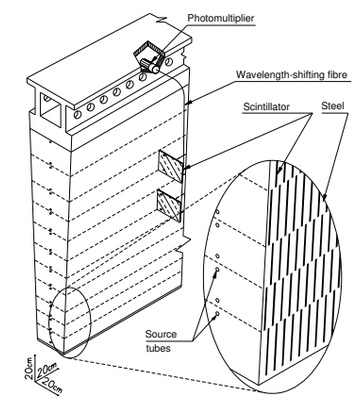
- Sampling calorimeter
- Plastic scintillators as active medium
- Steel as absorbers
- 256 modules
  - ~5000 cells and ~10 000 photomultipliers

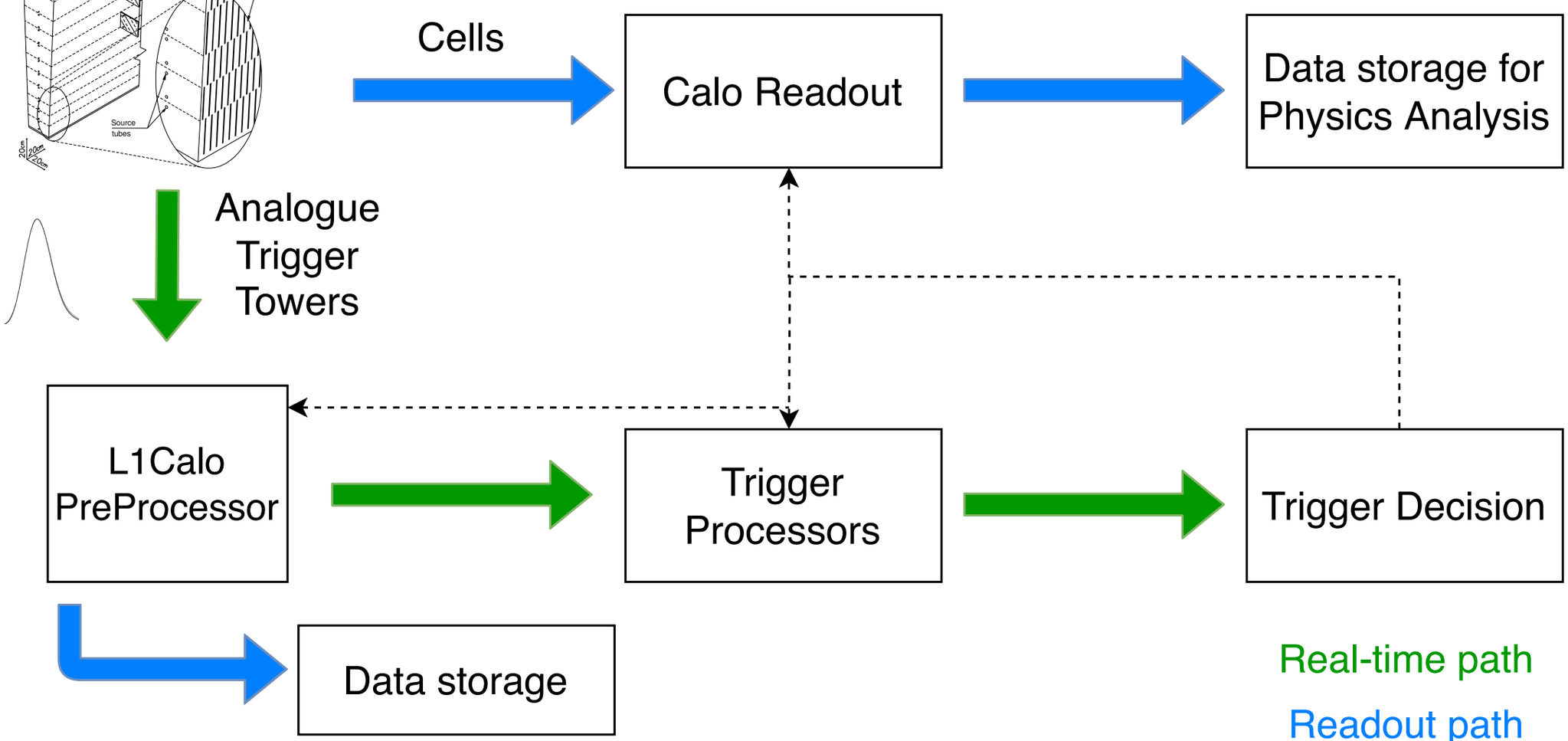


Calorimeter pulse shape

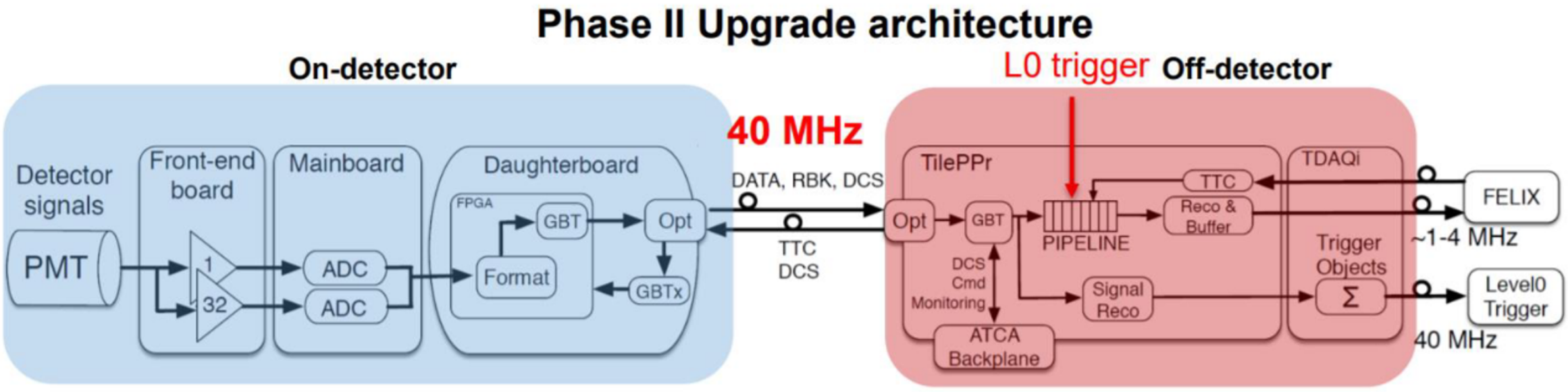
Current Dataflow vs Upgrade

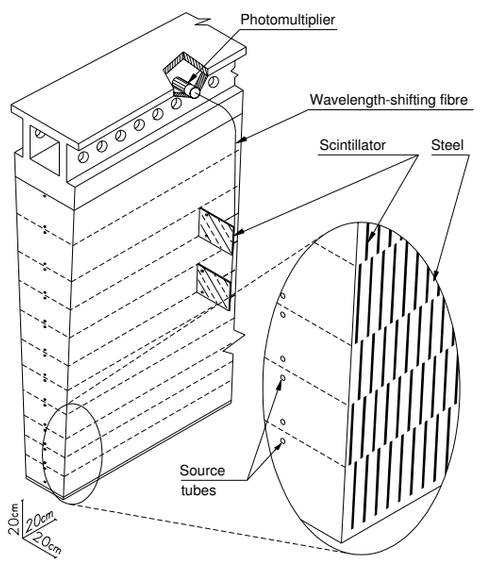


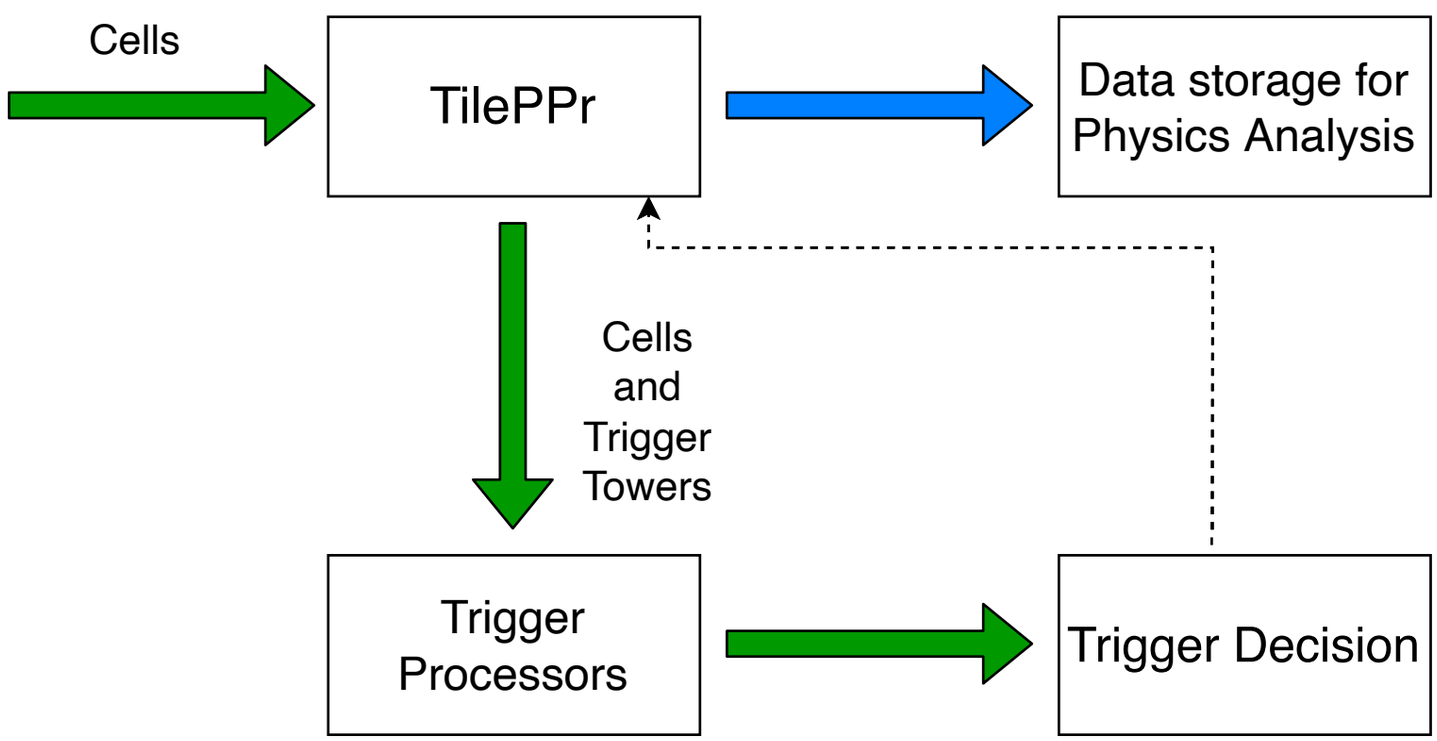




Current Dataflow vs Upgrade







Real-time path

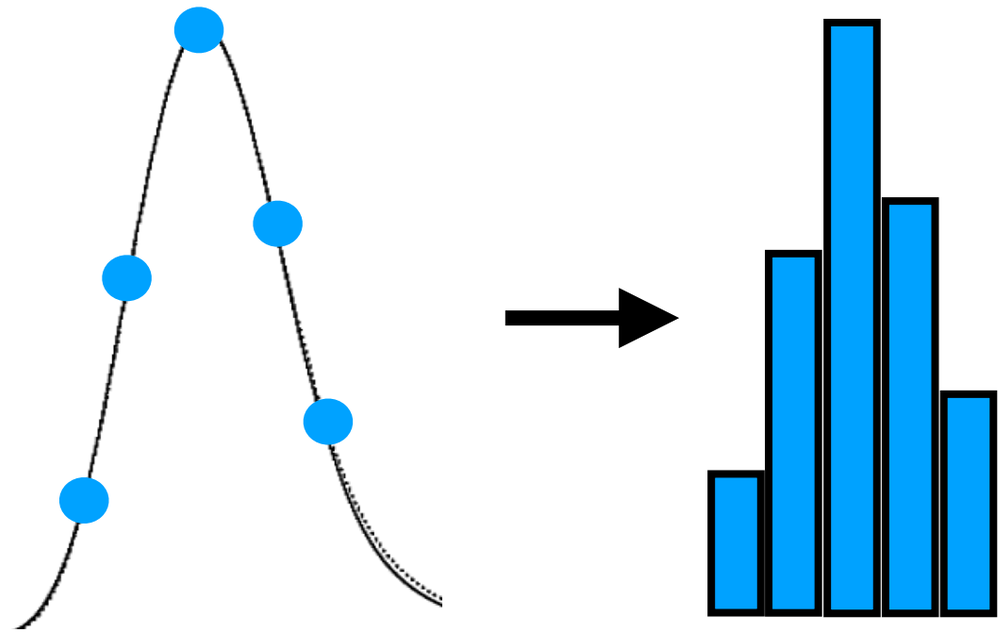
Readout path

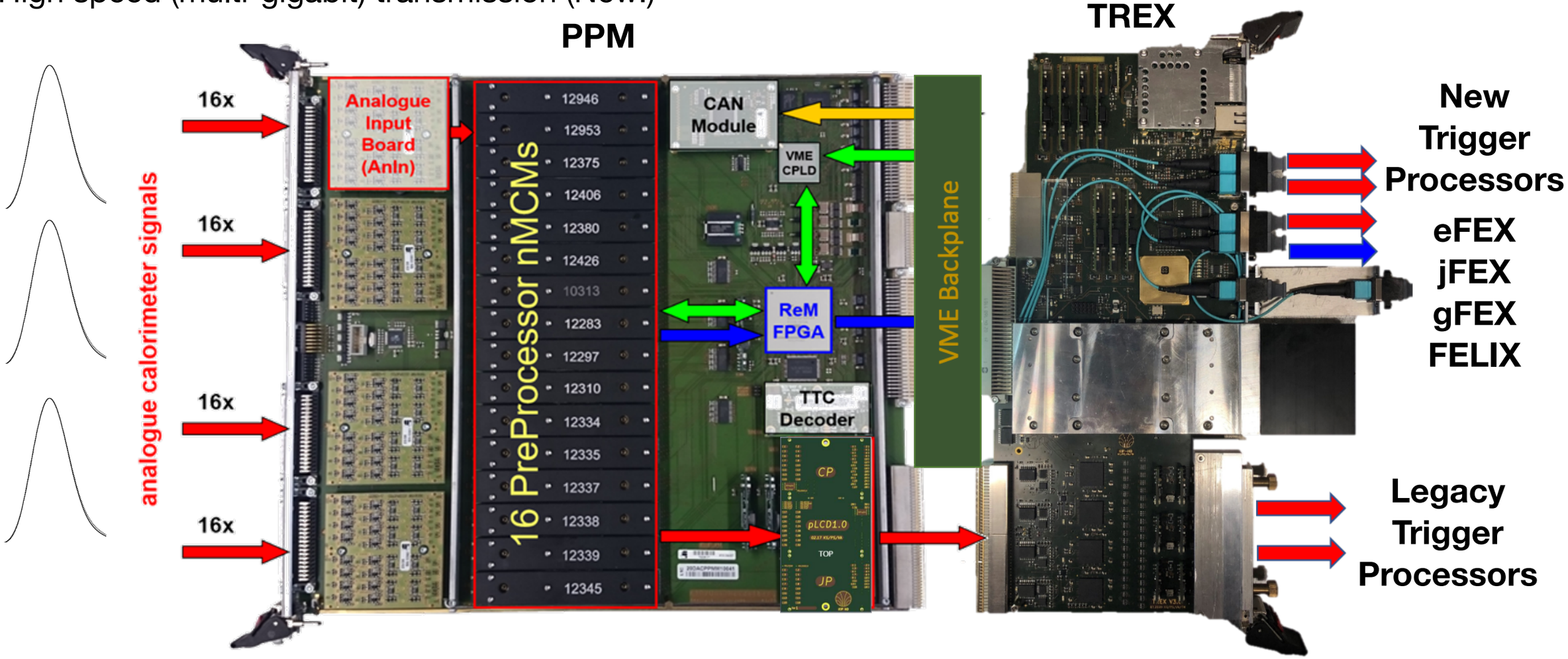
What is a PreProcessor?

- Field Programmable Gate Array (FPGA) -based system for fast custom data processing and I/O
    - Integrated circuit with configurable logic blocks
- First point in the off-detector dataflow
- Initial treatment/processing of the digital data
    - Energy reconstruction - reconstruction of the pulse based on finite digital samples
    - Bunch-Crossing Identification - assignment of the energy to the correct LHC bunch crossing
    - Synchronisation of all input signals
- Formatting and transmission to processors which run higher-level algorithms

Current PreProcessor?

- Analogue inputs from the calorimeter
- Digitisation - 5 to 15 samples
- Bunch crossing identification
- Peak-finding, ADC -> MeV conversion
- Digitised data stored in a pipeline awaiting trigger decision
- High speed (multi-gigabit) transmission (New!)

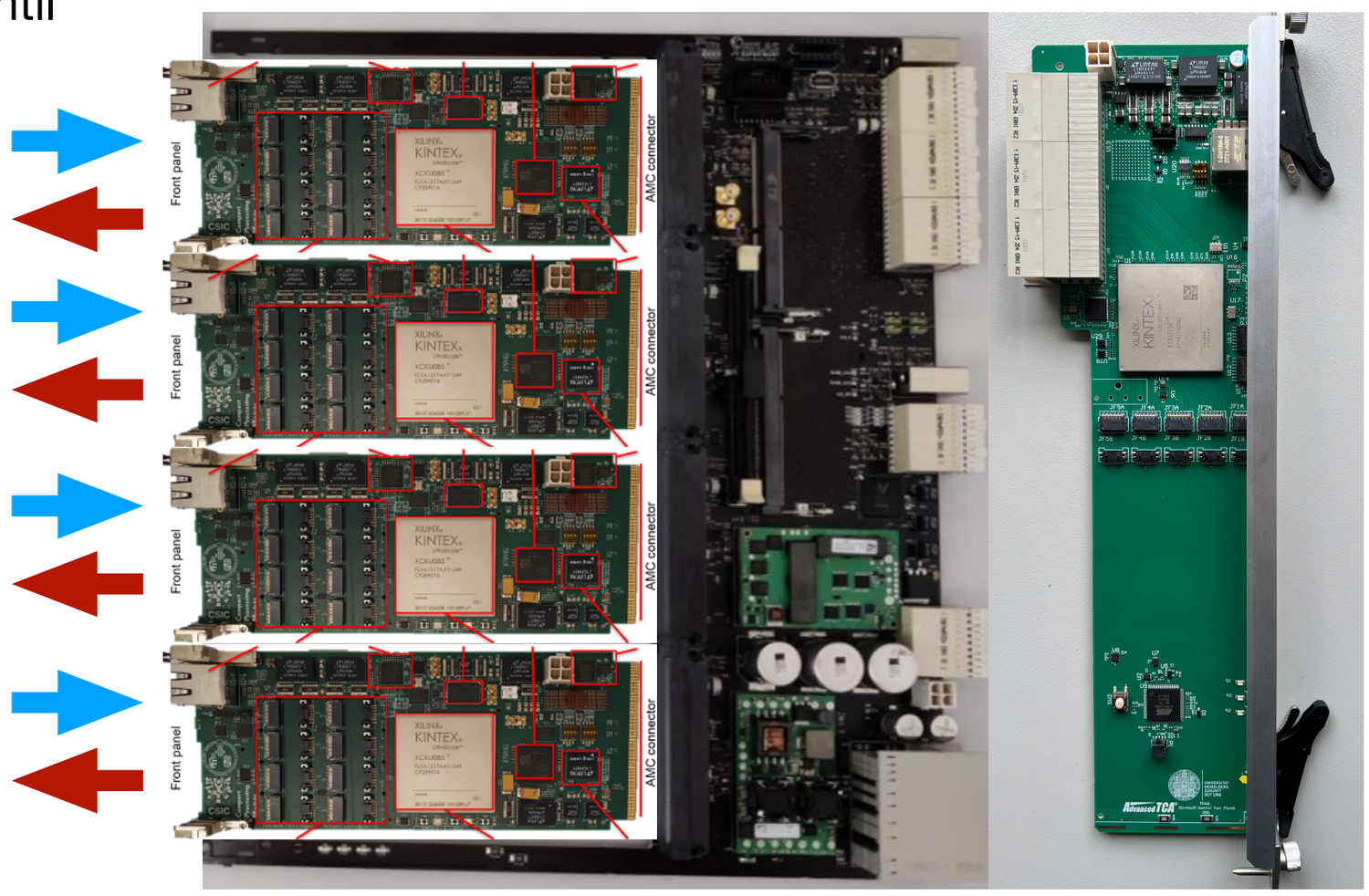




Upgrade PreProcessor

- Hub between on-detector & off-detector
  - Control and configuration of the on-detector electronics
  - Large data pipelines - data stored until trigger decision is made
- Processes 2 Tile modules/PPr
- Energy reconstruction for
  - Real-time - latency critical
  - Readout
- High-speed connectivity
  - Between On-detector
  - Between Trigger Processors
- In the prototyping stage

Compact Processing Modules



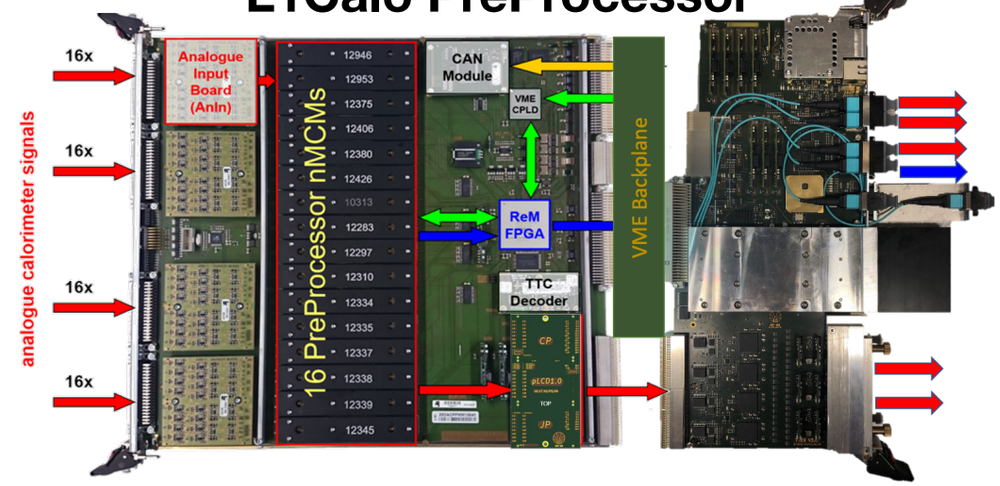
Carrier Board

TDAQi

Differences and similarities

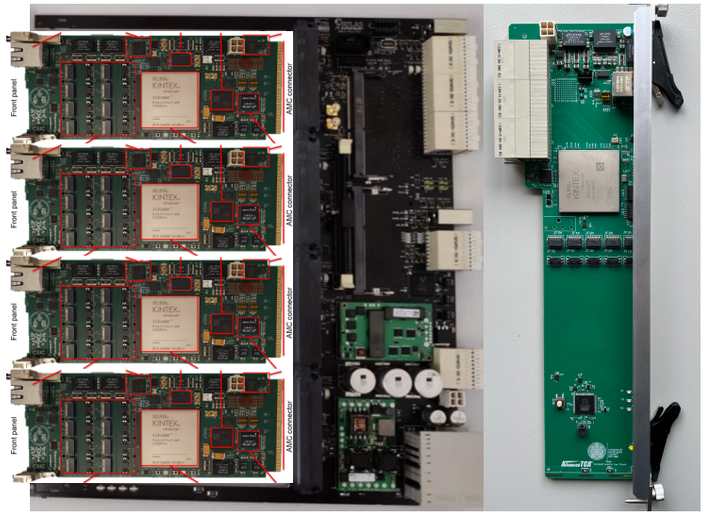
- Receives analogue signals
  - Analogue summed towers (coarse)
- Digitisation performed off-detector
- **8-bit** transverse energy E_T sent to Trigger processors
- High-speed optical outputs
- **100 kHz** data rate to the High-Level-Trigger (HLT)

L1Calo PreProcessor



VS

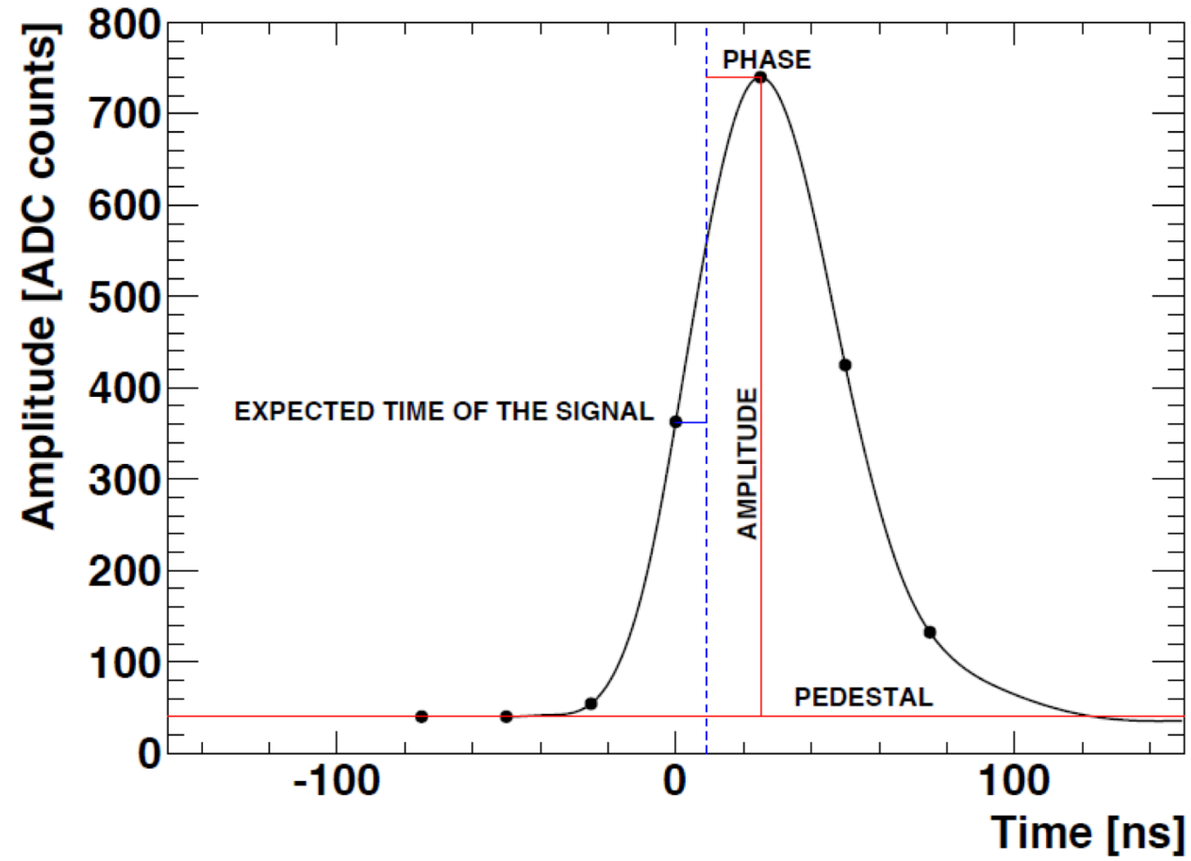
- Receives pre-digitised data from on-detector
- Trigger Towers formed by digital sums of cell energies
- **16-bit** cell energy E and time reconstruction - higher precision
- High-speed optical inputs and outputs
  - Radiation Tolerant Transfer Protocols
- **1 MHz** data rate to the HLT



TilePPr

Energy reconstruction

- Amplitude is proportional to the energy deposit
- Digital Filters are used to obtain the real amplitude
- Current PreProcessor uses FIR-based Peak-Finder algorithm
  - Improve the signal-to noise ratio
  - The filter output is calibrated to E_T via a Look-Up-Table (LUT)
- New hardware allows for more sophisticated reconstruction algorithms - more processing cycles
  - Optimal Filtering (baseline)
  - Wiener and Fit Filters
  - ANNs



Peak finder conditions

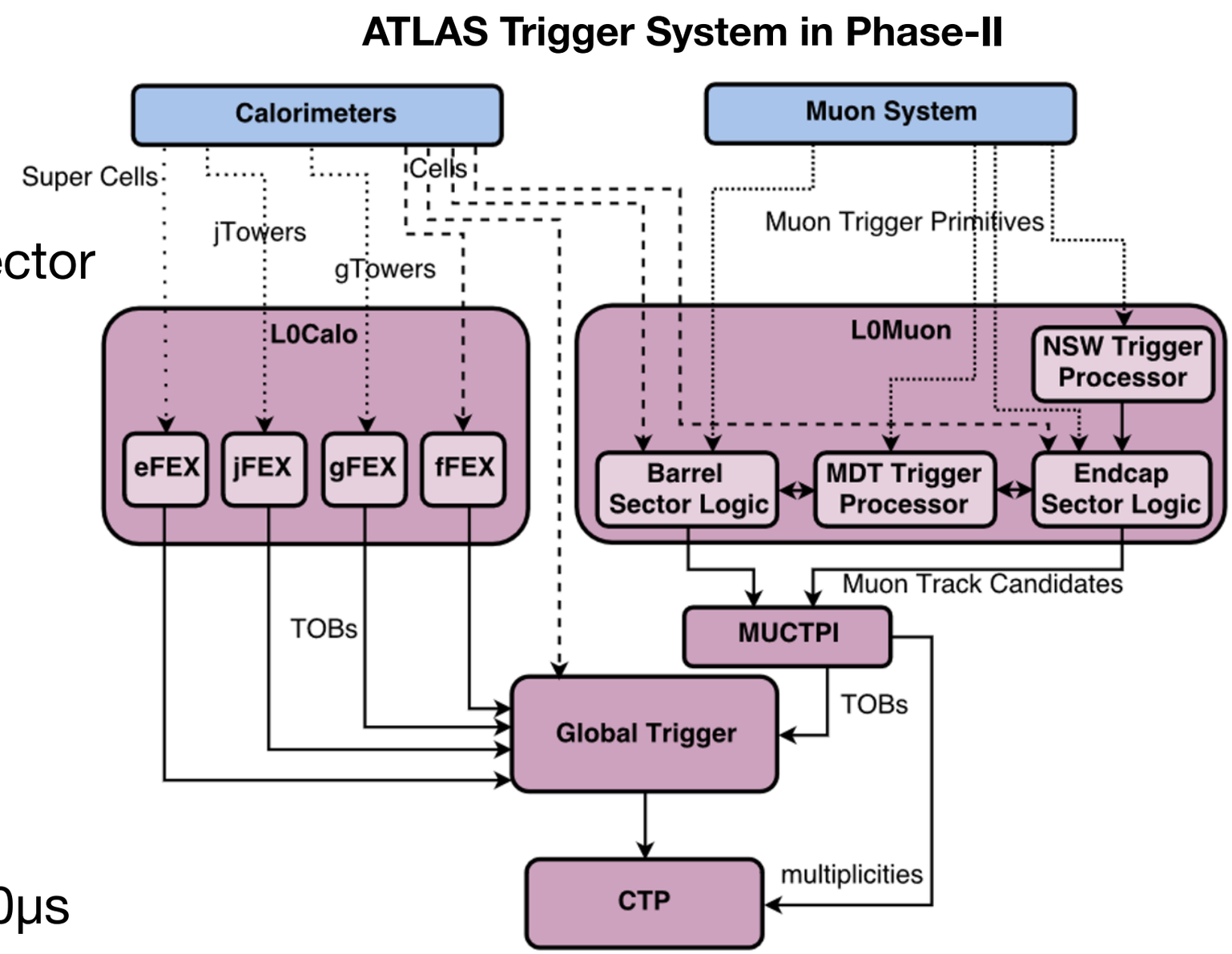
$$f_i = \sum_{k=0}^{4} c_k A_{i-k} \qquad f_{i-1} < f_i \geq f_{i+1}$$

Optimal Filtering based on weighted sums of the samples

$$E = \sum_{i=1}^{n} a_i S_i \qquad E\tau = \sum_{i=1}^{n} b_i S_i$$

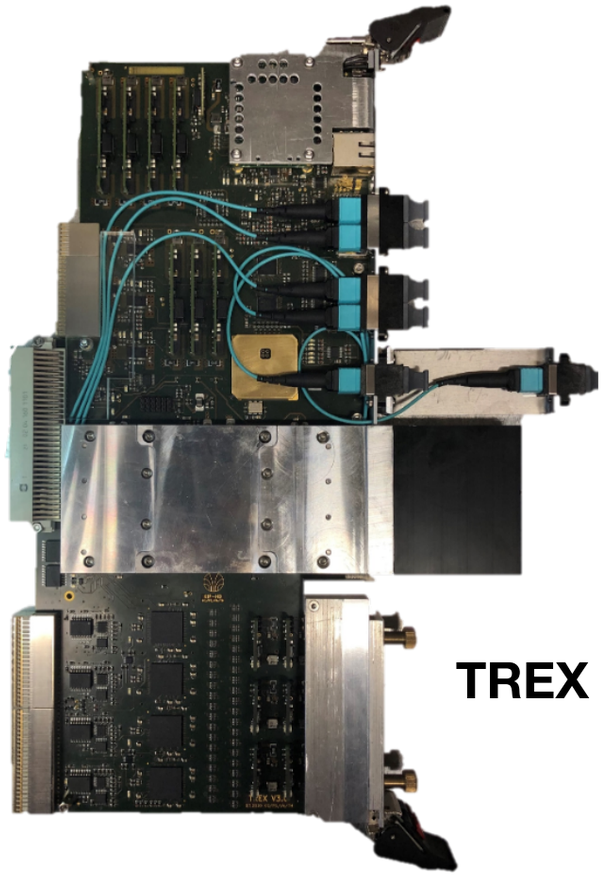
ATLAS Trigger System

- Fully digital Trigger system
- Only optical inputs from the detector
- L1/0Calo - Calorimeter Trigger
- L0Muon - Muon Trigger System
- Global Trigger
  - See Fer's talk
- Estimated allowed latency of ~10μs



The Tile Rear eXtension (TREX)

- Enables the input to L1Calo FEX modules
- Full system consists of 32 modules
- Sending 8-bit E_T results and 12-bit BC number to FEXes
- Alignment & synchronisation
- Data formatting & packing
- Latency optimised
- Electrical (for legacy) and optical outputs
- Fast data transmission
  - Real-time links @ 11.2 Gbps
  - Readout links @ 9.6 Gbps

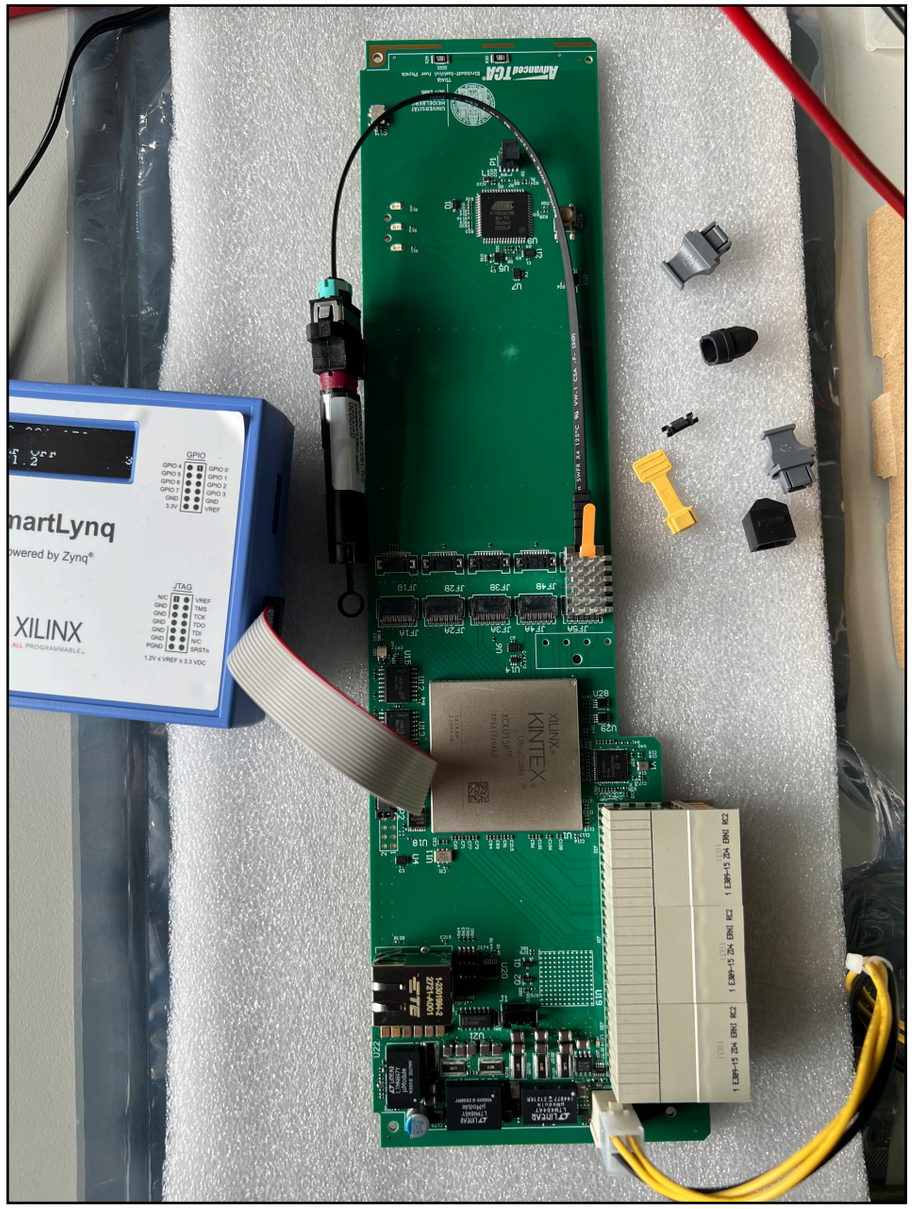


TREX Module

TREX modules installed in ATLAS

The Trigger and DAQ interface (TDAQi)

- Full system consists of 32 modules
- Receives cell energies from 4 CPMs
- E -> E_T conversion
- Summing of Cells to Towers
- Sorting of cells by E
- Energy flags for cells or a group of cells
- New additional interfaces in addition to L1Calo
    - L0Muon and Global
- All 3 Triggers processors uses different input formats
- Formatting and packing of data
- Purely optical outputs



TDAQi prototype under test at KIP

High speed data transmission

- Links speeds ranging from 9.6 up to 11.2 (12.8) Gbps
- Various frequency domains in the firmware
- Quality is measured via a Bit Error Ratio (BER)
- Error-free transmission is critical
  - Full validation of transmitters required
- Acceptable BER rates from 10^{-13} to 10^{-15}

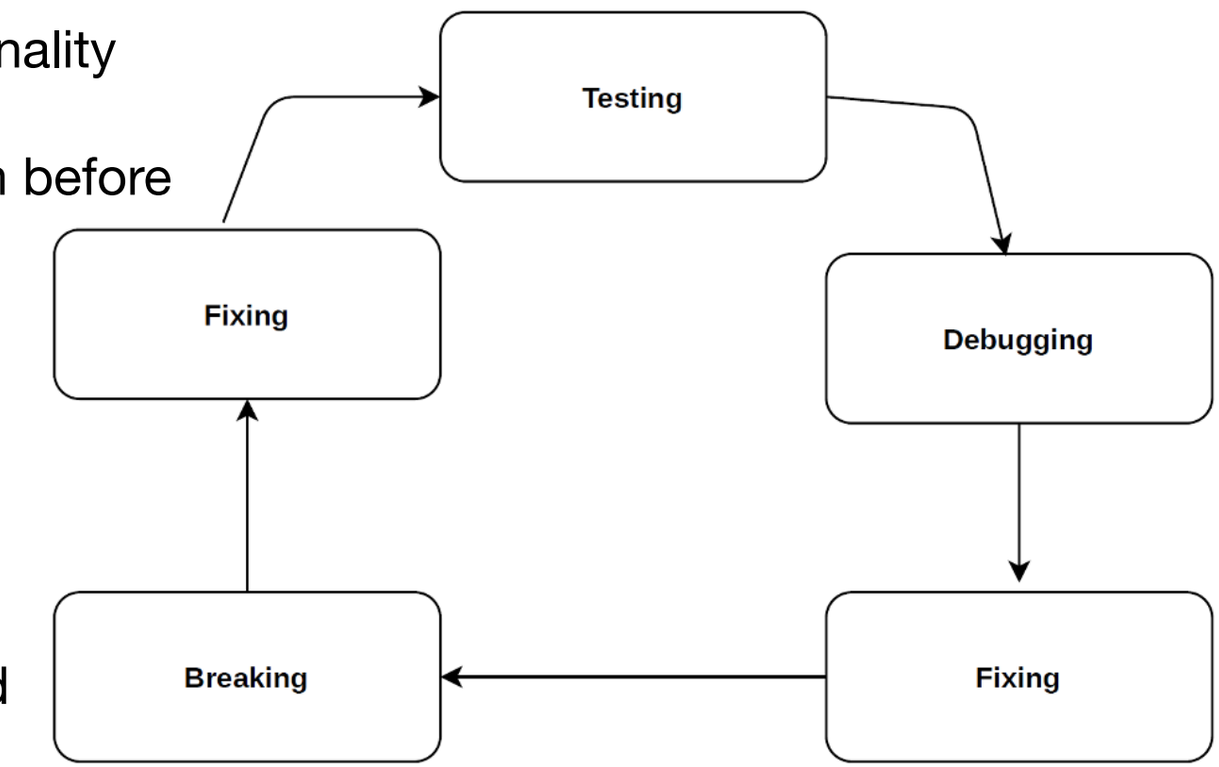
Module	Bandwidth (Module)	Data output (Full System)
TREX	• 290.4 Gbps (36.3 GB/s)	• 9.3 Tbps (1.2 TB/s)
TDAQi	• 486.4 Gbps (60.8 GB/s)	• 15.5 Tbps (1.95 TB/s)

$$BER = \begin{cases} \dfrac{N_{error}^{bits}}{N_{transferred}^{bits}}, N_{error}^{bits} > 0 \\ \\ \dfrac{1}{N_{transferred}^{bits}}, N_{error}^{bits} = 0 \end{cases}$$

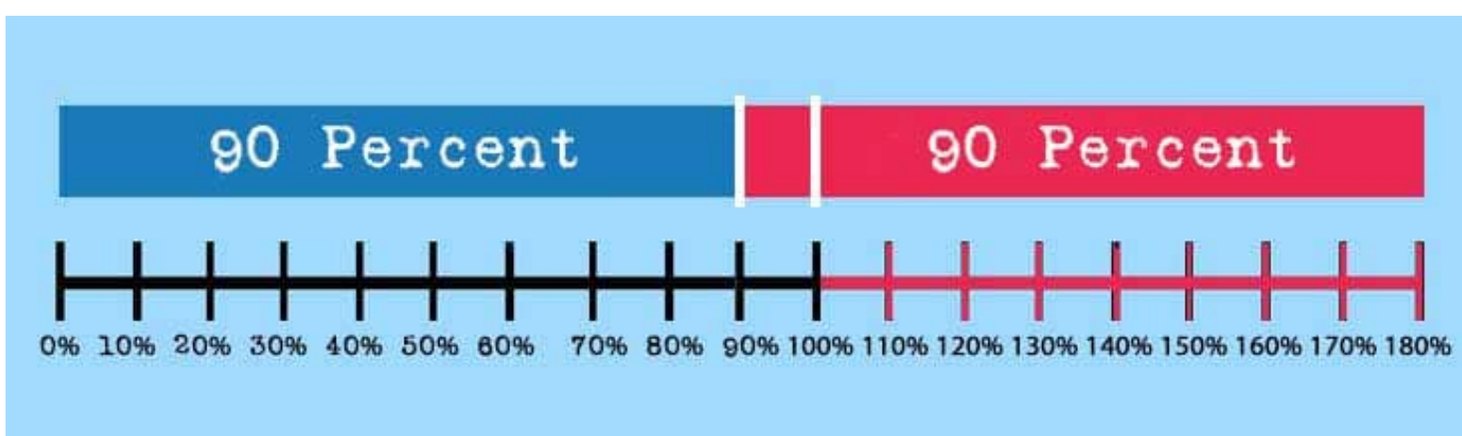
TX	RX	Status	Bits	Errors	BER
Quad_234/MGT_X0Y41/TX (xcku15p_0)	Quad_234/MGT_X0Y40/RX (xcku15p_0)	11.222 Gbps	6.626E12	0E0	1.509E-13
Quad_234/MGT_X0Y42/TX (xcku15p_0)	Quad_234/MGT_X0Y41/RX (xcku15p_0)	11.222 Gbps	6.626E12	0E0	1.509E-13
Quad_234/MGT_X0Y40/TX (xcku15p_0)	Quad_234/MGT_X0Y42/RX (xcku15p_0)	11.222 Gbps	6.626E12	0E0	1.509E-13
Quad_234/MGT_X0Y43/TX (xcku15p_0)	Quad_234/MGT_X0Y43/RX (xcku15p_0)	11.222 Gbps	6.626E12	0E0	1.509E-13

Experience designing and operating the TREX

- Both the L1Calo and the TilePPr are complex systems
    - Establish the test coverage of all features/ functionality
    - Scaling the system reveals further issues not seen before
- Latency
    - Very critical in real-time processing
    - Required to be minimised and deterministic
- Multi-Gigabit transceivers require processing overhead
- FPGA resources might be available - doesn't necessarily mean firmware will fit
- Overall the projects require tight coordination and integration with the receiver modules

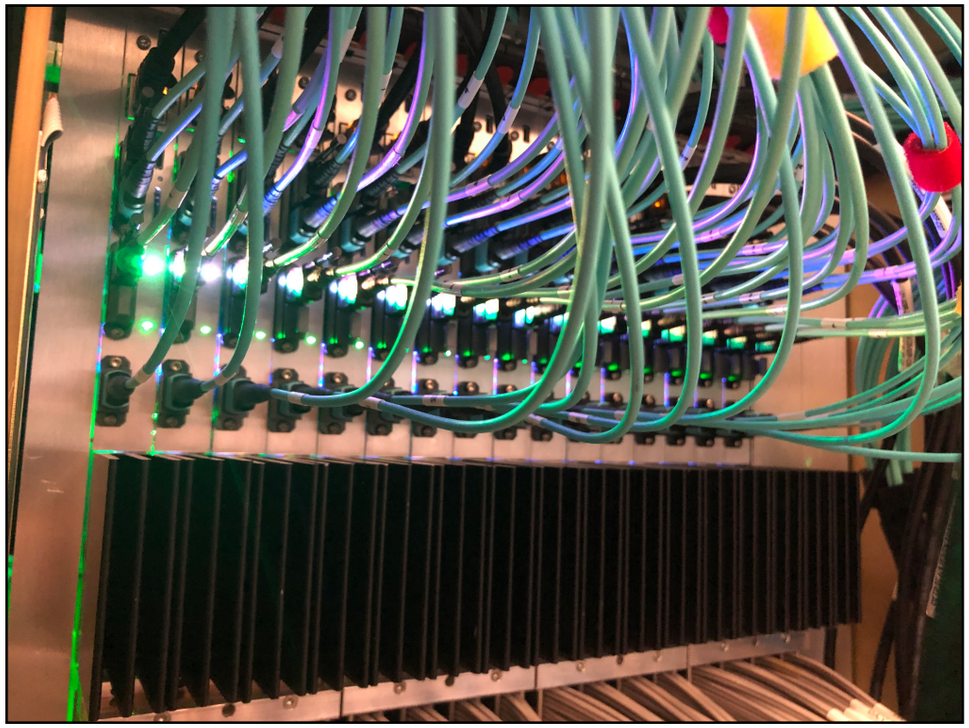


90-90 rule is very much true



Summary

- The TREX system has been designed, developed and integrated in ATLAS for Run3 - about to start in a months time
- Gained expertise in high-speed transmission and much more
  - Exploited the logic and interfaces TREX and TDAQi share
  - Latency-critical applications require careful and precise implementation
- Experience from TREX being used for the TDAQi
  - Similar technology utilised in both
- Experience designing real-time systems also used for the TilePPr

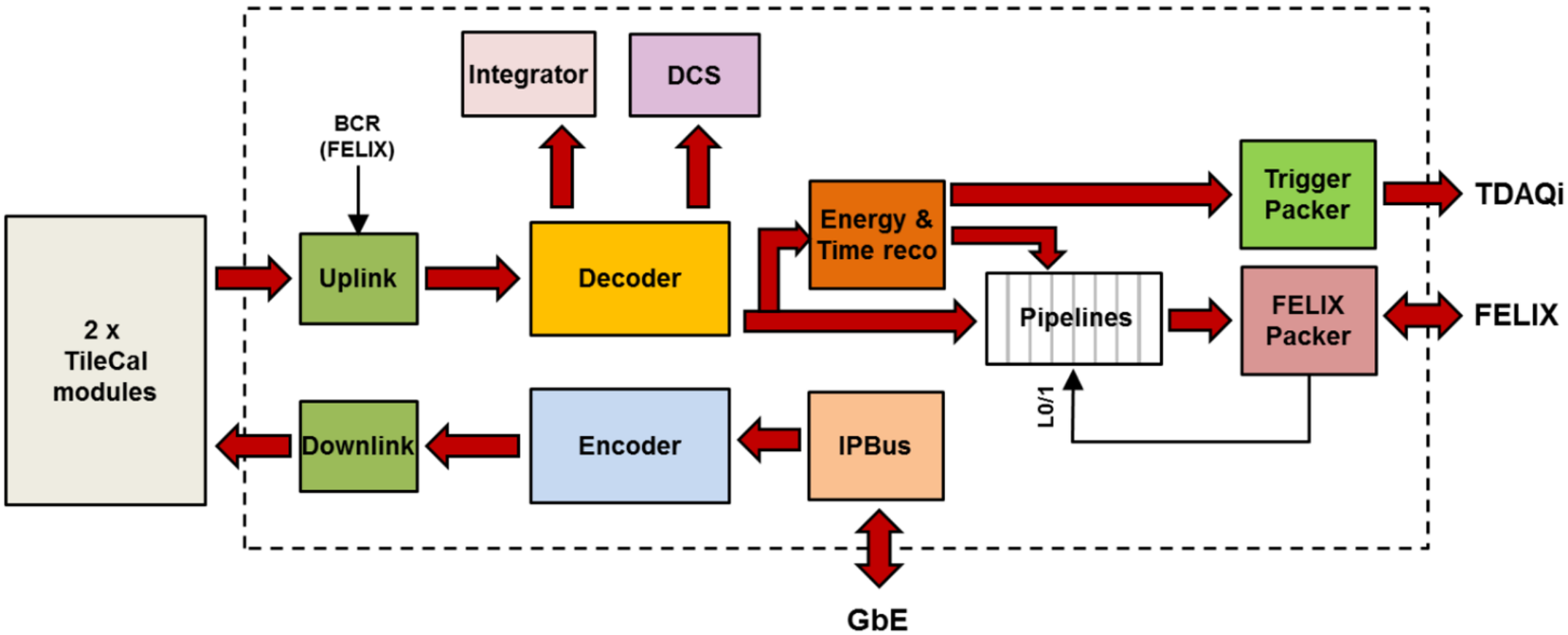


TREX output fibers in ATLAS

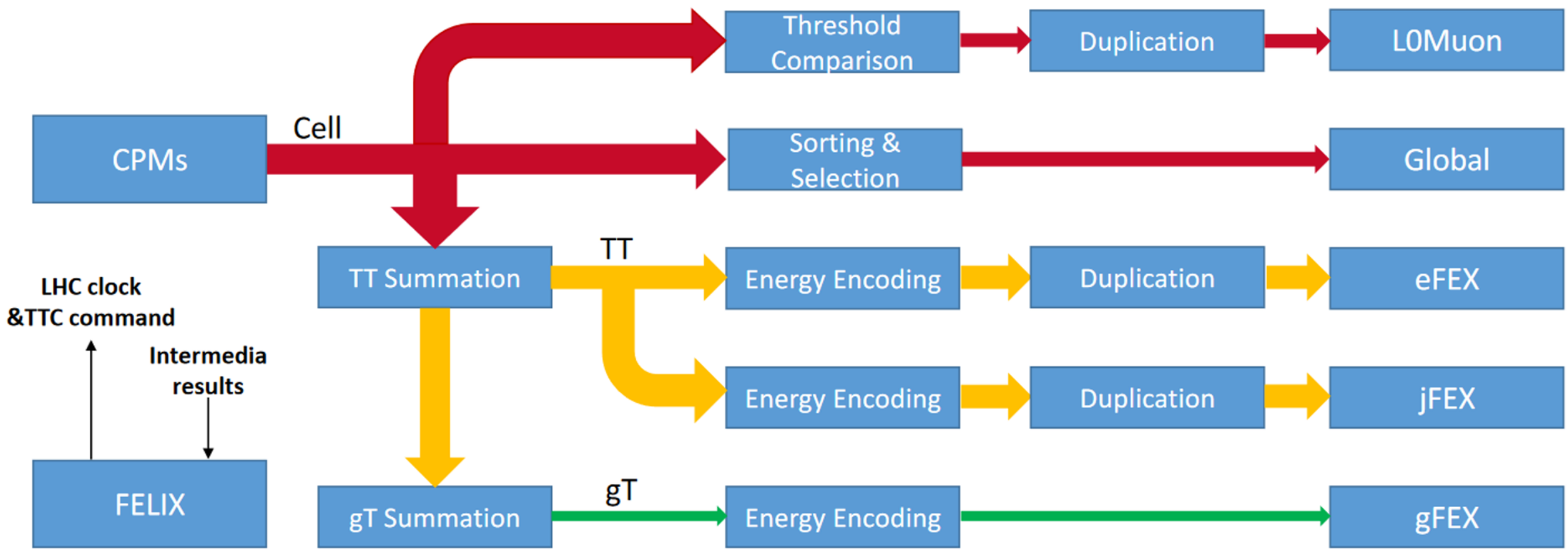
TilePPr Prototype

Backup

CPM Overview



TDAQi Overview



Out-of-time pile-up