Machine Interlocks Upgrading

Christophe MARTIN MPE workshop 14th Dec. 2010

Outline

- New HW designs for SMP* project
- New HW designs for BIS** project

- New VME platform supplied by BE/CO
- New interface for the FMCM units proposed by BE/CO

* Safe Machine Parameters

** Beam Interlock System

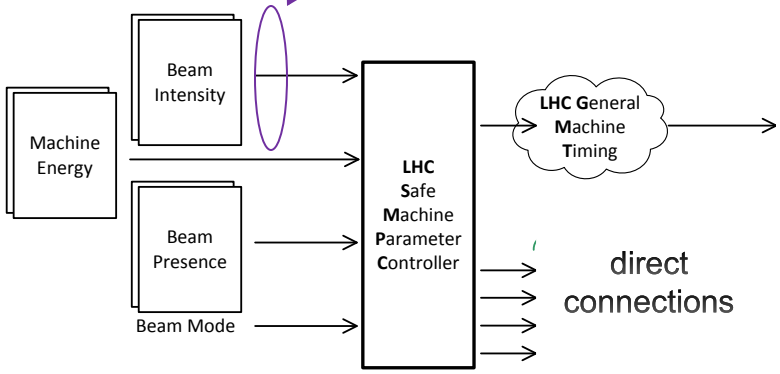
New designs for SMP project (1/2)

- New CIST board

(Used to transmit serial data from Equipment system to SMP controller)

- Replace the existing Timing module (named CTG)
- Main features:
  - Purely Hw (no more libraries, no more remote downloading…)
  - History buffer

- New FESA class
- New screen in Java application

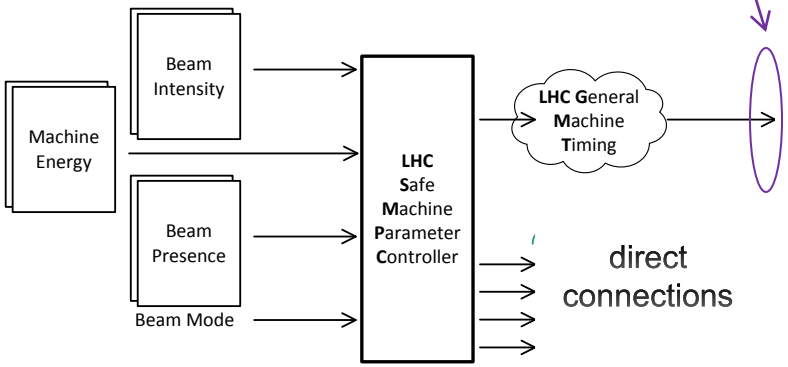


New designs for SMP project (2/2)

- CISV upgrade

  (Used to receive SMP data broadcasted by the Timing system)

  - New VHDL code with following main features:
    - Improvement internal process
    - History buffer
  - New FESA class
  - New screen in Java application



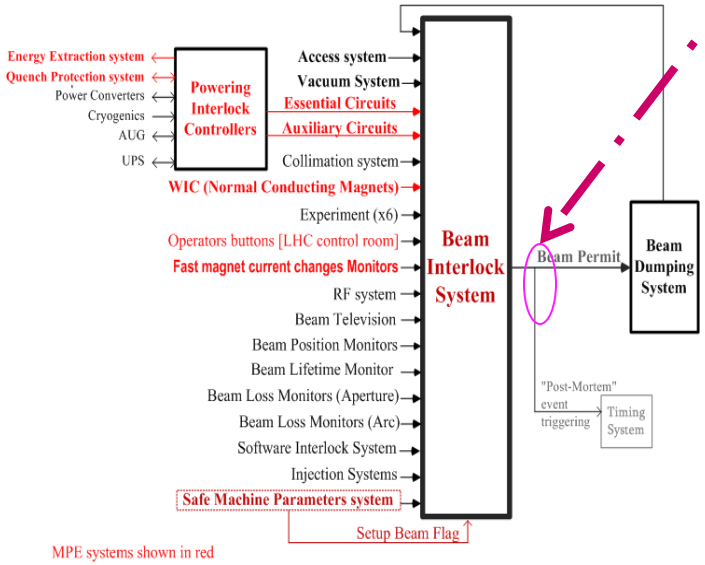
New designs for BIS project (1/5)

- New CIBV board

  (trigger to the LHC Timing for generation of PM event)

  - Replace the current Timing board
  - new VHDL in including new History Buffer

  - New FESA class
  - New screen in Java application



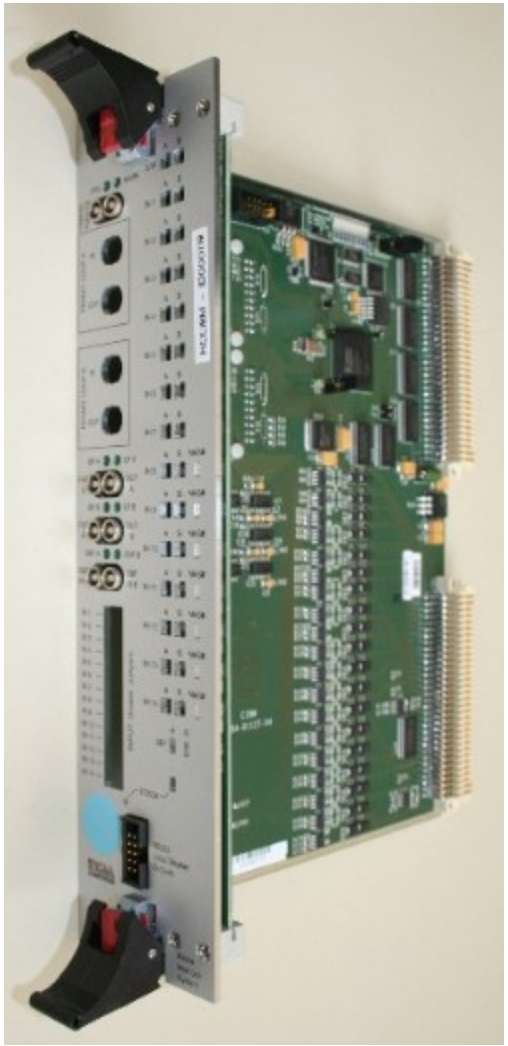
New designs for BIS project (2/5)

- CIBM upgrade

  (Main BIS element: it contains redundant Matrices and manages the Beam Permit loops)

  - new VHDL (for monitoring part only)
  - Implementation synchronized with new CIBT (see next slide)

  - Upgrade of FESA class
  - New screen in Java application



New designs for BIS project (3/5)

- New CIBT

  (Test and monitor the remote User Interface units)

  - New PCB with VME-bus interface
  - new VHDL for managing new CIBF (see coming slide)

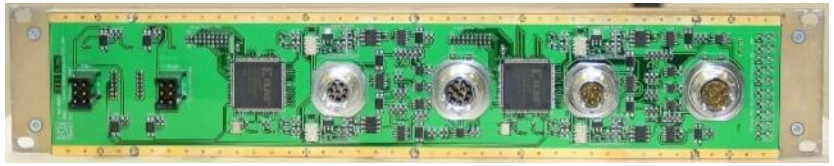
  - New FESA class
  - New screen in Java application

New designs for BIS project (4/5)

- CIBUR

  (Beam Interlock Interface unit installed in User System rack for distance length < 1.2km)

  - New design for a RadHard version of the CIBU
  - Replacement of obsolete components
  - Compatible with current version



New designs for BIS project (5/5)

- **CIBF upgrade**

(F.O variant of the Beam Interlock Interface unit for distance length **>** 1.2km)

CIBF (front view)

(rear view)

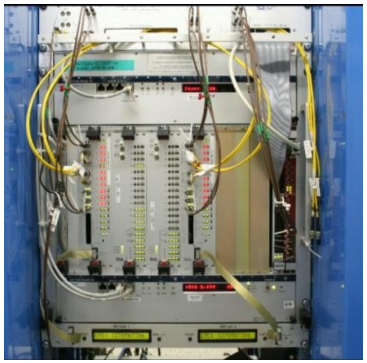
CIBL
(optical interface)

- *Unique optical card based on Laser transmitter*
- *Remote control and more monitoring info*
- *=> new VHDL code*
- *Same issues as for CIBU:*

  Radiation tolerance + Obsolescence of key components

Issues with new VME platform?

- New Operating system
  - *Linux (instead of LynxOS)*
- New VME-bus master card
  - *New device driver*
  - *FESA untouched?*
  - *New Timing cards?*
- New Crate
  - *Redundant Power-Supplies*
  - *CIBP Back-plane still compatible?*



BIC (front view)

(rear view)

CIBP (Back-Plane)

Wrap-up

- Lot of HW designs are scheduled for BIS & SMP project
- BIS is very stable and thanks to SMP V3, no urgency in term of their completion.
- Nevertheless, MI team stays vigilant for possible radiation issues and anticipate more robust solutions.
- Obsolescence of components is also taken into account and are included in new developments.

Fin

Thank you for your attention

New designs scheduling

	New/Upgrade	FESA class	Java Appl.	Scheduled	
CIST	new	new	new	during 2011	Installation expected on next Xmas Tech. Stop
CISV	Upg.	new	new	during 2011	" " " "
CIBV	Upg.	new	new	during 2011	" " " "
CIBM	Upg.	Upg.	Upg.	Not precisely defined	must be done by end of long shut-down
CIBT	new	new	new	" "	" " " "
CIBUR	new	n.a.	n.a.	" "	" " " "
CIBF	new	n.a.	n.a.	" "	" " " "

Concerning the FMCM interface:

- In the framework of the MUGEF system renovation, BE/CO has suggested to replace the current solution for interfacing the FMCM unit:
  - “low cost” solution called PICMG 1.3
  - => new wiring
  - = > new FESA class…

- Waiting for final decision…
  Help and support from BE/CO are expected.

RS422 link

I/O card named VIPC 626

embedded in:

BIS crate (LHC case) or Mugef crate (Transfer line)

Example of crate using PICMG 1.3 standard