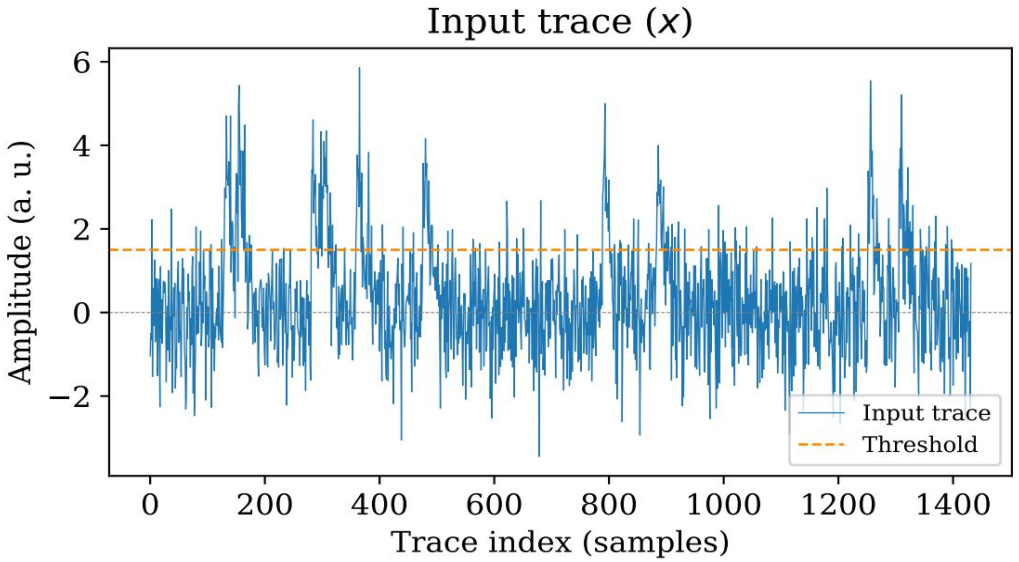
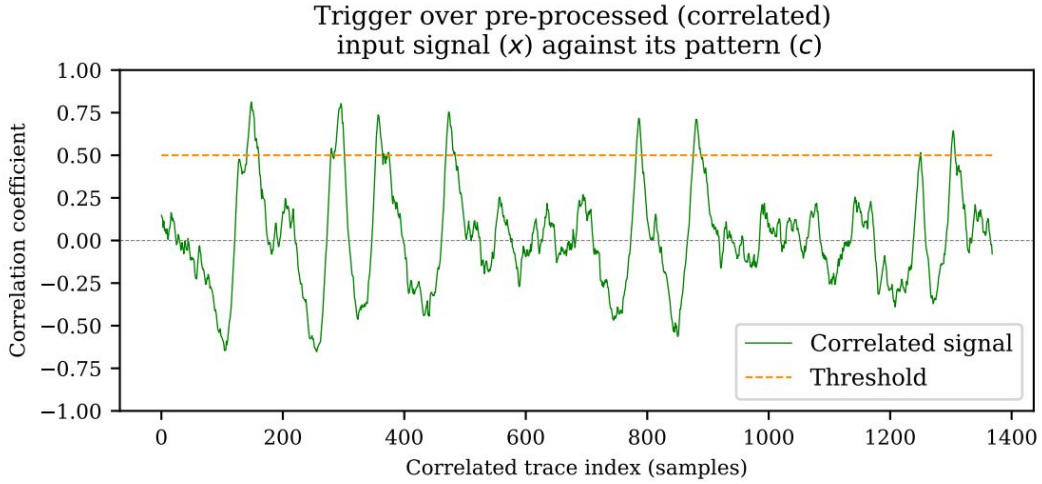
The Abdus Salam
International Centre
for Theoretical Physics

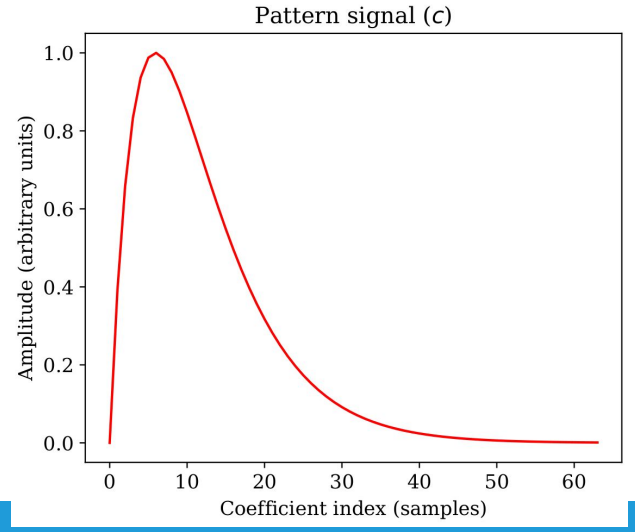
A simplified correlation index for fast real-time pulse shape recognition

MLAB - ICTP

Triggering over a correlated signal



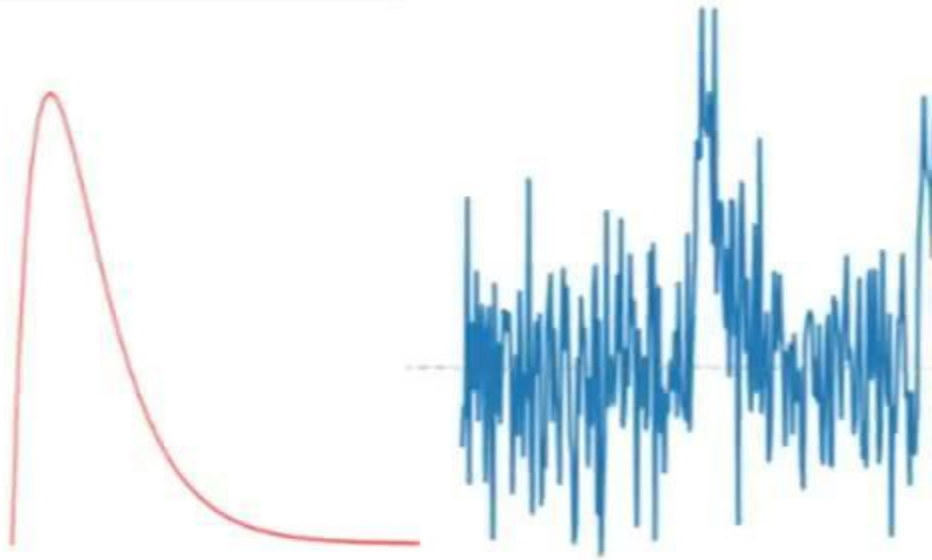




$$c_i = \frac{y_i - \bar{y}}{\sigma_y}$$

$$\rho_{xy} = \frac{1}{n}\sum_{i=0}^{n-1}\left(\frac{x_i - \bar{x}}{\sigma_x}\right)\left(\frac{y_i - \bar{y}}{\sigma_y}\right) = \frac{1}{n}\sum_{i=0}^{n-1} z_x \cdot z_y$$

IN



OUT

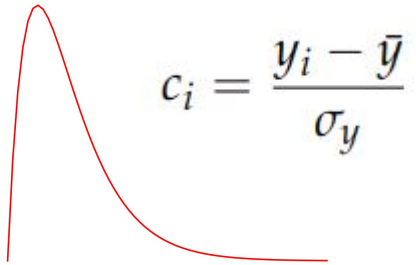
Correlating against a known pattern

Possible applications in this context

- Quality index factor for each detected pulse in DPP
- Increased SNR
  - However waveform is distorted
  - Latency is expected, but it's constant and measurable

Simplified Pearson-like correlation

- PCC -> Original Pearson correlation
- SPCC -> Simplified Pearson-like correlation



$$c_i = \frac{y_i - \bar{y}}{\sigma_y}$$

$$PCC = \rho = \rho_{x\hat{c}} = \sum_{i=0}^{n-1} z_x \cdot \hat{c}_i$$

$$z_x = \left(\frac{x_i - \bar{x}}{\sigma_x} \right)$$

$$\sigma_x = \sqrt{\frac{1}{n} \sum_{i=0}^{n-1} (x_i - \bar{x})^2}$$

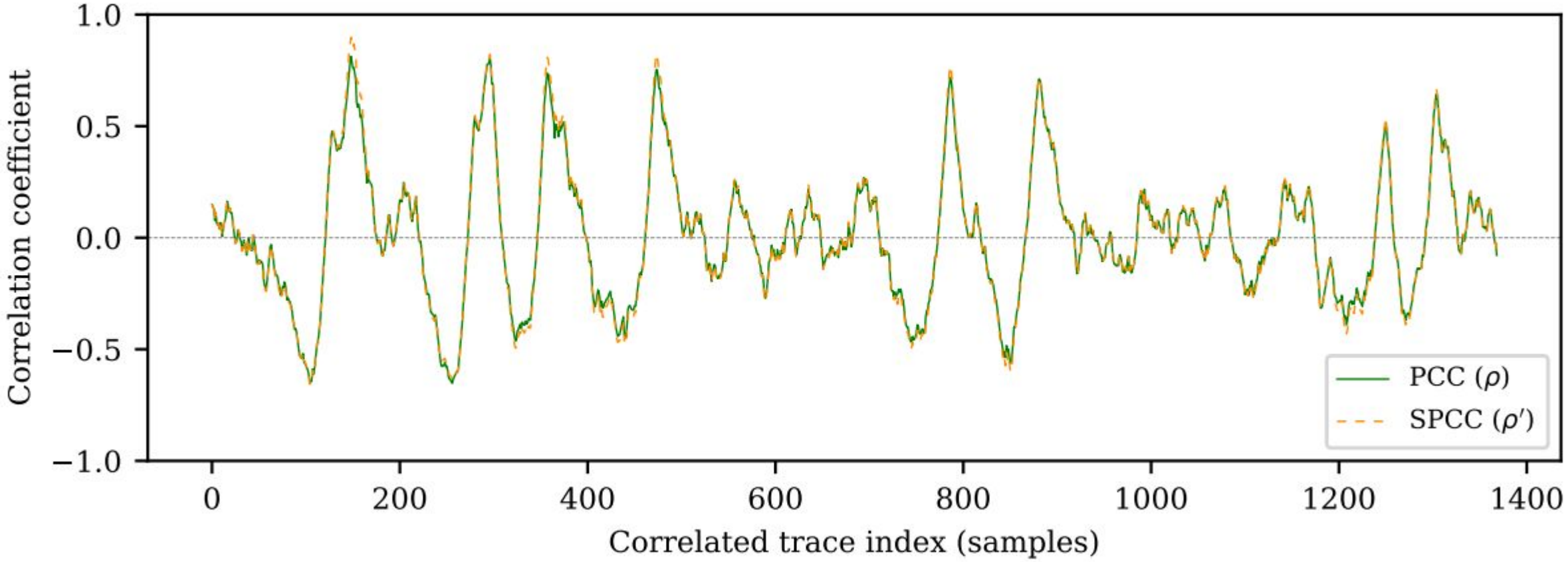
$$SPCC = \rho' = \rho_{x\hat{c}'} = \sum_{i=0}^{n-1} z'_x \cdot \hat{c}'_i$$

$$z'_x = \frac{x_i - \bar{x}}{D_x}$$

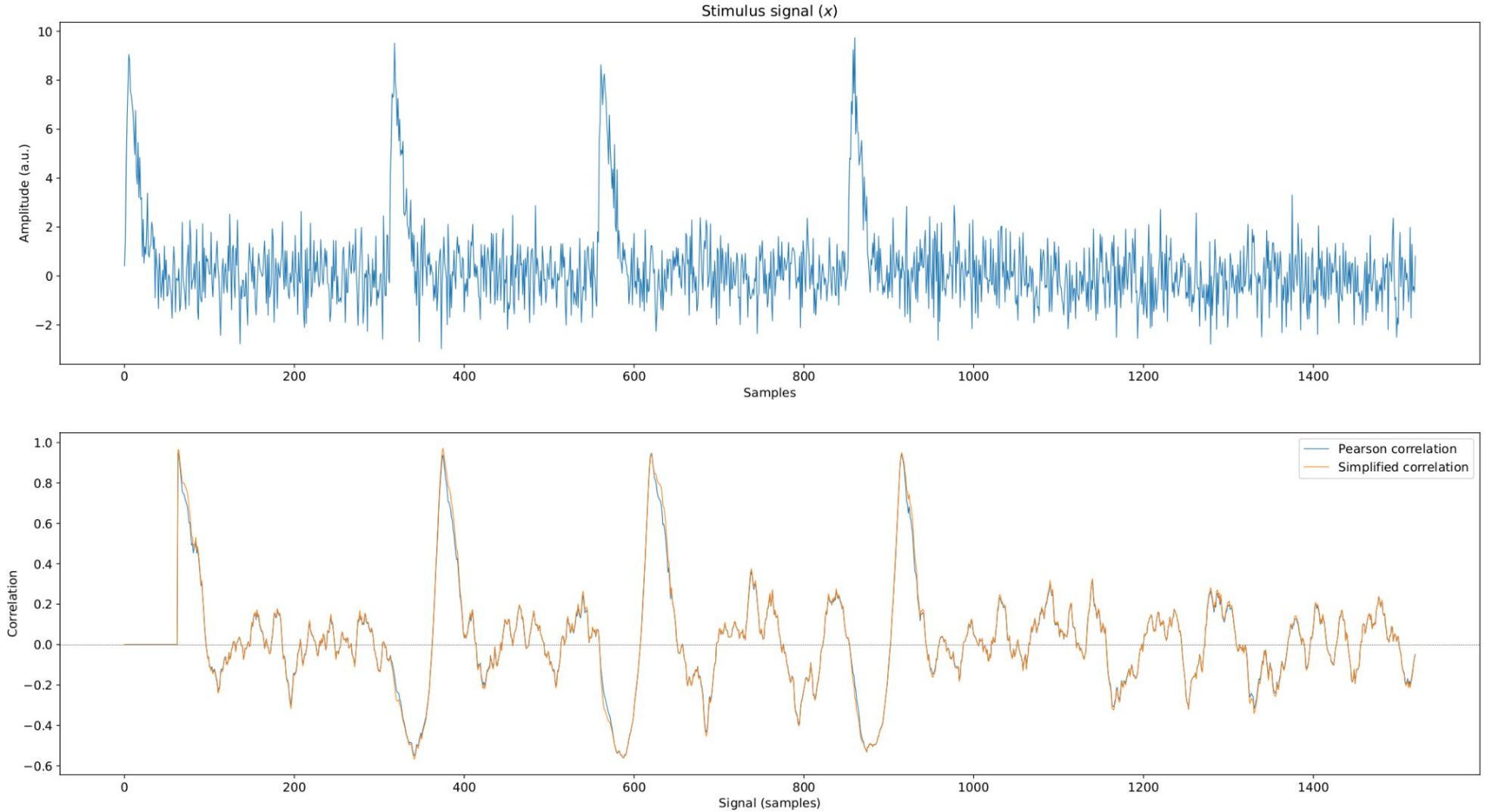
$$D_x = \frac{1}{n} \sum_{i=0}^{n-1} |x_i - \bar{x}|$$

Simplified Pearson-like simulations

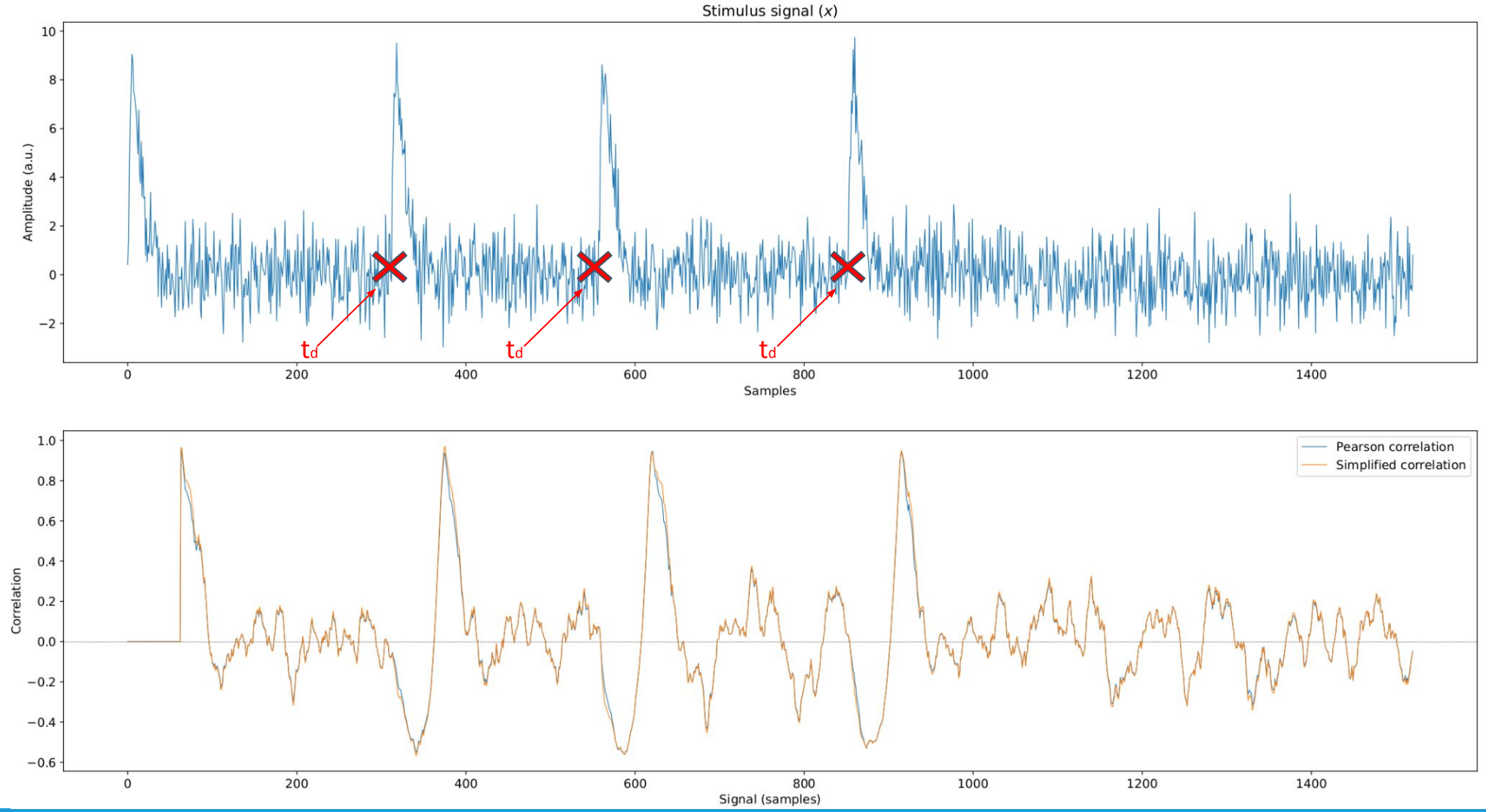
PCC vs SPCC correlations comparison



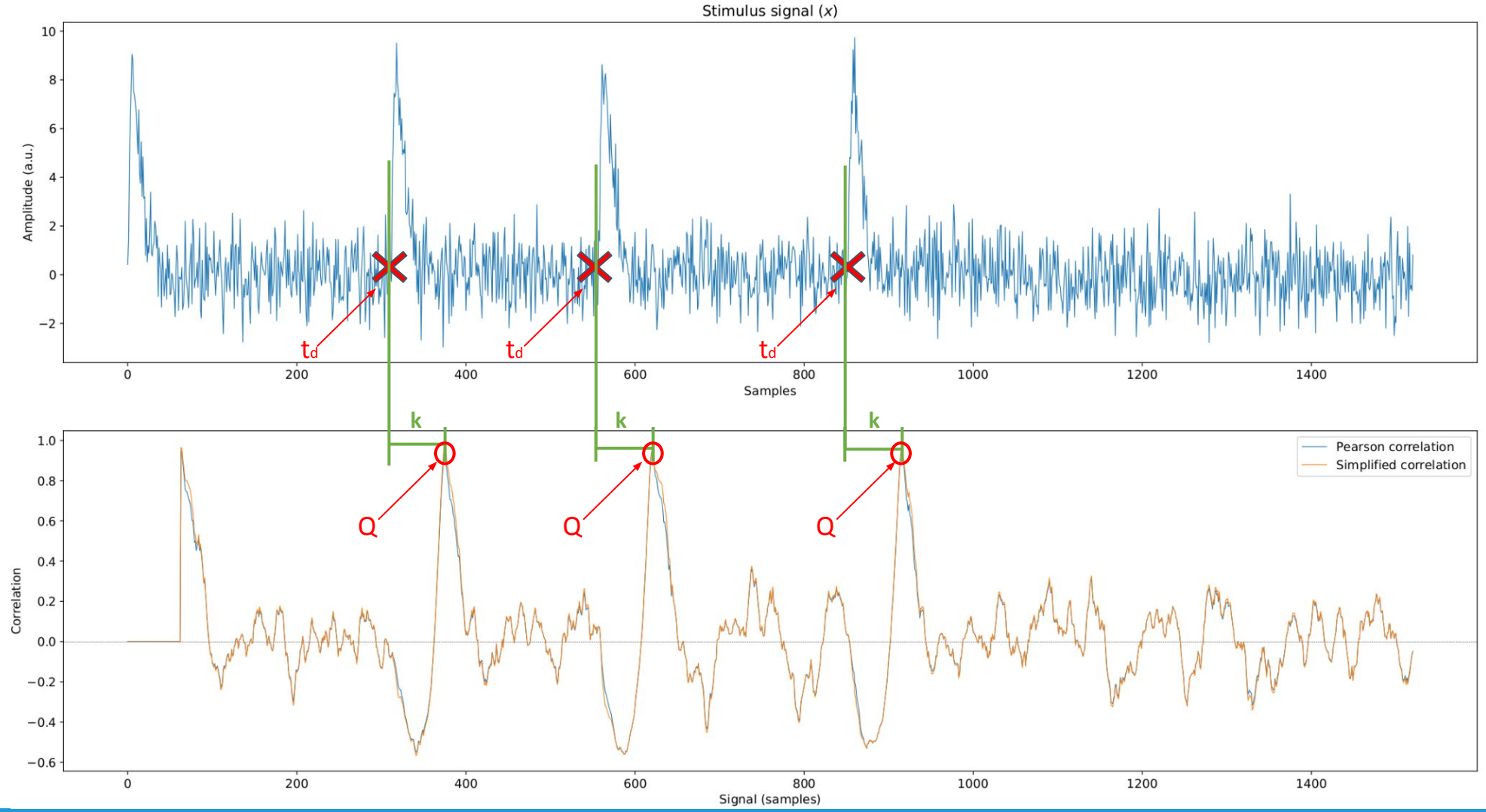
Quality index from single sample after "k" samples from arrival time



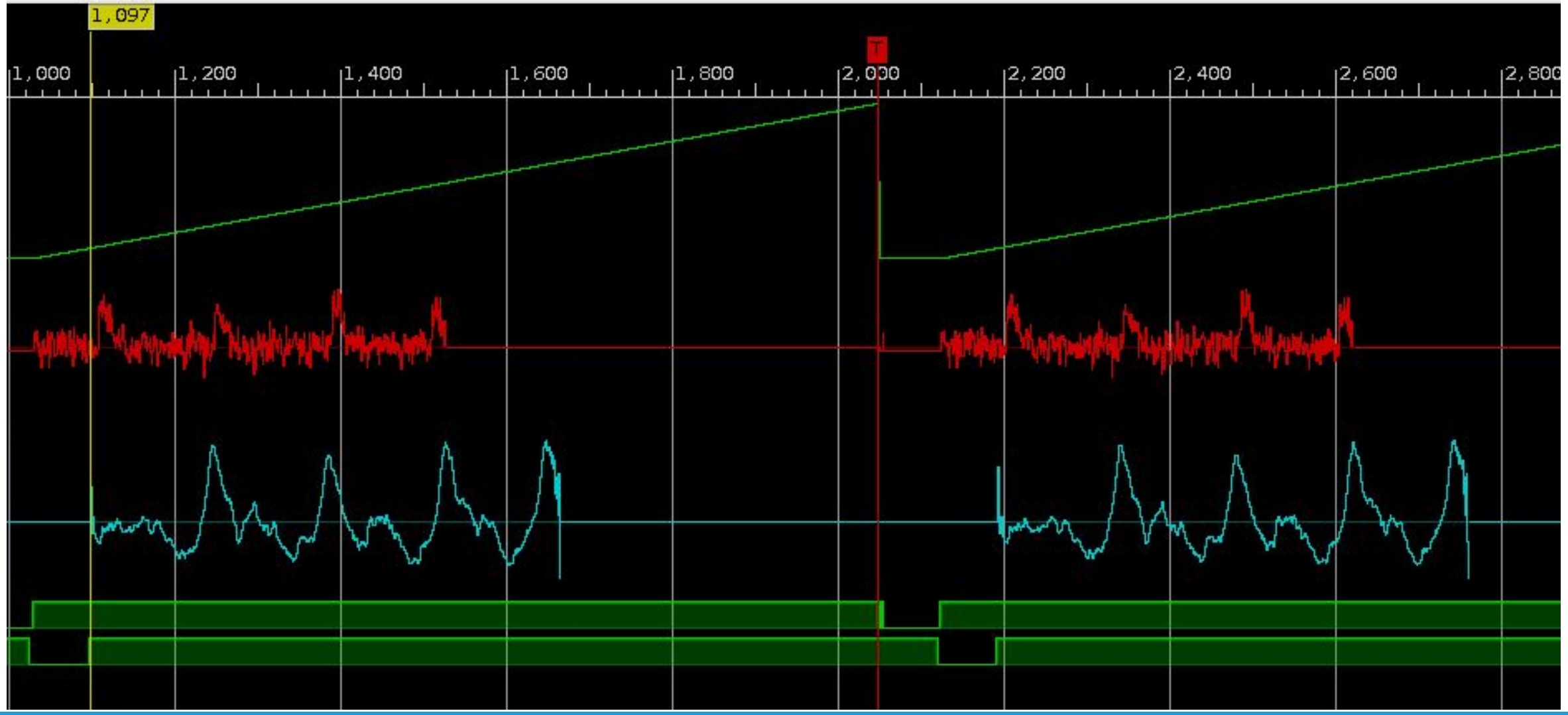
Quality index from single sample after "k" samples from arrival time



Quality index from single sample after "k" samples from arrival time



IP core (HLS) implementation test with ILA



Resource and performance comparison between both IP Cores

- Results for HLS implementation
  - Area -> Default settings
  - Performance -> Pipeline and unrolling
- Further version with VHDL

	Area		Performance	
	PCC	SPCC	PCC	SPCC
Resources utilization				
LUT (53200)	11.21% (5962)	15.15% (8058)	40.13% (21349)	42.70% (22718)
Registers (106400)	4.71% (5016)	4.74% (5040)	20.23% (21524)	22.06% (23468)
Block RAM (140)	0.00% (0)	0.00% (0)	0.00% (0)	0.00% (0)
DSP Slices (220)	29.55% (65)	0.45% (1)	54.55% (120)	24.09% (53)
Timing results				
Max. frequency (MHz)	119.3	122.4	137.8	143.4
Latency (clock cycles)	2.23×10^6	2.23×10^6	1.1×10^3	1.1×10^3
Estimated power consumption @ 100 MHz				
Average power (mW)	190	118	796	705

Backup slides

IP core (HLS) implementation outputs. Comparison with simulations

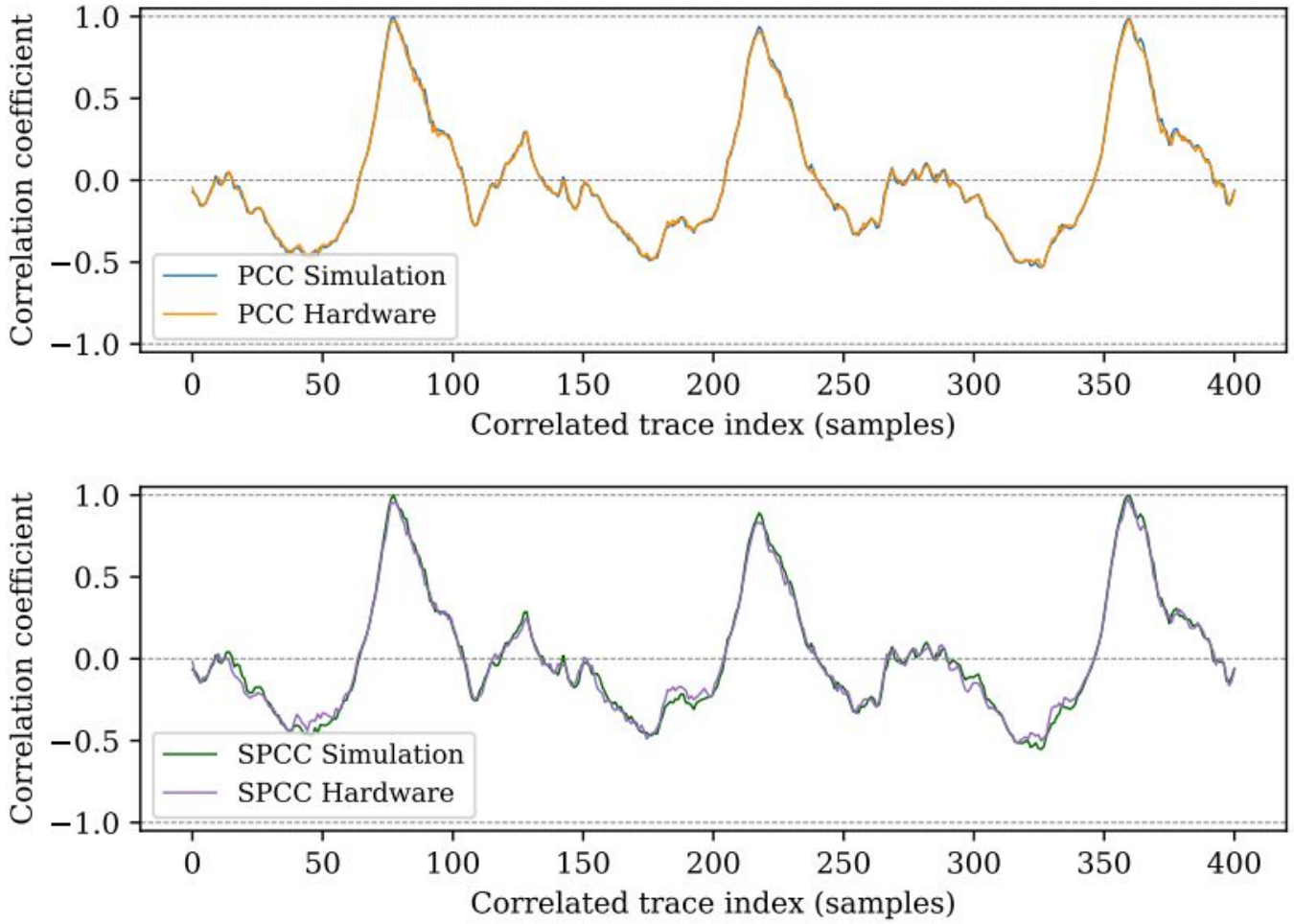
Results:

- Quantization: 14 bits (fixed-point)
- Throughput > 100 MHz
- Latency or Area optimizations tested

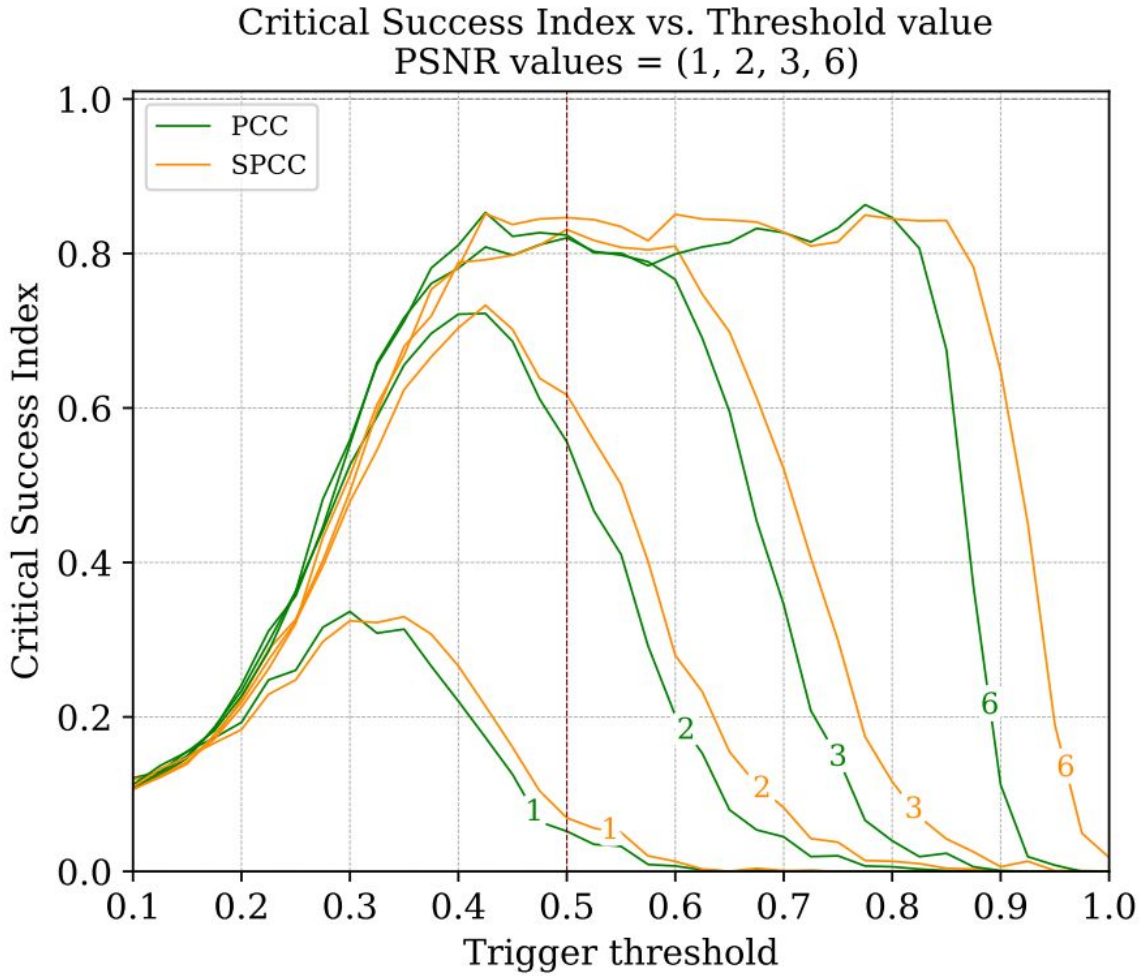
Normalized mean average error (IPs vs simulation):

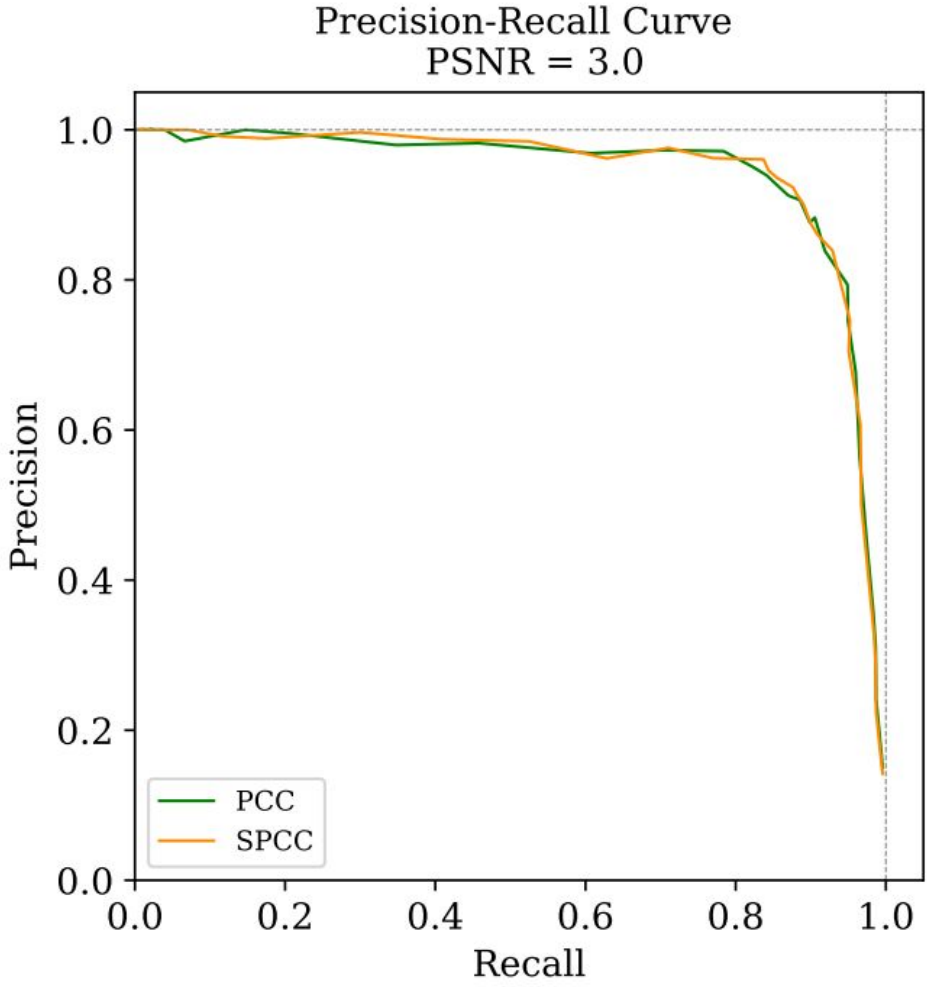
Pearson: 1.07%

Optimized: 1.98%



Similarity between original and simplified algorithm (simulations)





Conclusions:

- Simulations demonstrated the improved pattern recognition capabilities when pre-processing a raw stream (either PCC or SPCC)
- Simplified correlation (SPCC) performs very similarly to Pearson Correlation (PCC) in terms of recognition performance
- SPCC reduces dramatically DSP usage in both optimization FPGA implementations (area vs latency)

Further work:

- Develop and test a VHDL core (instead of HLS) optimized for both: latency and area, simultaneously
- Test a classification system based on the HDL core, capable to distinguish multiple pulse types