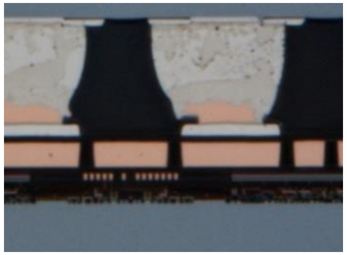
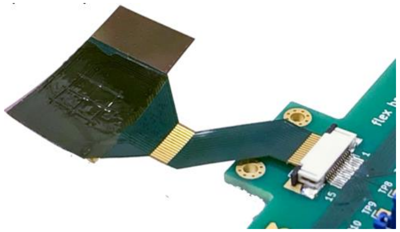
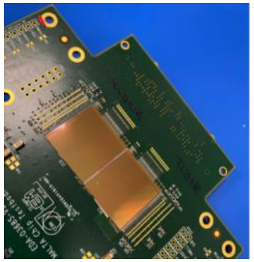
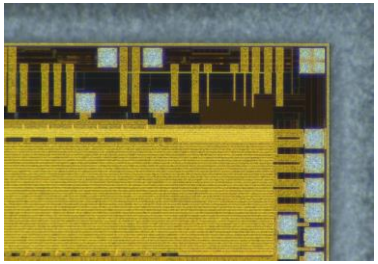
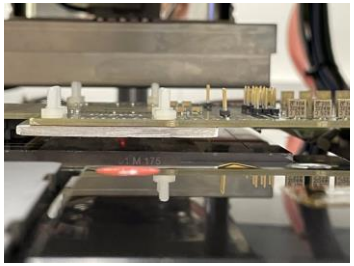
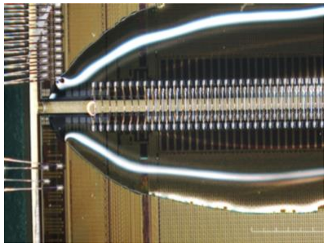
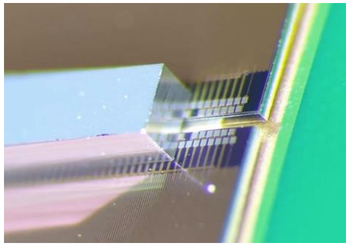
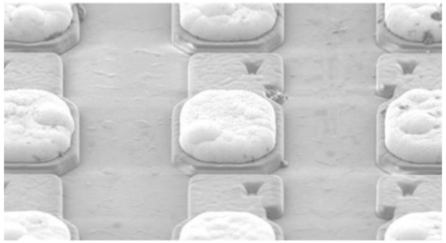
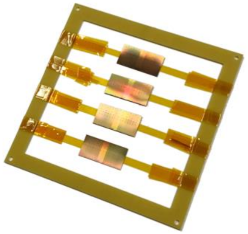
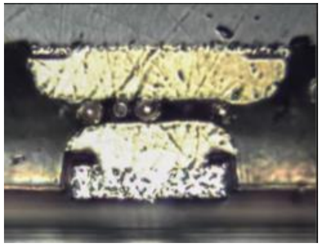






WP 1.3 – Module Development Introduction

Petra Riedler, Dominik Dannheim

WP 1.3 Team

- The WP 1.3 team is very diverse with contributions from **CERN staff, CERN users, students and fellows** working on silicon module development.
- Hiring of 2 doctoral students (with 50% funding), 2 fellows and 1 TECH on WP 1.3 funds:

Milou van Rijnbach
(DOCT WP 1.3/ATLAS, Oct. 2020)

Florian Dachs
(FELL WP 1.3, Oct. 2020)

Julian Weick
(DOCT WP 1.3/DT, Apr. 2021)

Peter Svihra
(FELL WP 1.3, Oct. 2021)

Janis Schmidt
(TECH WP1.3/AIDAinnova, Jan. 2022)

Former fellows and students:

- Mateus Vicente Barreto Pinto (FELL, now at University of Geneva) continues to be very active in WP 1.3
- Roberto Cardella (PJAS, now University of Geneva)
- Morag Williams (DOCT, now ESRF)

Mateus Vicente
(Univ. Geneva)

WP 1.3 Meetings & Outreach

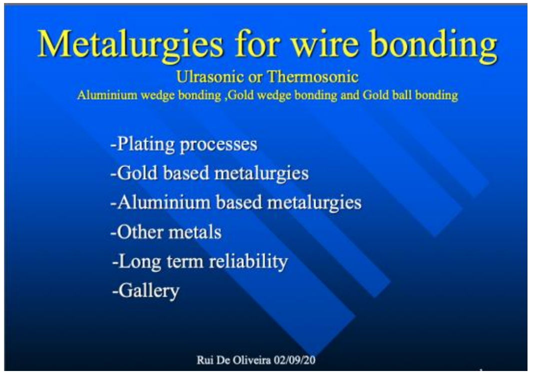
EP R&D

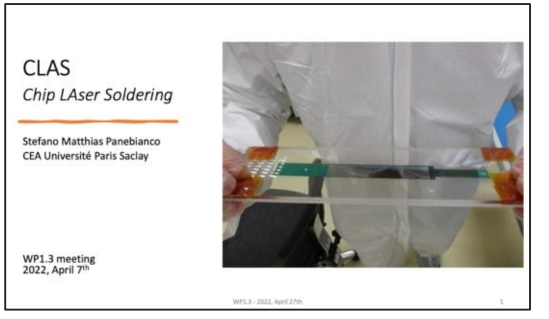
- WP 1.3 holds **monthly meetings (https://indico.cern.ch/category/11714/)** which provide updates on the different activities as well as a platform for exchange and discussion.

- We invite **experts for focus talks** on specific technologies, e.g. Ni/Au plating (Rui de Oliveira), encapsulation irradiation studies (Susanne Kuehn) to **kick-off developments and provide a summary of present experience.**

- We have **talks on specific developments for experiment upgrades** (e.g. ALICE ITS3 Chipflex by Magnus Mager, Solder interconnection studies for LHCb UT by Stefano Panebianco) and **collaborate closely with the experts in these teams.**

- **Presentations at conferences and workshops** to report on development and progress (e.g. in 2022 contributions at Trento workshop, VCI, Elba, IWORID, TWEPP, …)





WP 1.3 Activities

WP 1.3 focusses on the study and development of new modules for hybrid and CMOS pixel detectors:

- Using existing chips, e.g. ALPIDE, MALTA1, MALTA 2, Timepix3 or CLICpix2, ALTIROC and sensors → **no dedicated chip/sensor development, use what is available and adapt to build flexible concepts**
- Collaborating with the other work packages mainly on silicon detectors → **exchange and collaborate** (e.g. feed-back on chip pads, RDL, tests, interconnection for novel chip/sensors)
- Closely working with industrial partners to develop and test technologies & processes → develop and tune processes and products **(e.g. DISCO, Dexerials, Conpart, FBK, IZM , Optim or PacTech, HiTech)**
- Closely collaborating with services at CERN → **develop procedures and processes, analyze material** (e.g. Micropattern lab EP-DT-EF, Bondlab, QARTlab, BE-CEM-EPR or EN-MME).
- **Working closely with institutes and collaborations in the field to develop concepts and validate them –** e.g. University of Geneva, LPNHE Paris, University of Oslo, AIDAinnova

In line with ECFA roadmap topics in several areas: e.g. 3D integration (module level), compact module concepts, BEOL layer deposition (RDL), interconnection (chip2chip, module level)

R&D Plan and Deliverables

EP R&D

2020	2021	2022	2023	2024

Thinning & Dicing

Planned: 36 M, completed, standard recipe using stealth dicing for various thicknesses, used by different projects, equipment for handling set up (e.g. see Nov. '21 R&D day presentation)

Redistribution Layer

Planned: 18 M, delayed & onoging, (see slides by J. Weick)

Test of 2.5 D integrated modules

Planned: 40 M, ongoing, flip chip/ interconnection and RDL work ongoing to build modules (see slides by P. Svihra, F. Dachs, M. van Rijnbach)

Irradiation and testing of modules

Planned: 50 M, ongoing, demo modules and assemblies being tested, interconnect test structure irradiation planned next year followed by modules (see slides by P. Svihra, F. Dachs, M. van Rijnbach)

Module with photonic chip and electrical driver/receiver

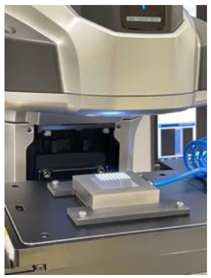
Planned: 56 M, ongoing, conceptual studies starting (see slides by J. Weick)

QA procedures for ultra-thin modules

Planned: 60 M, ongoing, equipment (metrology, release chuck, thickness tool) installed and operational, used by several projects, further equipment as defined in original plan under study, detailed studies and material analysis to deliver reproducability

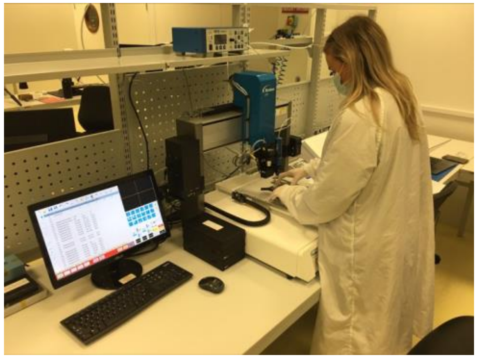
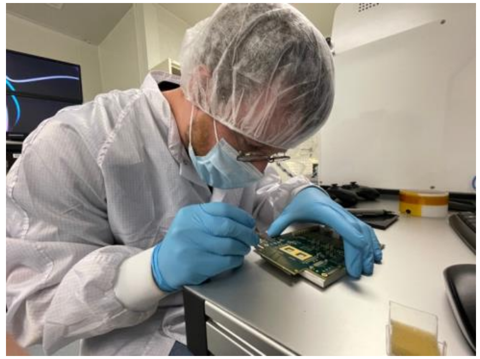
WP 1.3 Infrastructure & Investments

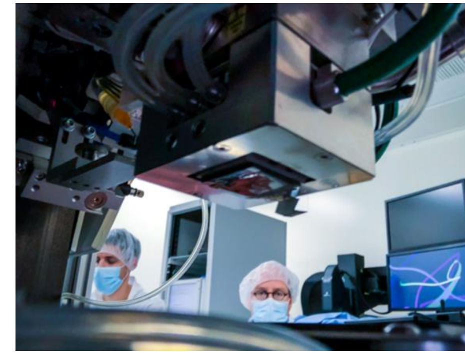
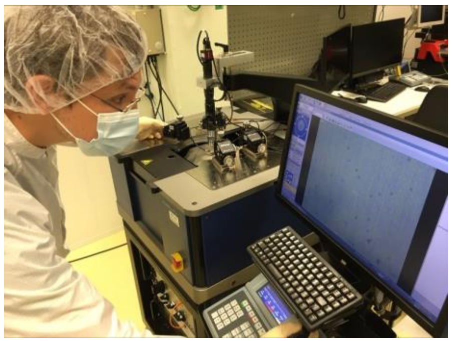
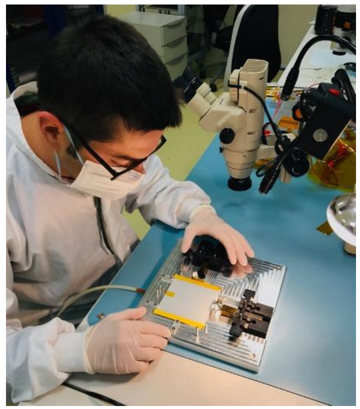
- **Dedicated area in the DSF cleanroom** (and SAS) for common equipment.
- All **equipment is listed on the WP 1.3 EP R&D web-page** with instructions how to book time and access. A contact person for each equipment helps users with setting up and using the tools.
- Cost sharing with projects/experiments optimising synergies and common needs.



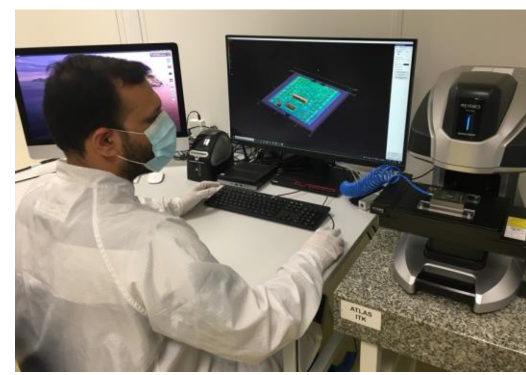
Item	Date	Comment
Plasma cleaner and gases	2021	Cost sharing with Bondlab
Flip chip bonder upgrade	2021	Bonding tool for modules and maintenance
Diamond scriber	2021	Cost sharing with QARTlab
Keyance metrology tool	2020	Cost sharing with ATLAS ITk
Onosoki thickness tool	2020	
Small pad ENIG production line	2022	
Release chuck and thin wafer upgrade	2020 and 2022	
Consumables (gel-paks, wafer boxes, etc.)	Cont'd	
Mini X-ray	2022	Under evaluation
Table top AFM	2023	Under evaluation
Automated inspection system	2024	Under evaluation







Small pitch interconnect
Peter Švihra

Single die ENIG process
Janis Schmidt

Module interconnection studies
Florian Dachs

Module tests
Milou van Rijnbach and Florian Dachs

Flex development and module concepts
Julian Weick

Small pitch interconnect

Peter Švihra

Outline

- Single-die bump-bonding
  - Laboratory and beam-test results
- ACF interconnect
  - Daisy chain test structures
- Summary and outlook

Single-die small pitch bonding

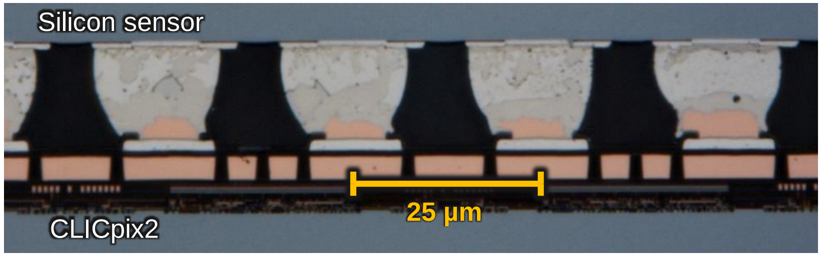
- Targeting hybrid detectors
  - Standard interconnect requires full wafer processing
  - Not suited for R&D of new devices or multi project wafers
- Development of single-die process utilising already existing devices

CLICpix2
- 25 µm pixel pitch
- 128 x 128 pixels
- 3.2 x 3.2 mm

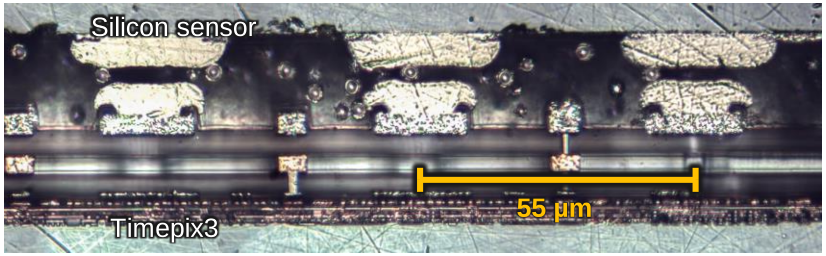
Timepix3
- 256x256 pixels
- 55 µm pixel pitch
- 14 x 14 mm

- Already caught interest of other teams (PicoPix, TimeSpot)

Single-die small pitch bump-bonding



Anisotropic Conductive Film (ACF)



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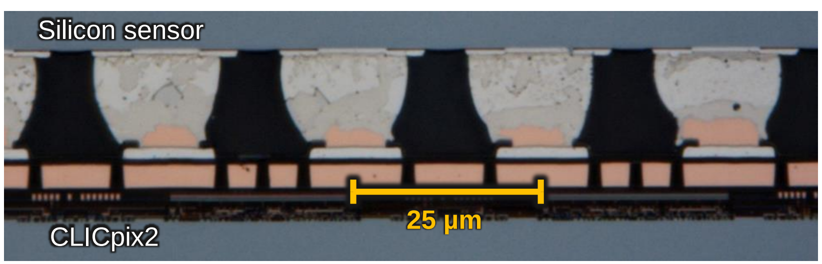

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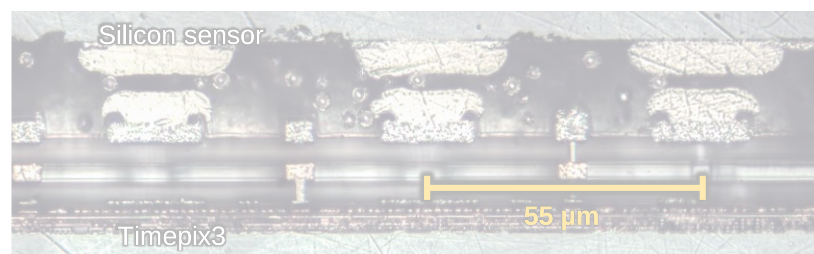
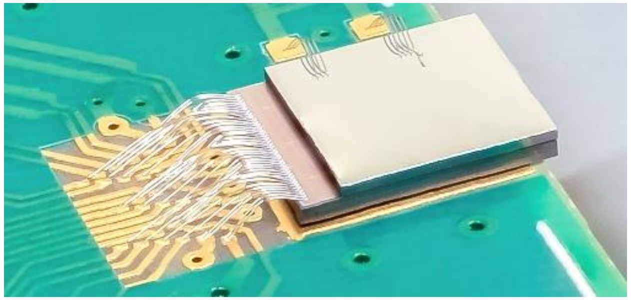


Bump-bonding R&D for single dies

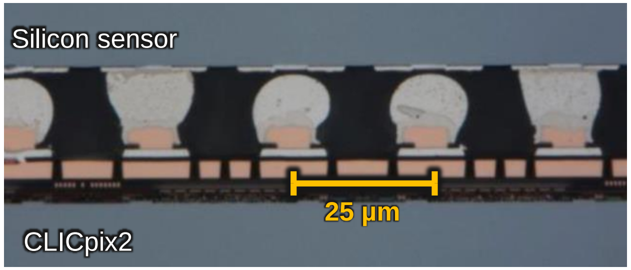
- Bump-bonding of small pitch detectors is still very challenging
  - Good yields for pixel pitch **> 50 µm**, requires full wafer processing

- R&D with IZM has developed single die bonding process for **25 µm pixel pitch**
  - Preparation of carrier wafers with mask alignment marks and bond layer
  - Bond each single ASIC die on an individual carrier wafer
  - Bump deposition: sputtering of plating base, resist lithography, Cu+SnAg-galvanic, resist removal and etching of plating base outside bumps, reflow of bumps
  - Removal of ASICs from carrier wafer
  - UBM deposition on sensor wafers (at Advacam / IZM)
  - Singularisation of sensors (at Advacam / IZM)
  - Flip-chip of ASICs and sensors
  - X-ray measurements for quality control.

CLICpix2 ASIC bump-bonded to an active edge silicon sensor



Cross-section of some failed connections



First (feasibility) stage of the process characterised in the thesis of Morag Williams

Fraunhofer IZM

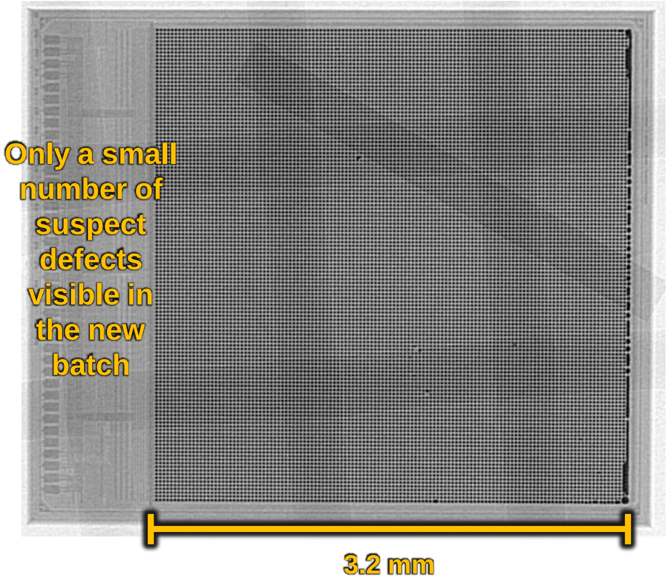
Bump-bonding R&D for single dies

- The process has been optimised after the first (feasibility) stage

- Recently a new batch of CLICpix2 and FBK active edge sensor (from AIDA2020) assemblies bonded at IZM
  - Different guard-ring configurations
  - **50 µm**, **100 µm** and **130 µm** sensor thickness

- How to characterise interconnect quality?

X-ray scan of bonded CLICpix2, 973-3-A3



Bump-bonding R&D for single dies

EP R&D

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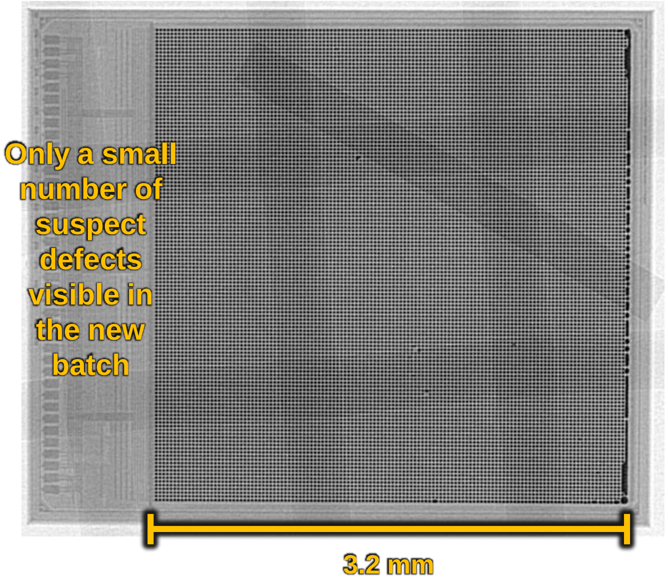


Characterisation
- Electrical characterisation
  - Voltage – current (IV)
  - Voltage – capacitance (CV)

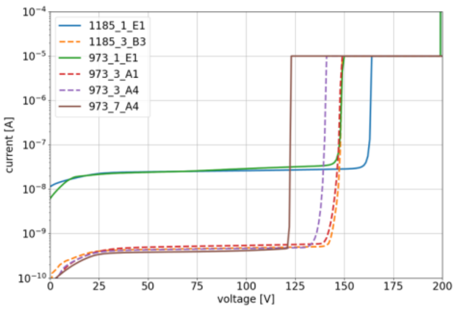
Electronic response
- ASIC testpulse
- Radioactive source measurement
- Interconnect yield

Beam-test
- Hit collection efficiency
  - Voltage/threshold dependency
  - Interconnect yield
- Timing performance

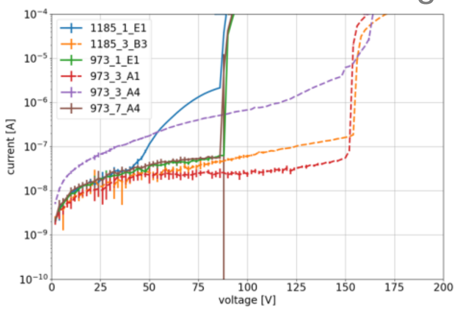
Lab tests

Electrical characterisation

IV curves at FBK



IV curves after bonding



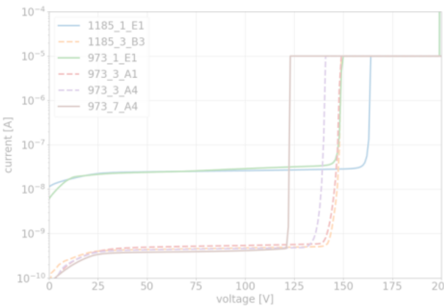
- Effect of different guard-ring layouts visible
  - Floating GR leads to highest breakdown

Wafer	Device	Sensor Thickness	Guard ring	Breakdown voltage [V]
973	1-E1 / 7-A4 3-A1 / 3-A4	50 µm	no float	-91 / -91 -160 / -161
1185	1-E1 / 3-B3	100 µm	no / float	-88 / -170
3826	4-B4 / 7-A5	130 µm	no	-85 / -85

Lab tests

Electrical characterisation

IV curves at FBK



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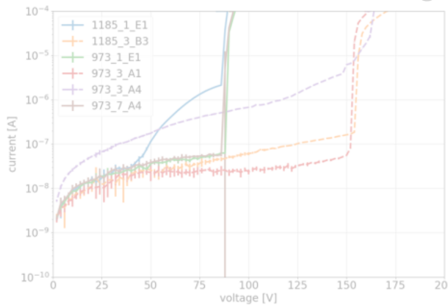

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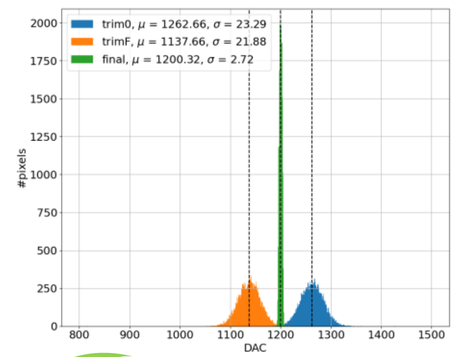
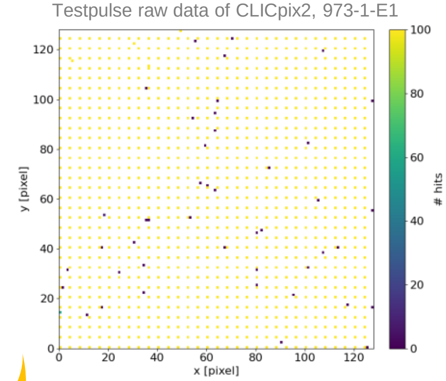
Electronic response

Pixel equalisation of CLICpix2, 973-1-E1



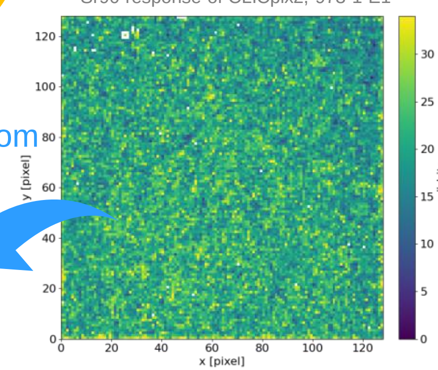
Testpulse raw data of CLICpix2, 973-1-E1



always noisy

linked testpulse response to neighbours

Sr90 response of CLICpix2, 973-1-E1



no hits from Sr90

Wafer	Device	Sensor Thickness	Guard ring	Breakdown voltage [V]	# of px masked	# of px with shorts	# of px w/o connection
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Lab tests

Electrical characterisation

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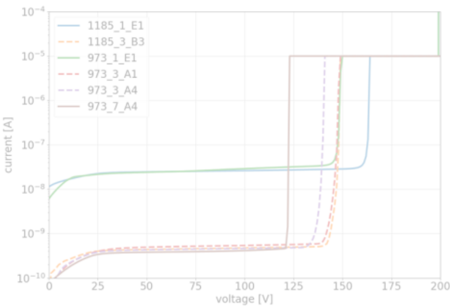

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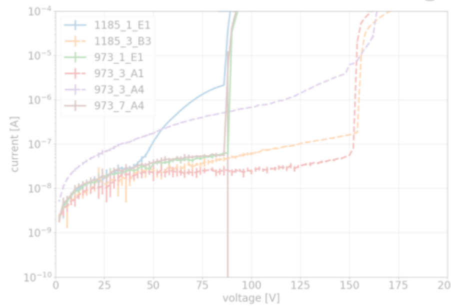

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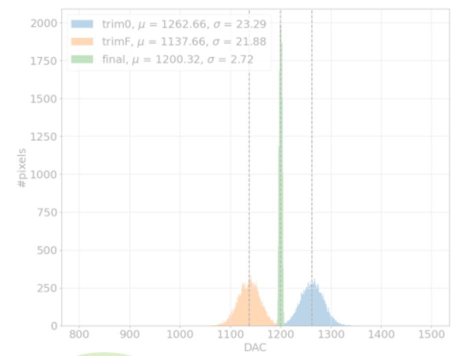

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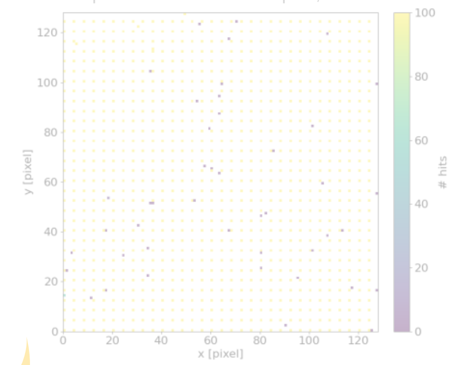

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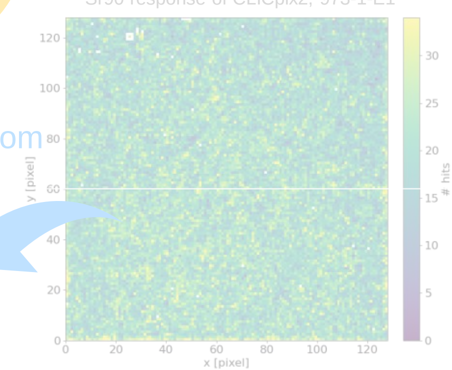

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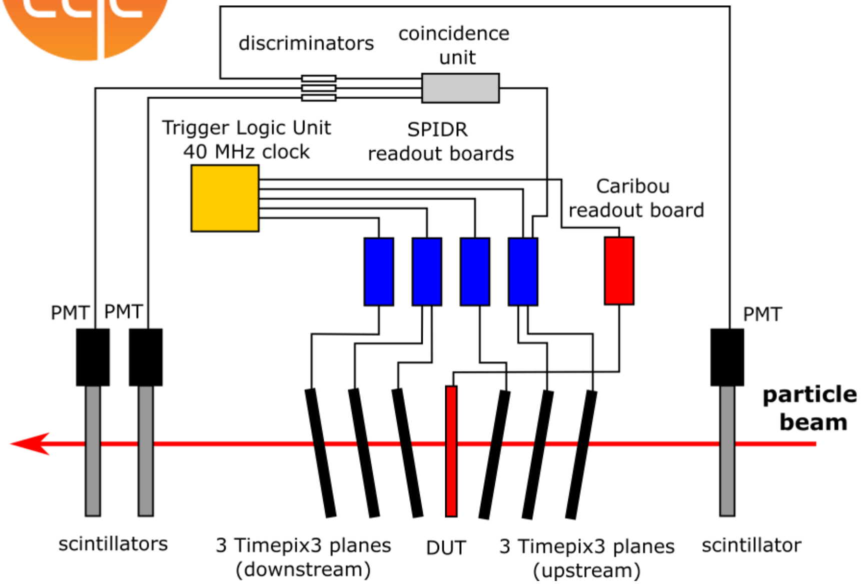
> 99.9% interconnect yield (total 16384 pixels)

Beam-test

CLICdp Timepix3 telescope



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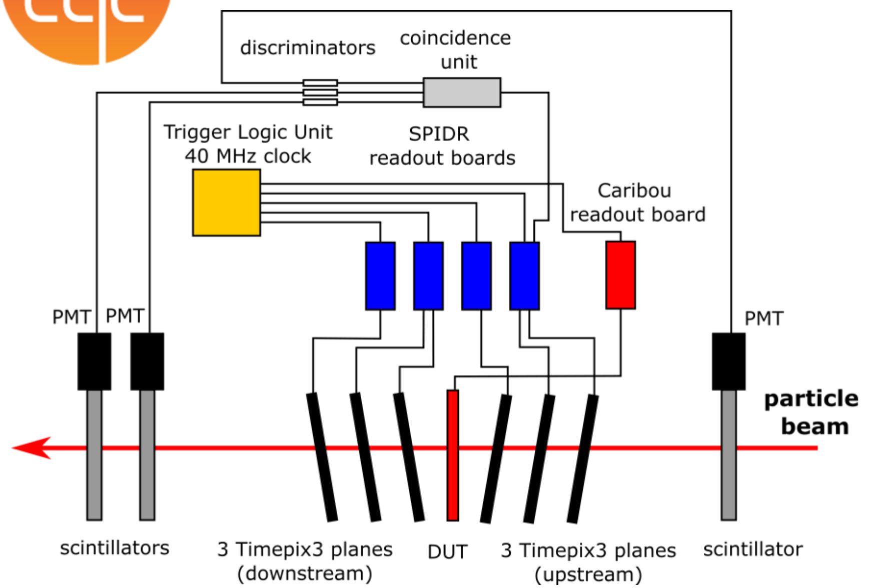
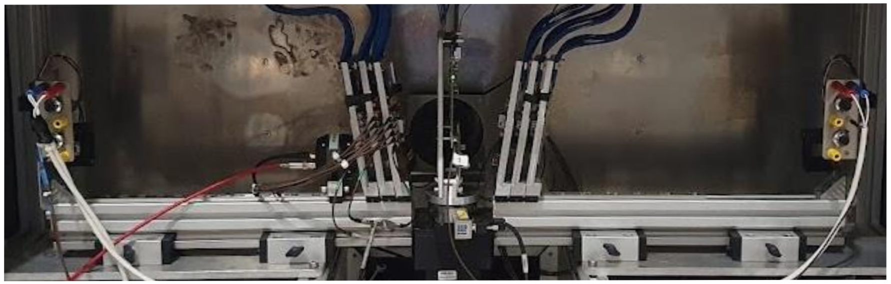
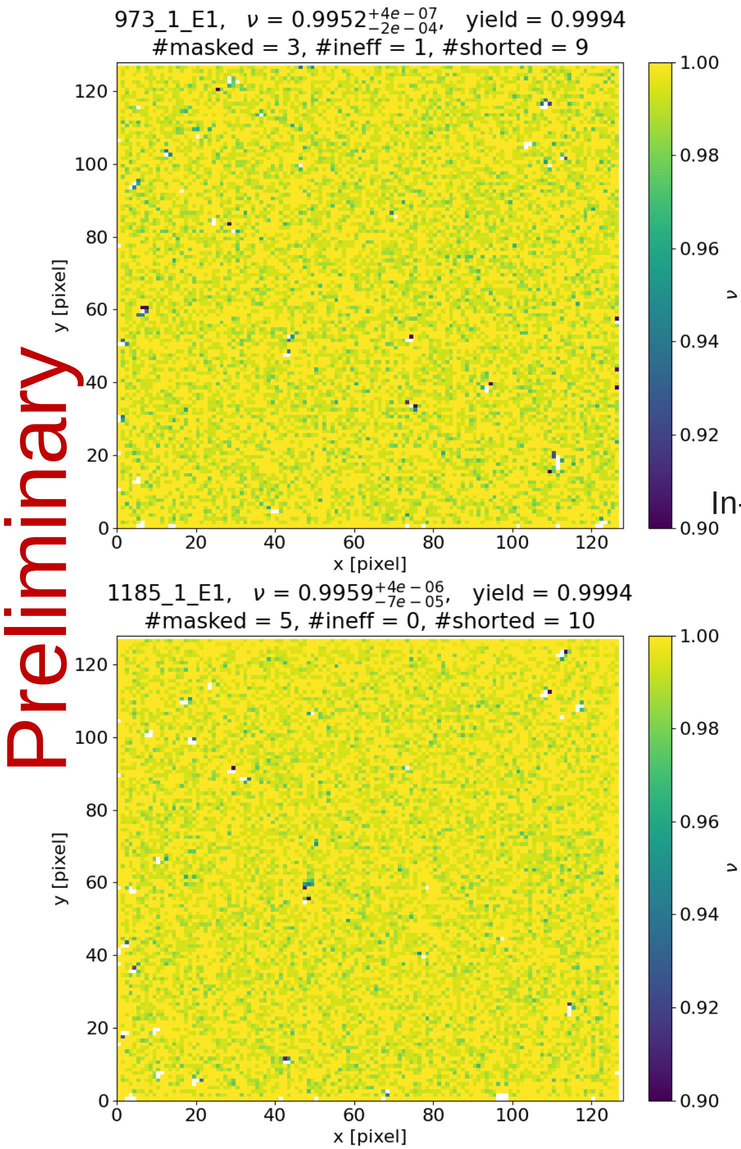




- Track intersects can validate interconnect yield



50 µm sensor thickness

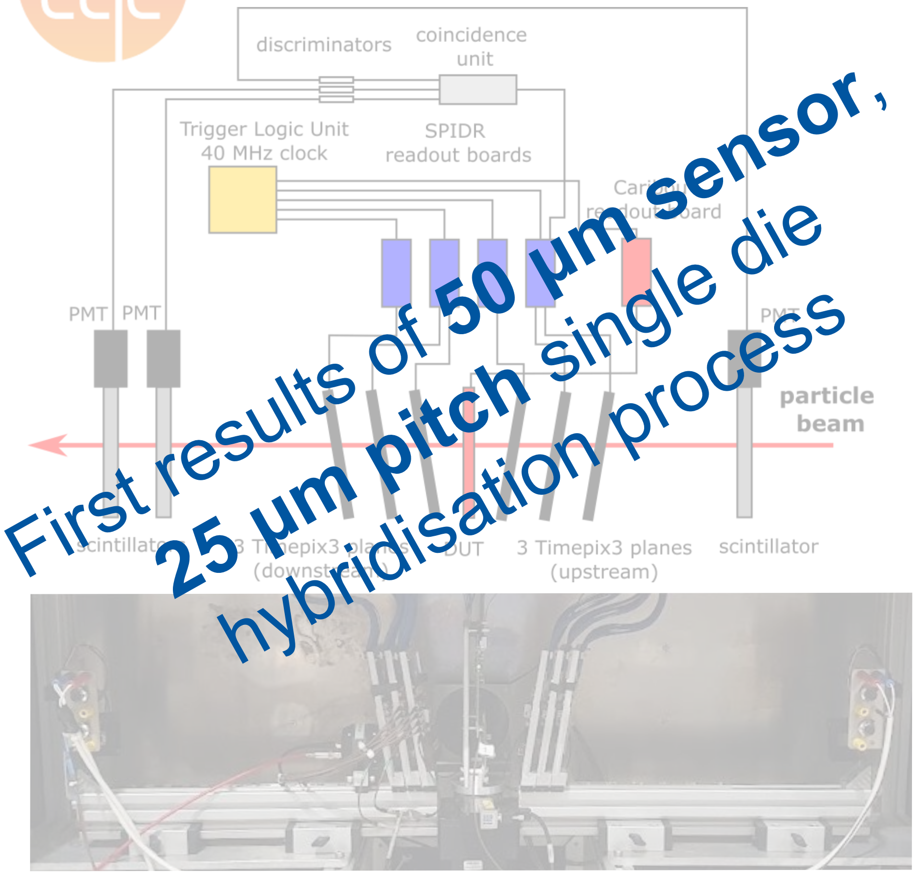
In-pixel efficiency, yield results match the lab tests

100 µm sensor thickness

Beam-test

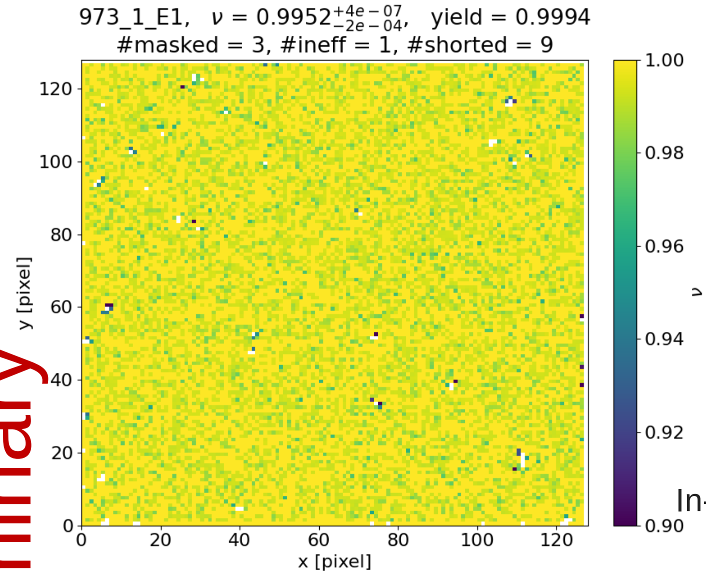
- Track intersects can validate interconnect yield

CLICdp Timepix3 telescope



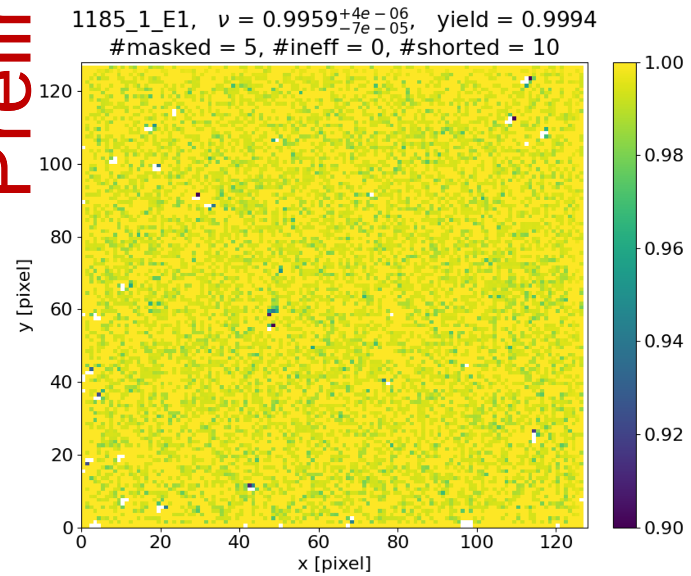
First results of **50 µm sensor**, **25 µm pitch** single die hybridisation process

Preliminary



50 µm sensor thickness

In-pixel efficiency, yield results match the lab tests



100 µm sensor thickness

Single-die small pitch bonding

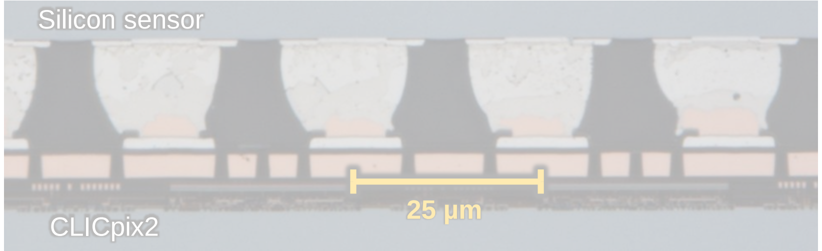
- Targeting hybrid detectors
  - Standard interconnect requires full wafer processing
  - Not suited for R&D of new devices or multi project wafers
- Development of single-die process utilising already existing devices

CLICpix2
- 25 µm pixel pitch
- 128 x 128 pixels
- 3.2 x 3.2 mm

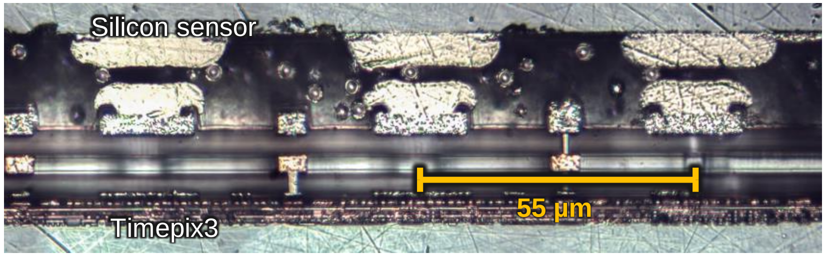
Timepix3
- 256x256 pixels
- 55 µm pixel pitch
- 14 x 14 mm

- Already caught interest of other teams (PicoPix, TimeSpot)

Single-die small pitch bump-bonding



Anisotropic Conductive Film (ACF)

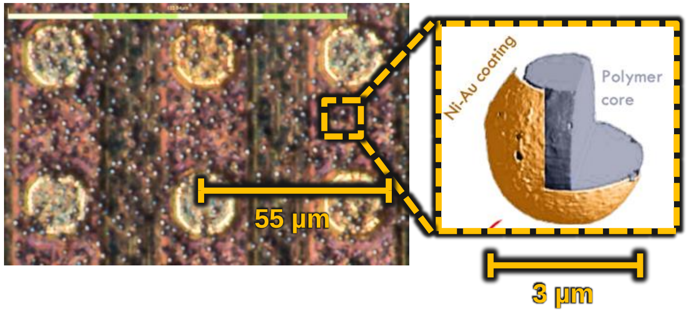


ACF hybridisation workflow

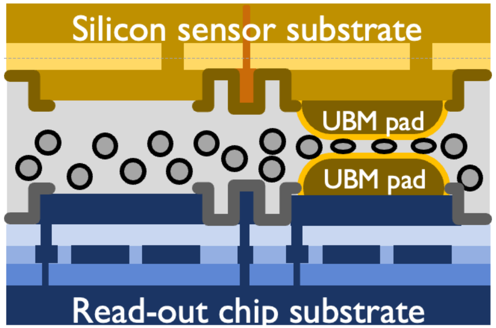
- Anisotropic Conductive Film (ACF)
  - Epoxy film with small (3µm) conductive particles
    - Widely used in industry (chip-on-flex, display manufacture, …)
  - Alternative in-house process compared to standard bump-bonding, needs R&D to adapt to pixel detectors

- Under Bump Metallisation (UBM) required
  - Electroless Nickel (Electroless Palladium) Immersion Gold – EN(EP)IG
    - In-house ENIG deposition for single dies under development @CERN

Timepix3 pixel matrix with ACF



Unplated (left) *vs* Plated (right)



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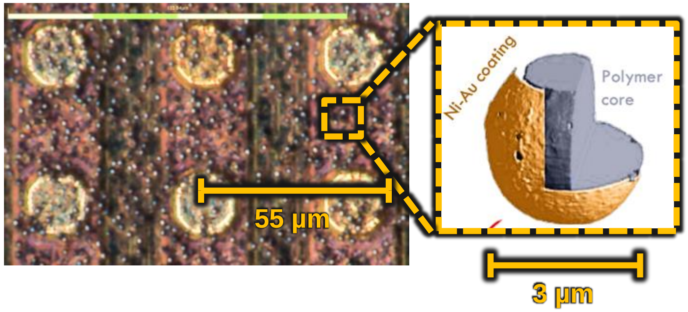

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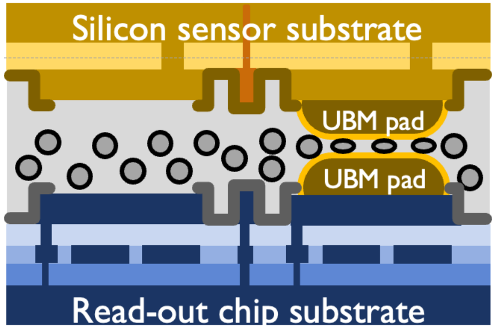

Preparation
- Sensor/ASIC/test structure procurement
- ACF material procurement

UBM
- ENIG
- Visual inspection

ACF
- Lamination
- Flip-chip bonding

Testing
- Cross-sections
- Electrical/mechanical tests
- Test-beam and source measurements

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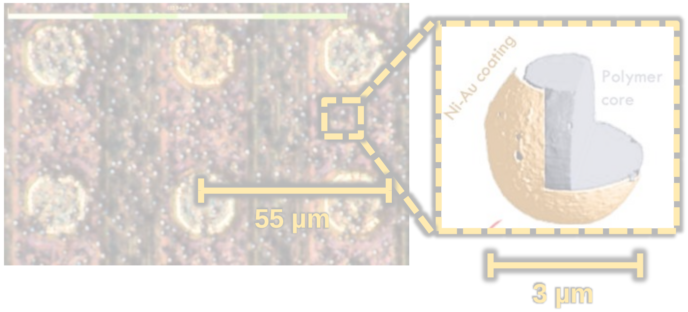

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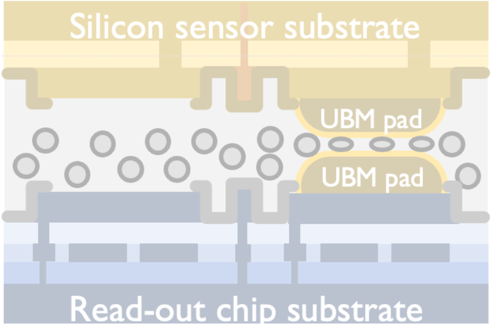

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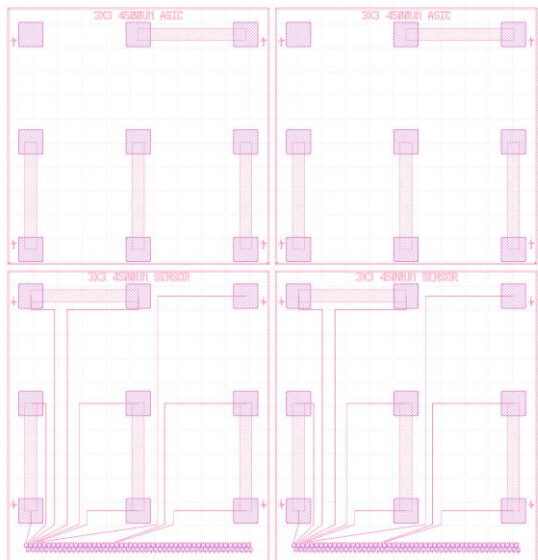
Preparation – daisy-chain devices

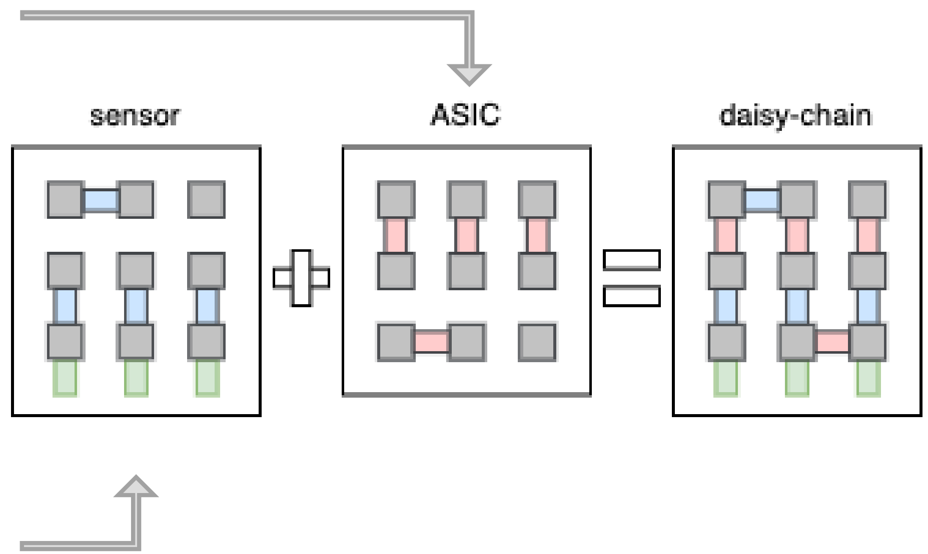
Design by Matteo Centis Vignali (FBK)

- Need to validate interconnect yield, electrical resistance, thermo-mechanical stress

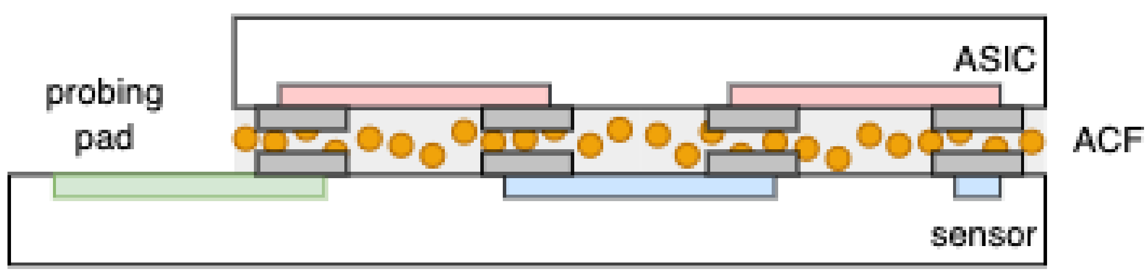
Top view:

3x3, pitch 4500um, diceable



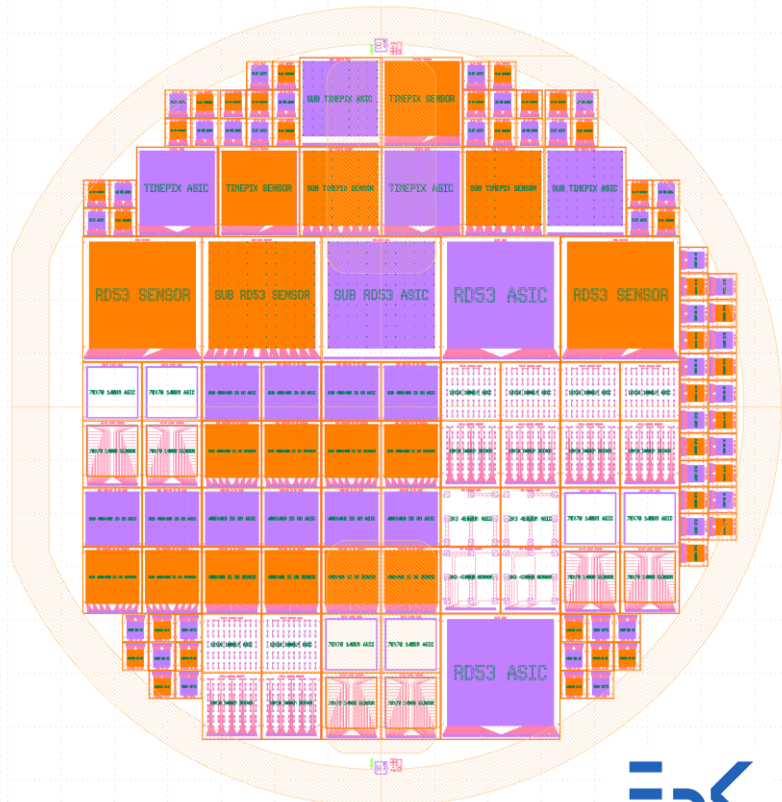


Side view:



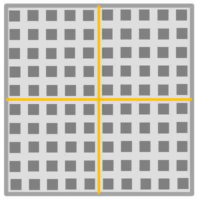
Preparation – daisy-chain devices

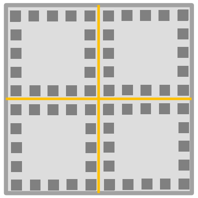
Design by Matteo Centis Vignali (FBK)



- Design being produced at FBK
  - 6” glass wafers, up to 650µm thick
  - Increased metal thickness (2 µm instead of standard 1 µm) and standard passivation thickness to better match topology of typical sensor/ASIC pairs
- Delivery expected in the following month
  - 70-150 probing pads based on the device
  - About 8 wafers in total

	pitch	size in mm	connections	per wafer	type	diceable
160x160 20um	20 um	3.2 x 3.2	25600	36	grid	no
CLICpix2	25 um	3.2 x 3.2	16384	34	grid	no
400x400 25um	25 um	20 x 20	640000	5	grid	yes
Timepix3	55 um	14 x 14	65536	4	grid	no
Timepix3 islands	55 um	14 x 14	65536	4	grid	no
RD53	50 um	20 x 20	160000	4	grid	no
RD53 islands	50 um	20 x 20	160000	2	grid	no
70x70 140um	140 um	20 x 20	2112	3	peripheral	yes
10x10 1000um	1000 um	20 x 20	400	3	grid	yes
3x3 4500um	4500 um	20 x 20	36	1	grid	yes


grid


peripheral

ACF hybridisation workflow

EP R&D

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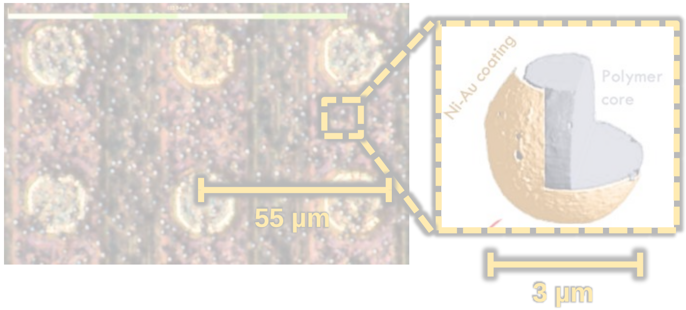
Timepix3 pixel matrix with ACF



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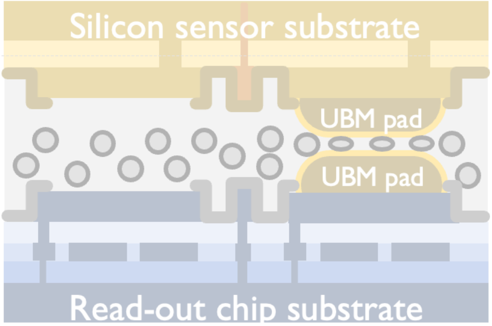

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- ENIG
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ACF
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Next talks by Janis, Florian & Julian

Conclusions and outlook

- **Small pitch bump bonding**
  - Single die process developed for **25 µm pitch** CLICpix2 hybrid assemblies
    - Very good efficiency results for **50 µm thick sensors**
  - Laboratory and beam-test results show excellent **yield of above 99.9%**

- **ACF interconnect**
  - In-house UBM plating and in-house ASIC-sensor connection (talk by Janis)
    - Extensive ENIG studies to achieve uniform metal growth
  - Ongoing improvements of the bonding parameters and ACF materials
  - Extended the ACF project to target module integration (see talk by Florian & Julian)

Small pitch interconnect

Peter Švihra

Single die ENIG process

Janis Schmidt

Module interconnection studies

Florian Dachs

Module tests

Milou van Rijnbach and Florian Dachs

Flex development and module concepts

Julian Weick

Single die ENIG process

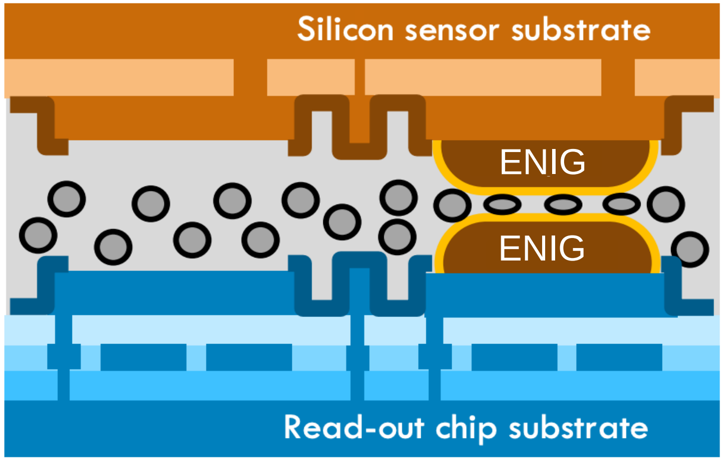
Janis Schmidt

Outline

- In-house ENIG UBM
- Process overview
- Results and challenges
- Summary and outlook

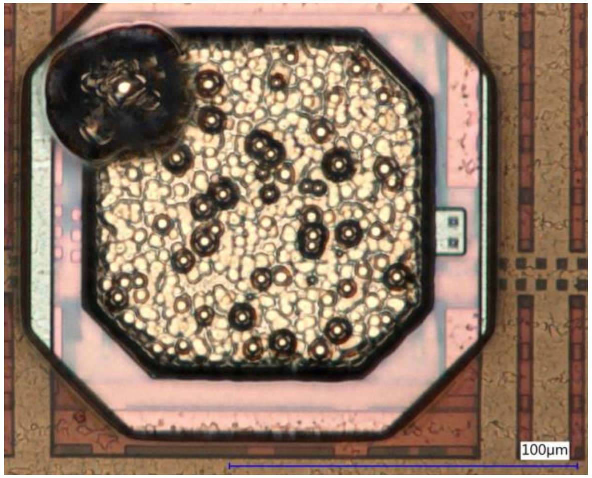
Motivation

- Basis for interconnection technologies (as ACF)
  - Height and surface area
  - Cavities for excess adhesive



ACF bonding with conductive micro-particles

- In-house production (at the EP-DT Micro-Pattern workshop Rui de Oliveira)
  - Single die processing possible
  - Short turnaround time
  - Quick adjustments possible
  - Quality control

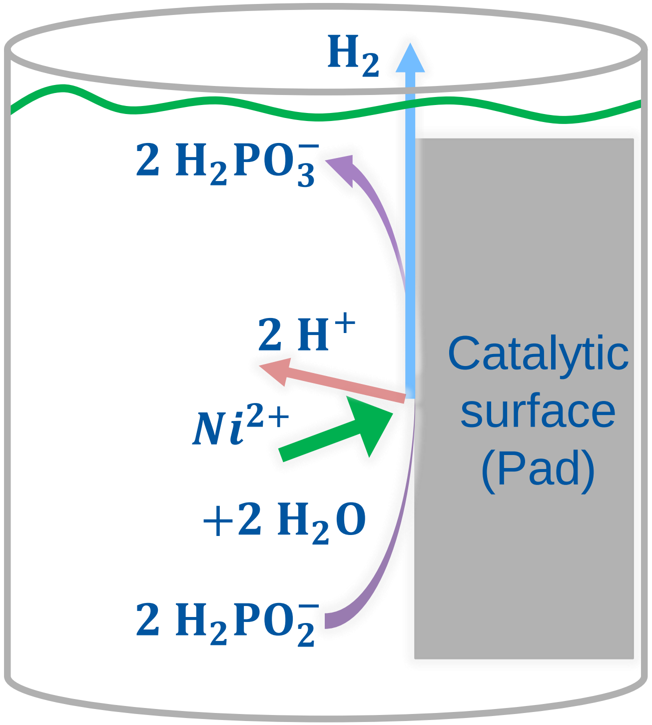


Insufficient quality from external producer

Electroless Nickel Immersion Gold

- Primarily used in PCB production
  - Bigger pad size
  - Different pad material

$$Ni^{2+} + 2H_2PO_2^- + 2\,H_2O \xrightarrow{cat} Ni + 2H_2PO_3^- + H_2 + 2H^+$$



1. **Electroless Nickel**
   - **Ni-P alloy**
   - **Bulk deposition**
   - **Autocatalytic**
2. Immersion Gold
   - corrosion protection
   - < 0.5 µm thick

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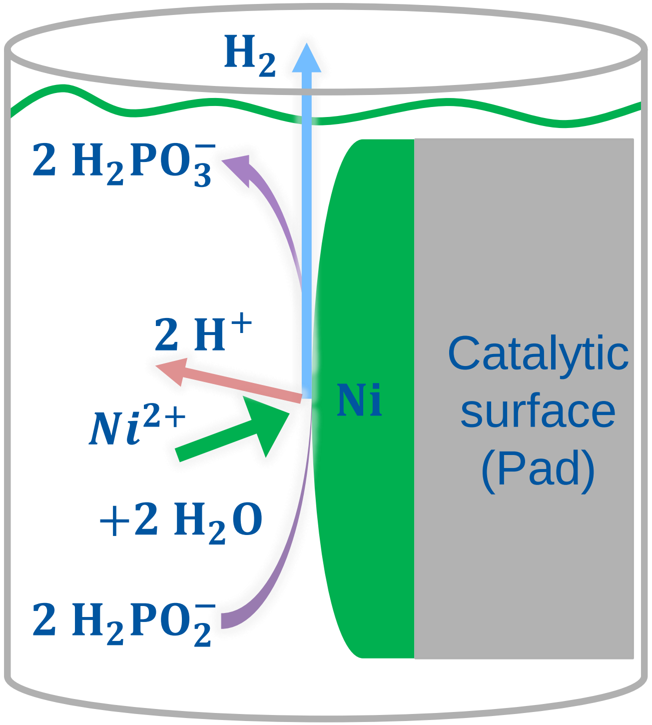

Electroless Nickel Immersion Gold

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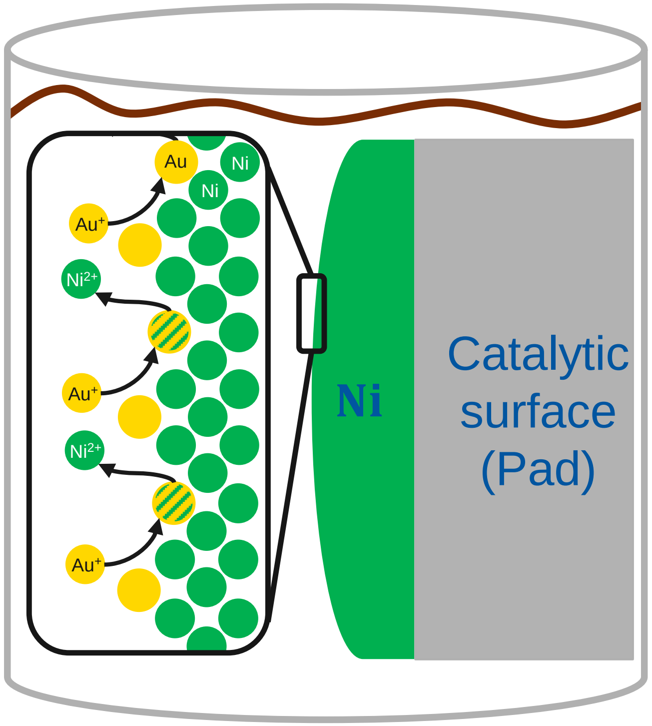
$$\mathbf{Ni + 2\,Au^{+} \rightarrow Ni^{2+} + 2Au}$$



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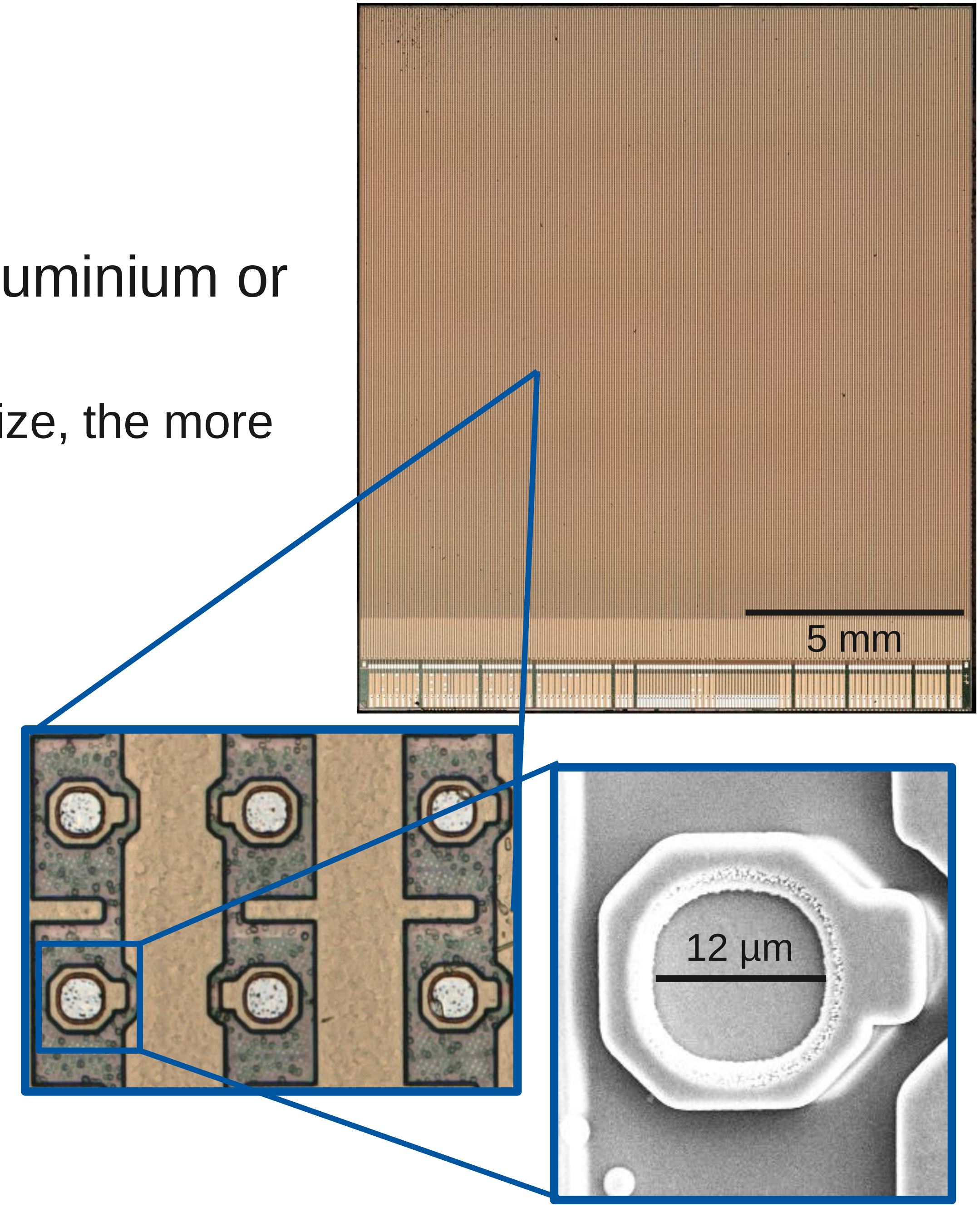
   - Ni-P alloy
   - Bulk deposition
   - Autocatalytic
2. **Immersion Gold**
   - **corrosion protection**
   - **< 0.5 µm thick**

Samples

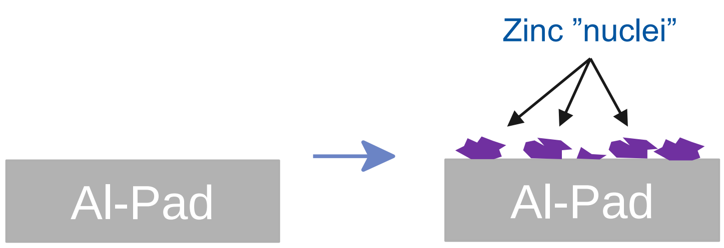
- Plating possible on aluminium or copper pads
  - The smaller the pad size, the more difficult the plating

Used samples		
	Pad size	**Material**
Timepix3	**12 µm**	**Al**
Timepix3 with UBM	**18 µm**	**Pd-Au**
MALTA2	**88x88 µm**	**Al**
ALTIROC1	**88x88 µm**	**Al**
CLICpix2	**8x10 µm**	**Al**

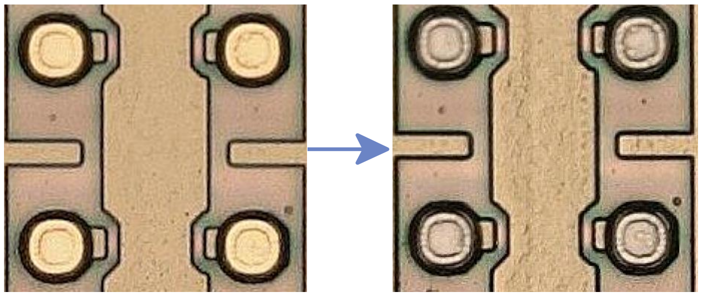


Pre-treatment

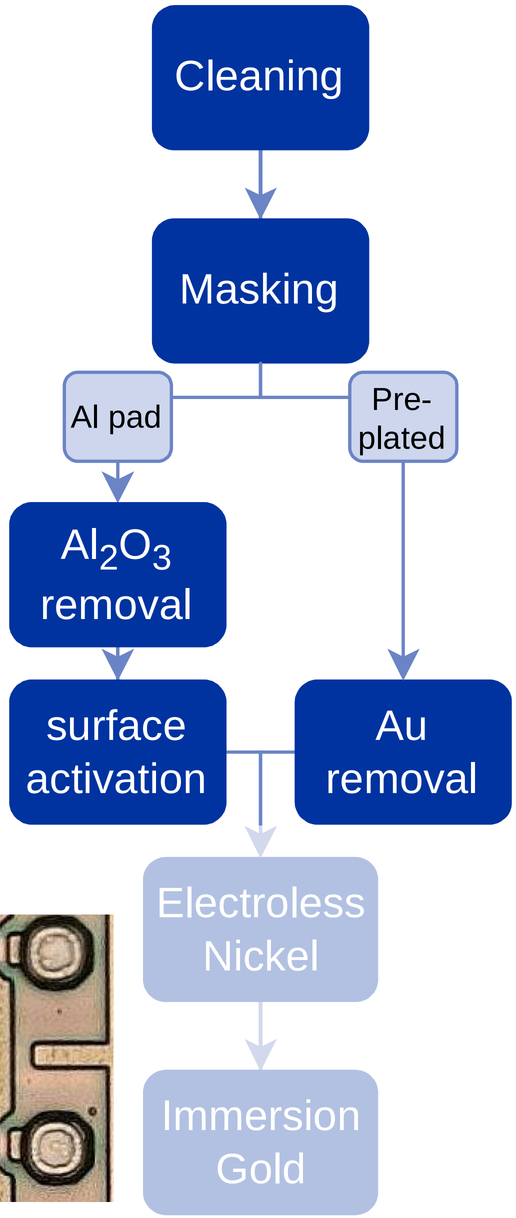
1. Chemical cleaning
   a. Alkaline detergent in ultrasonic bath
   b. Acetone bath
   c. Deionized water rinsing
2. Masking with toluene soluble paint
3. Oxide removal
   a. 75% H_3PO_4
4. Double zincation



3. Gold removal
   a. Cyanide

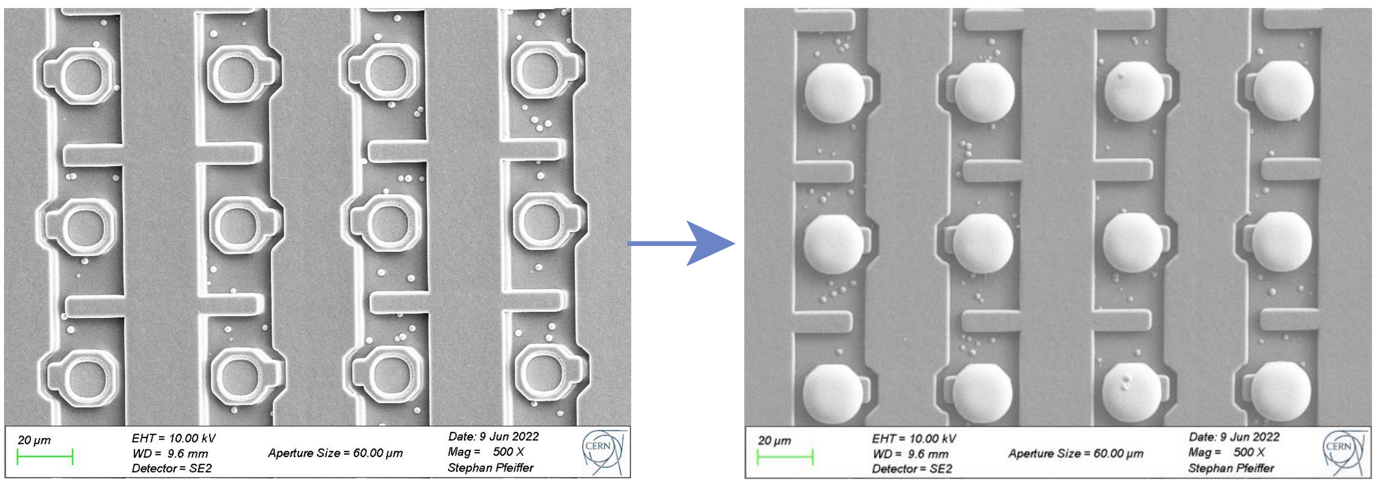


Exposed Pd-surface is catalytic

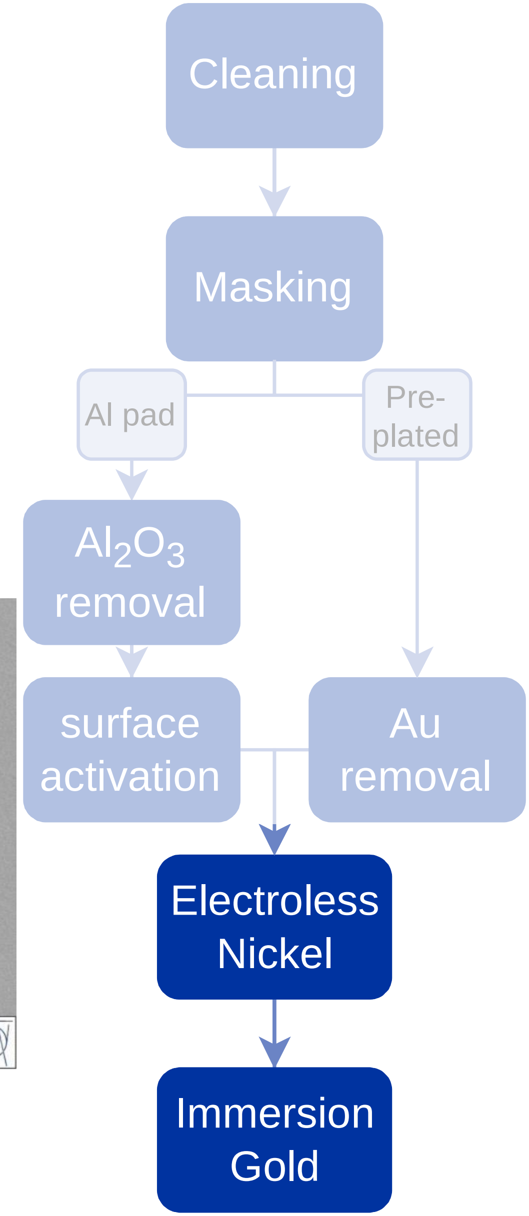


Electroless Nickel

1. Electroless Nickel
   - Growth rate 20 µm/h
   - Limited by reaction speed of $H_2PO_2^-$
   - Temperature, PH, $H_2PO_2^-$ concertation



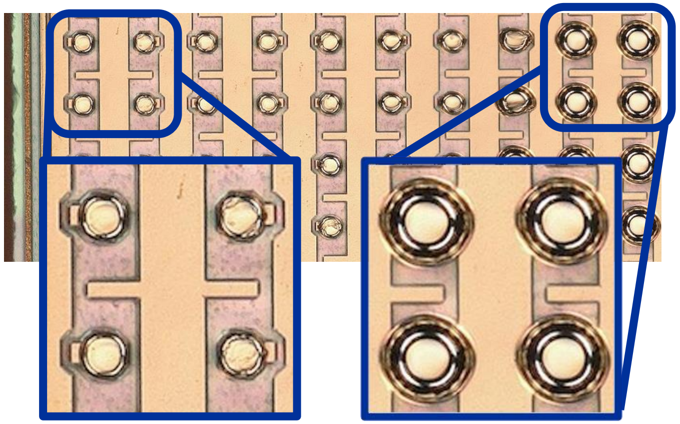
2. Immersion Gold
   - Limited by diffusion speed of Au^+ and Ni



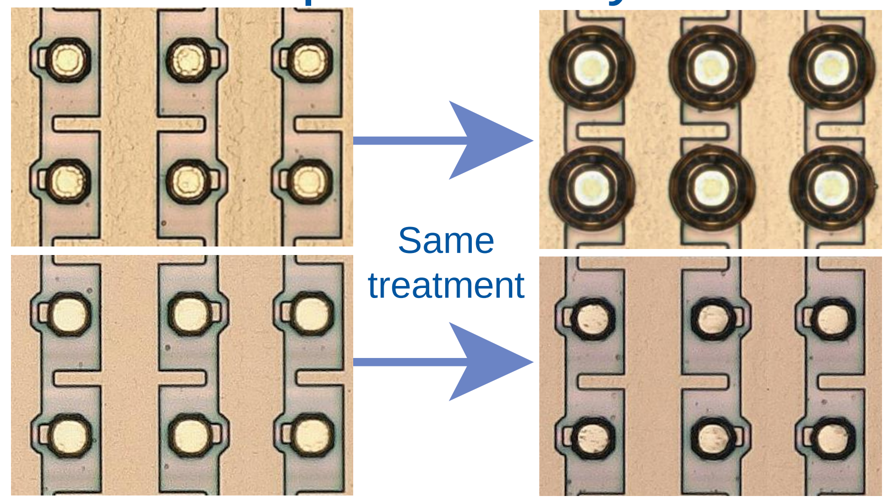
Challenges

Uniformity

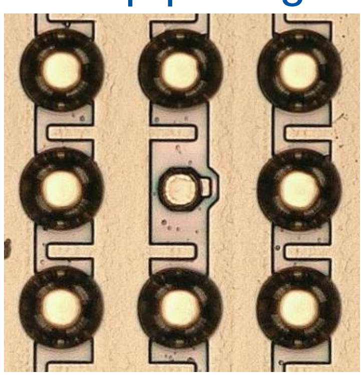
Missing plating at the edge



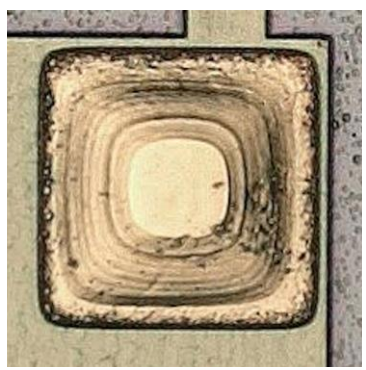
Reproducibility



Skip plating



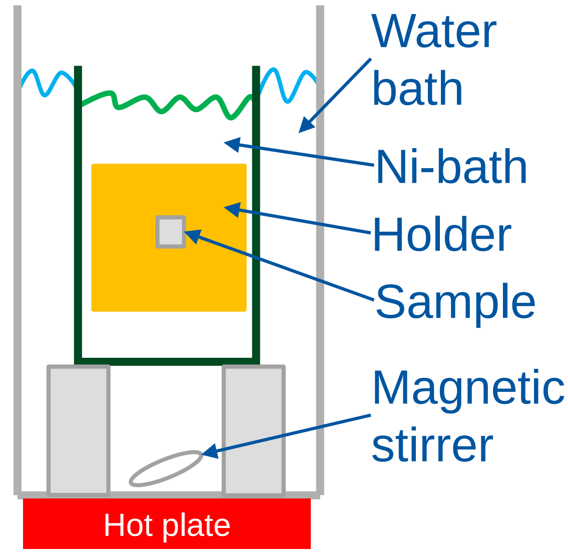
Step plating



- Improved reproducibility in separate smaller bath
- Stabiliser and contamination poisons catalytic surface and terminates the reaction
  - Diffusion faster to small pads and edge

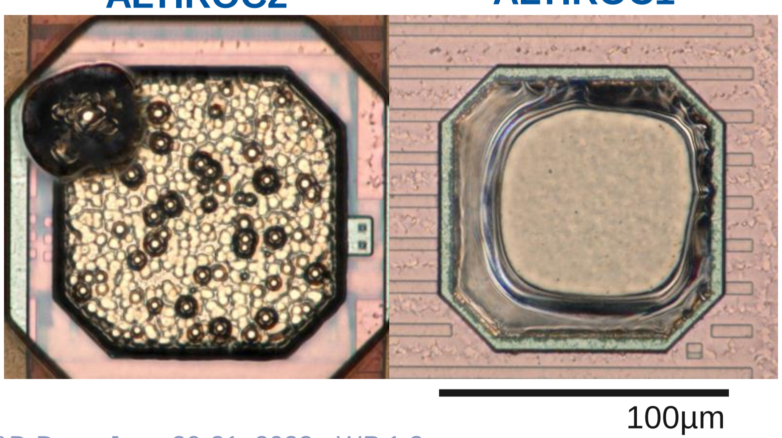
Current setup and results

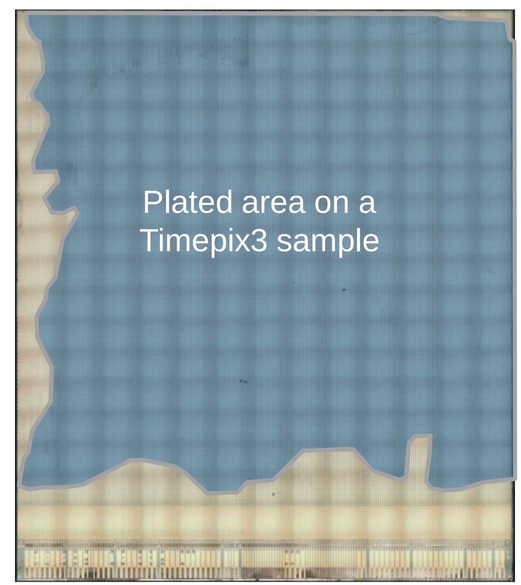
- Nickel bath in water bath
  - Small volume of 0.5 – 1l
  - No mechanical convection
  - Adaptation of parameters possible
    - Temperature, PH level, $H_2PO_2^-$ concertation
- In past focus on Al pad Timepix3
  - Improved plated area to ~ 80-90%
- Partially already better results than external plating



External ENIG on **ALTIROC2**

In-house ENIG on **ALTIROC1**

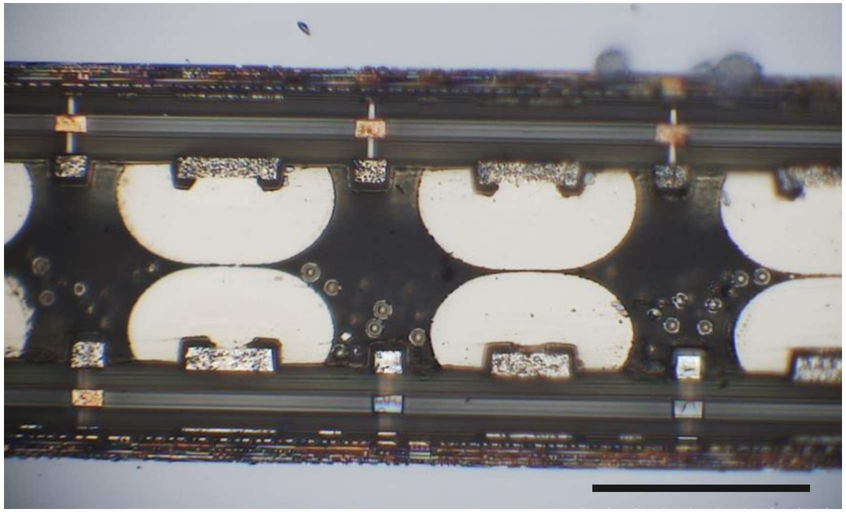




Conclusion and outlook

- Ongoing development of in-house ENIG plating
  - Plated area to ~ 80-90% on Al-pad Timepix3
  - Better understanding of occurring problems
- Large enough area to start with ACF trials

- Dedicated production line
- New chemicals
  - Aluminium activation
  - Nickle bath
    - Higher purity
    - Different and known stabiliser


40 µm

Small pitch interconnect
Peter Švihra

Single die ENIG process
Janis Schmidt

Module interconnection studies
Florian Dachs

Module tests
Milou van Rijnbach and Florian Dachs

Flex development and module concepts
Julian Weick

Module interconnection studies

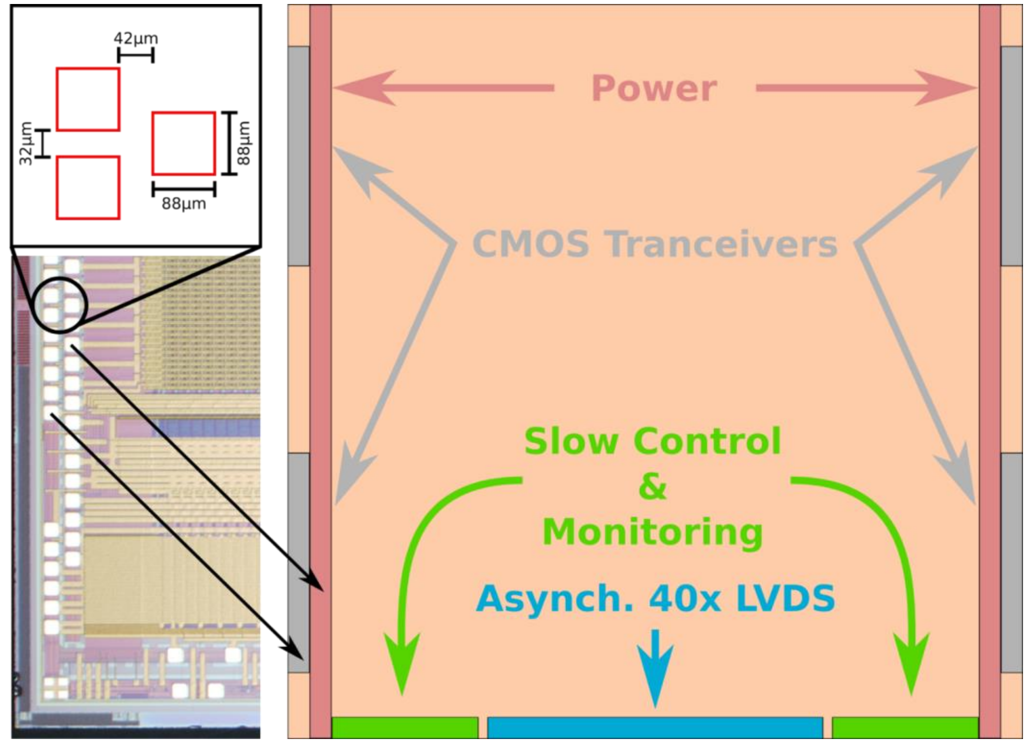
Florian Dachs

Outline

- MALTA module capability
- MALTA module production and testing
- ACF interconnection studies
- Summary and outlook

MALTA module capability

- MALTA features:
  - Monolithic CMOS pixel detector
  - Fully asynchronous front-end and readout
  - $2x2cm^2$ size, 512 x 512 pixel matrix
  - $36.4x36.4µm^2$ pixels → high granularity
  - Raditation hard to $2x10^{15}$ n^{eq}/cm^2 and 100MRad
- Main 40x bit parallel LVDS readout at bottom periphery
- Alternatively, data can be routed between CMOS transceiver blocks at the left and right chip edge (1 ns pulse width)
- MALTA word contains 4 chip ID bits for a maximum module size of 16

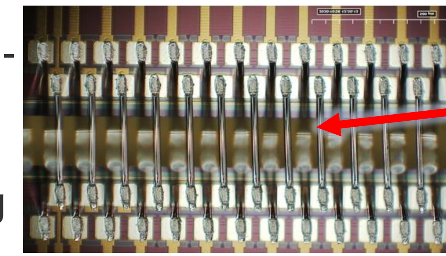


The MALTA pad layout allows the assembly of modules with chip-to-chip power and data transmission.

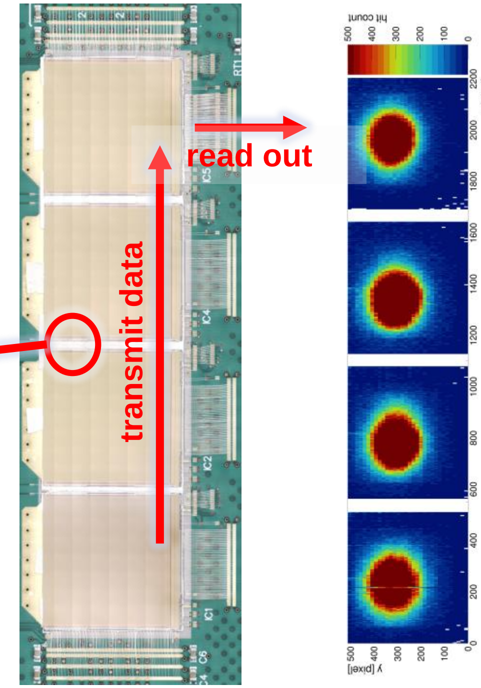
The entire module is read out through the primary chip.

MALTA module production and testing

- Several 2-chip and 4-chip modules successfully assembled and tested
- Interconnection for these modules was realized using Al wedge wire bonding (EP-DT Bondlab)
- Signal timing and data transmission along the module verified
- Beam tests in the lab and at the SPS North Area (**see slides by M. van Rijnbach**)



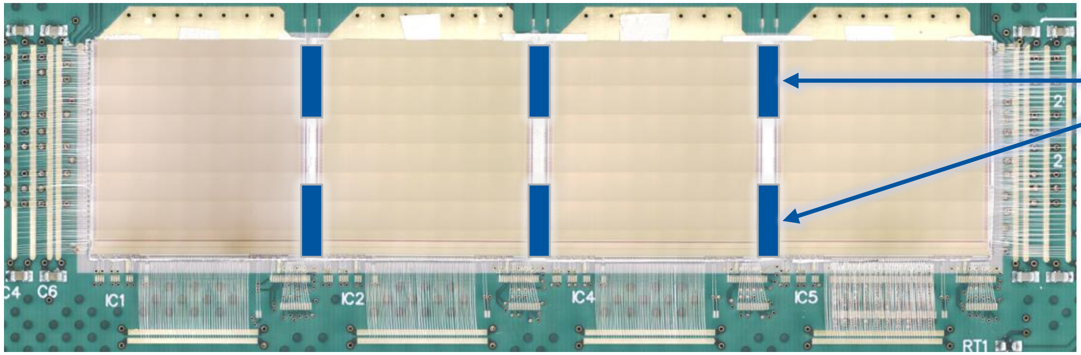
Sr90 source test



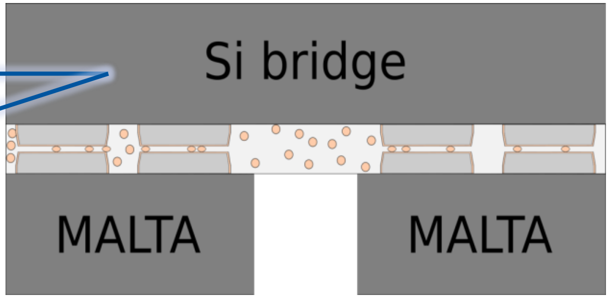
Designation	Used chips	Performed tests
Dual 1	2x MALTA (100µm thick, 25µm epitaxial layer)	^{90}Sr, muons, pulse timing, threshold
Dual 2	2x MALTA (100µm thick, 25µm epitaxial layer)	^{90}Sr, muons, pulse timing, threshold
Quad 1	4x MALTA (100µm thick, 25µm epitaxial layer)	^{90}Sr, muons, pulse timing, threshold
Quad 2	4x MALTA (100/300µm thick, 25µm epitaxial layer)	^{90}Sr, muons, pulse timing, threshold, SPS beam tests
Quad 3	4x MALTA (100/300µm thick, 25µm epitaxial layer)	^{90}Sr, muons, pulse timing, threshold, SPS beam tests

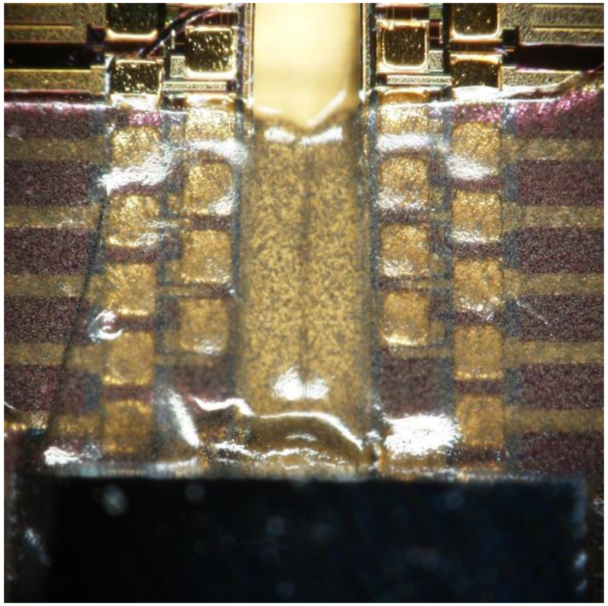
ACF interconnection studies for MALTA modules

EP R&D



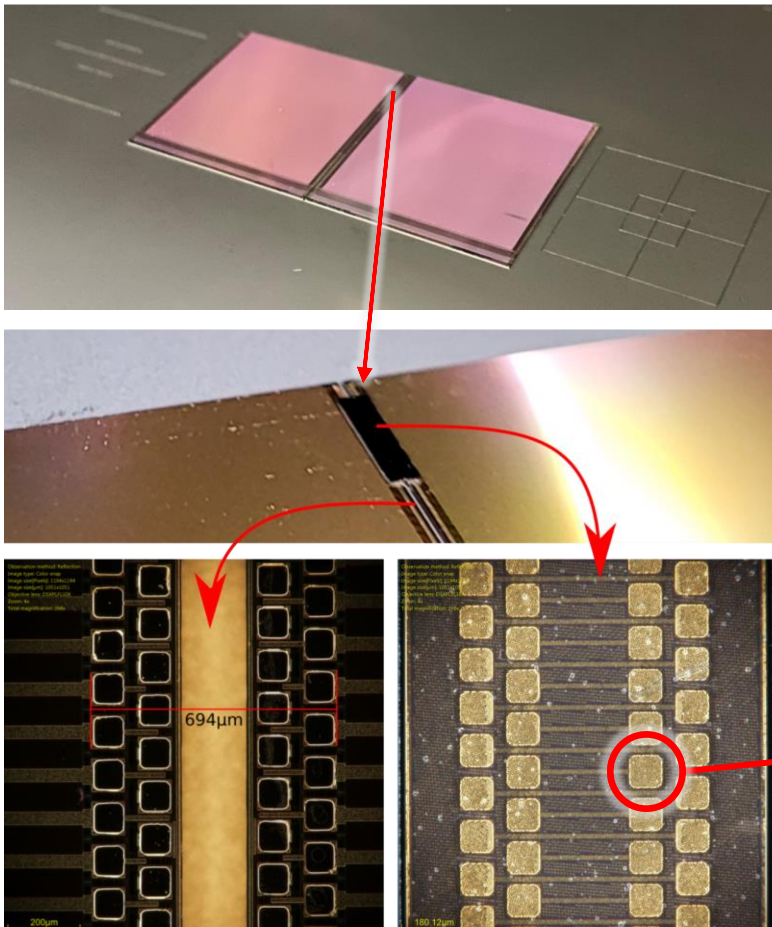
Conceptual 4-chip module with ACF interconnections



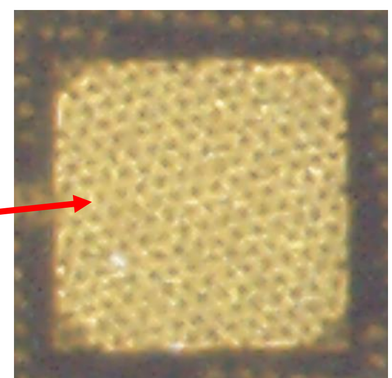


- Besides MALTA, STREAM wafer reticle also features silicon interposer ("Si-bridge") for chip-to-chip data and power transmission
- ACF under study for mechanically robust and scalable alternative to wire bonds (**see slides by P. Svihra**)
- Prerequisite: Ni/Au plated pads (**see slides by J. Schmidt**)
- Replace wire bonding connections between chips – and potentially all connections – by moving to a flip chip module approach (**see slides by J. Weick**)

ACF interconnection studies for MALTA modules – material preparation



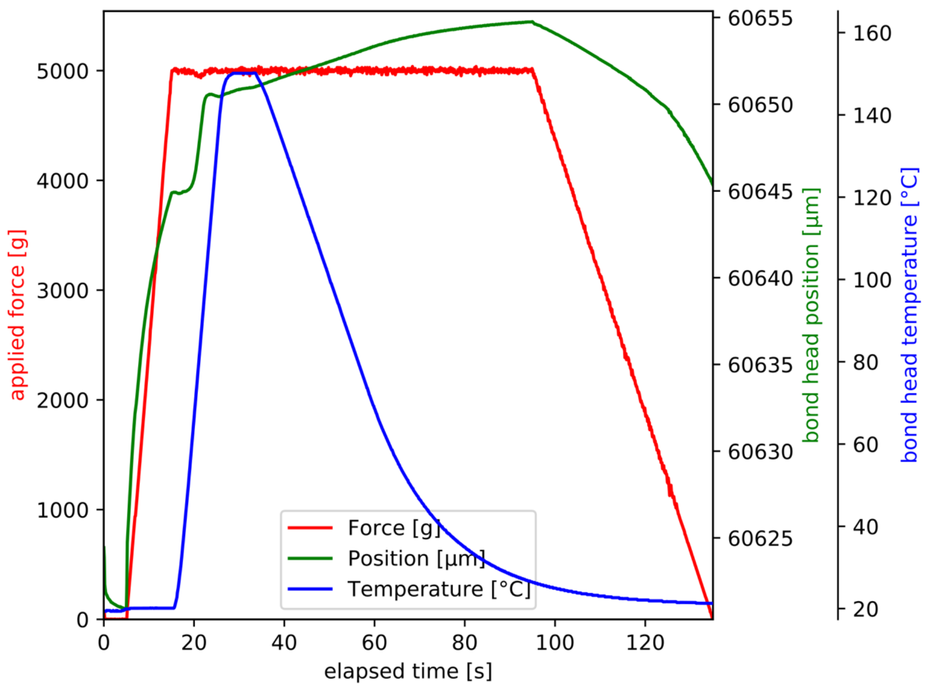
- Si-bridge produced on same reticle as MALTA chip, thus thinned to 100/300 µm
- ENIG plating of single dies at EP-DT micropattern workshop (chips and Si-bridges)
- chips are positioned on dedicated SiC vacuum chuck to match pad pitch on Si-bridge
- silicon interposer ("Si-bridge") is laminated with ACF



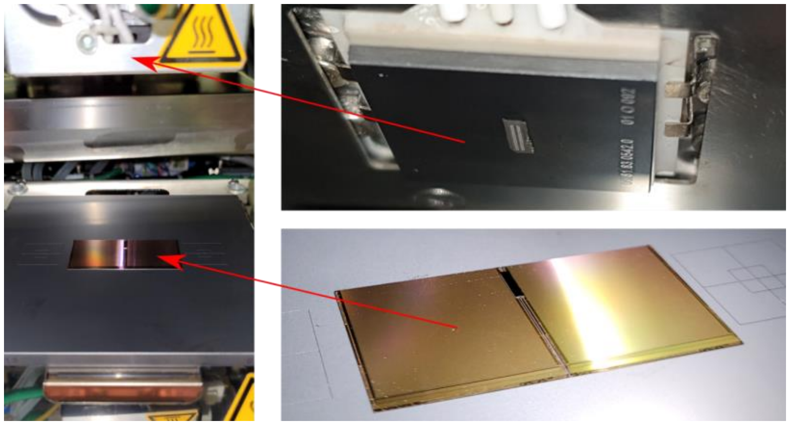
This step required many tests with multiple ACF flavours, support structures, lamination procedures, etc.

→ well tested procedure established

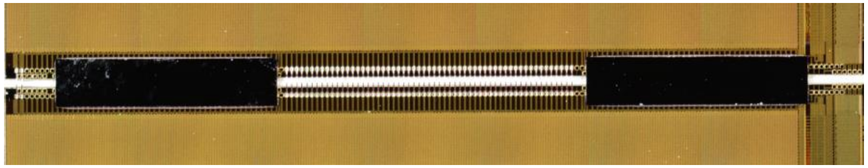
ACF interconnection studies for MALTA modules – bonding process



bond head on top



vacuum chuck on bottom

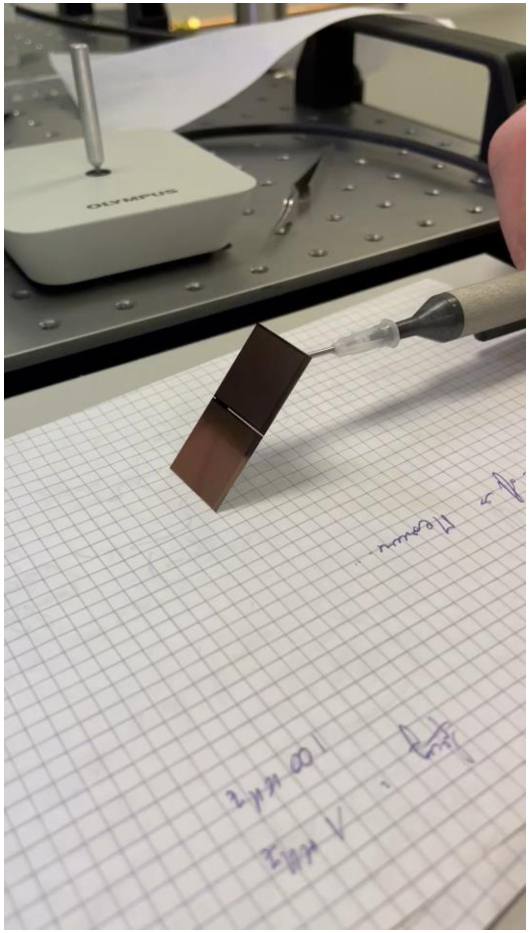


finished product

- High bonding pressure needed (in this case: 5kg pressure on 1x5mm^2 Si-bridge)
- Curing temperature of 150ºC needed for 10s
- **Mechanically intact modules can be assembled reliably**

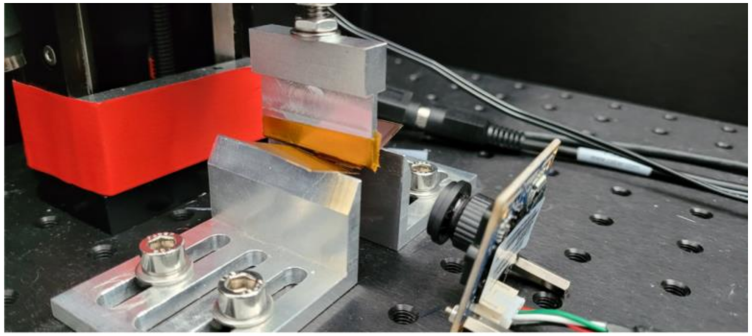
ACF interconnection vs vacuum pen

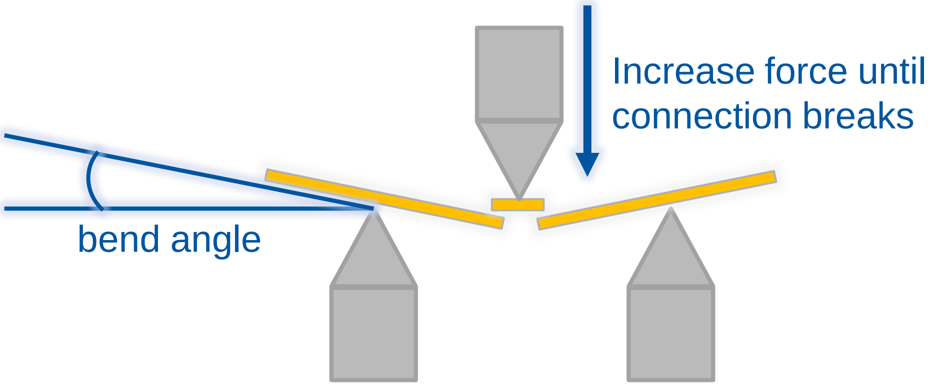
- Assembly in the video consists of two dummy MALTA chips and one Si-bridge
  - All dies 100 µm thick
  - Glue contact area between Si-bridge and chips ~ 4 mm^2
  - Pad contact area: 1.22 mm^2
- ACF connection proves to be extremely sturdy even with just one Si-bridge in place

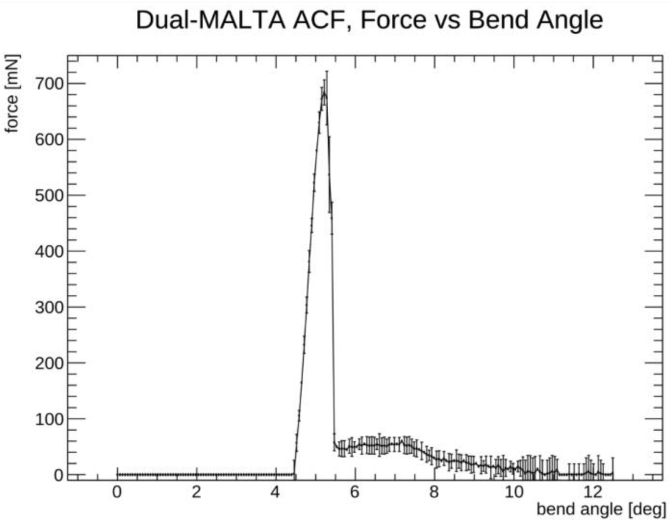


ACF interconnection studies for MALTA modules – mechanical tests

- **Mechanical stress test performed with ALICE setup** (by Magnus Mager and Alperen Yuncu)
- Module is placed on two fixed pins
- Pressure is applied on Si-bridge with third pin
- **Connection breaks abruptly at 700 mN force and a 5° bend**
- **Setup offers quantitative method to study ACF mechanical performance e.g. versus irraditation**

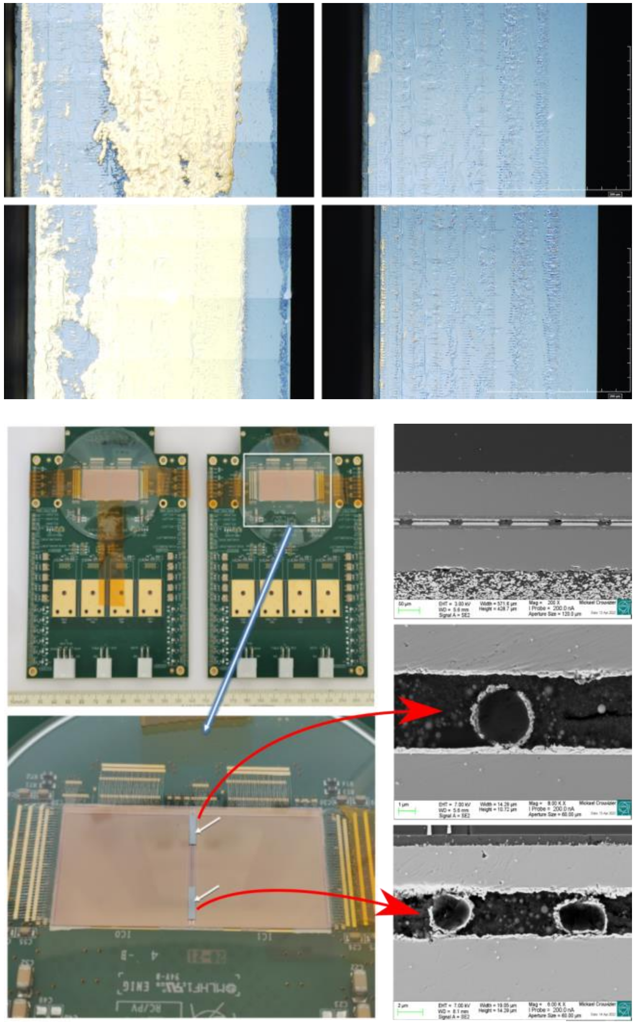






ACF interconnection studies for MALTA modules – electrical tests

- Electrical tests only show partial functioning
  - Shorts observed on power and bias connections
- ENIG depositions on chip edges observed
  - Possible explanation for shorts
  - Currently looking for ways to prevent these depositions, e.g. masking
- SEM images show missing connections on one bridge (5kg pressure was used on both)
  - ACF glue was past expiration and may have hardened (supply of new glue very difficult in current market situation)
  - New ACF glue is being procured to repeat the assembly



Cross sections done at EN-MME-MM

Summary and further steps

- Connect MALTA chips using a Si bridge that provides data and power transfer from chip to chip using ACF
- Process set up, flip chip machine support, bonding procedure and mechanical tests are commissioned and can be carried out routinely
- Electrical tests have not yet been successful
  - New ACF must be procured for module production
  - Address observed issues with shorts and prevent ENIG deposition on chip edges
- In parallel development of dedicated test-structures (see talk by Peter and Julian)
  - Dedicated structure to evaluate interconnection yield, signal behaviour, resistance and power transfer of ACF

Small pitch interconnect
Peter Švihra

Single die ENIG process
Janis Schmidt

Module interconnection studies
Florian Dachs

Module tests
Milou van Rijnbach and Florian Dachs

Flex development and module concepts
Julian Weick

MALTA module beam tests

Milou van Rijnbach, Florian Dachs

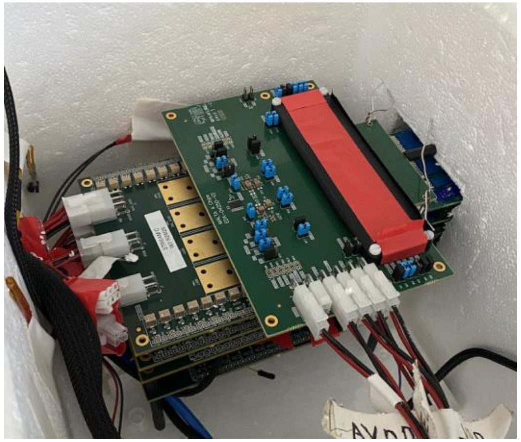
Outline

- Tests of wire bonded MALTA 2-chip and 4-chip modules in a table top telescope
  - Telescope setup and analysis
  - ^{90}Sr tests
  - Cosmic muon tests
- Tests of 4-chip module in SPS telescope
  - 6 MALTA planes as reference, 1 plane as device under test (DUT)
- Future plans and outlook

Table top telescope: ^{90}Sr tests

Mix of 1-, 2- and 4-chip modules

- Small scale set-up : **4 MALTA plane telescope set-up with possibility for Sr90 and cosmic muons measurements** (limited statistics).
- Flexible set-up to demonstrate basic **functionality of new chips / modules and improve DAQ procedure. Dry test before installation in the beam.**
- Alignment, reconstruction and tracking routines.
- **Test of all multi-chip modules with chip-to-chip connections in this setup.**



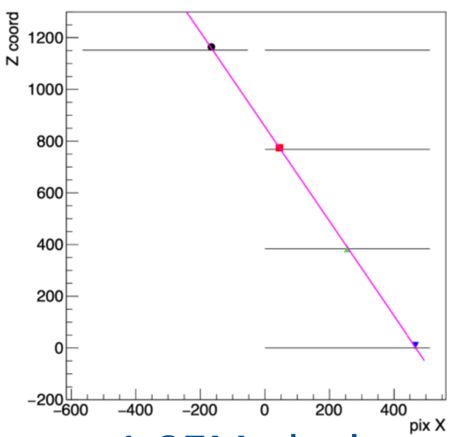
Dual chip module

P0: Dual Chip

P1: Single Chip

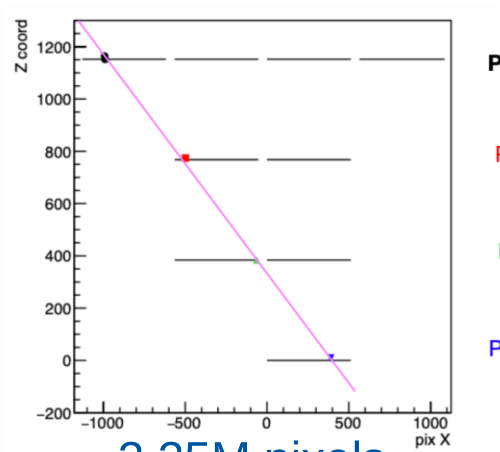
P2: Single Chip

P3: Single chip



1.25M pixels

Quad+Dual chip modules



P0: Quad Chip

P1: Dual Chip

P2:Dual Chip

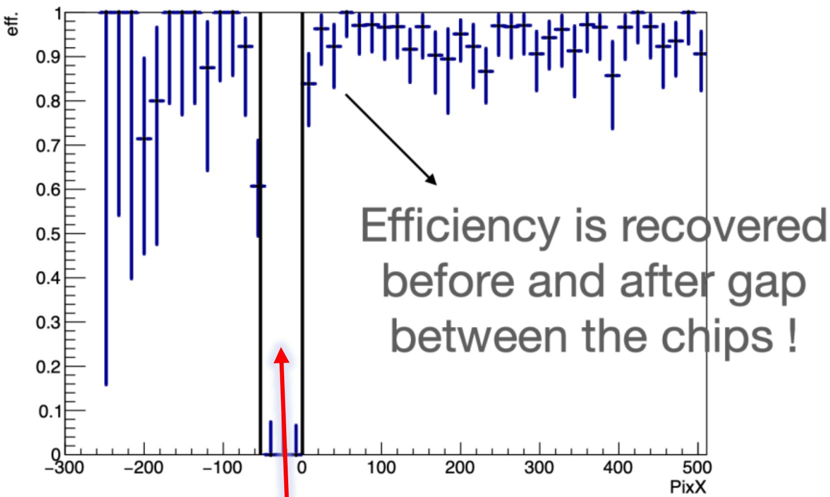
P3: Single chip

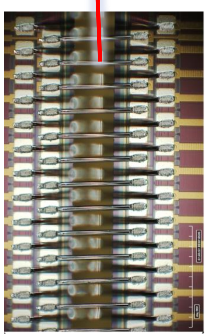
2.25M pixels

Table top telescope: Cosmic muon tests

Mix of 1-, 2- and 4-chip modules

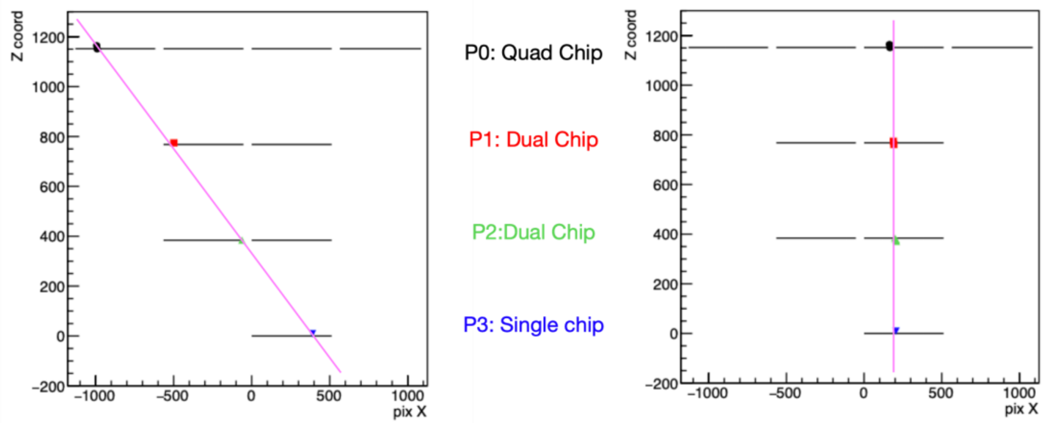
1D (x-direction) Efficiency map of dual chip module





Gap ~ 2 mm
from pixel to pixel

Event reconstruction in quad chip + 3 reference planes (inclined and straight track)

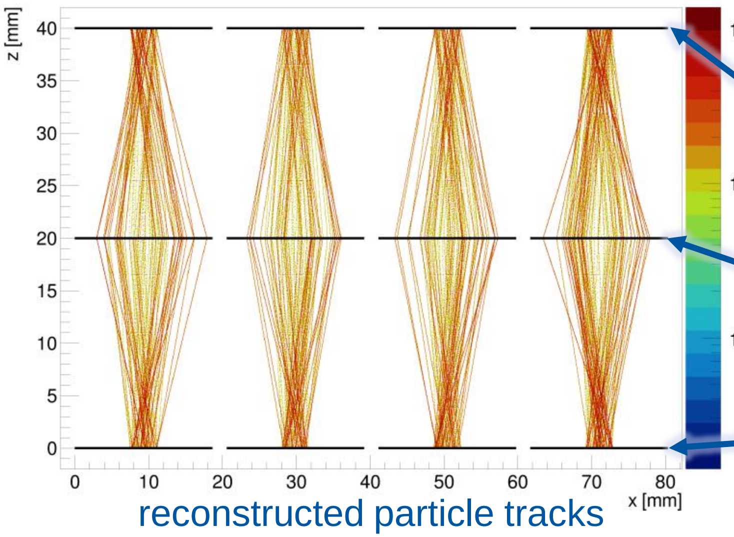


- All data is transferred via the CMOS transceivers from one chip to the next and only the master chip is read out.
- No statistics at outermost side of left chip due to geometrical acceptance for cosmic muons (see plot of event reconstruction).
- At low statistics, alignment with cosmic muons becomes challenging. However, significant areas of the module achieve efficiency >90%.
- Gap is limited by minimum distance required for wire bonding and chip edge/last active pixel → see slides by Julian for a flip chip module approach

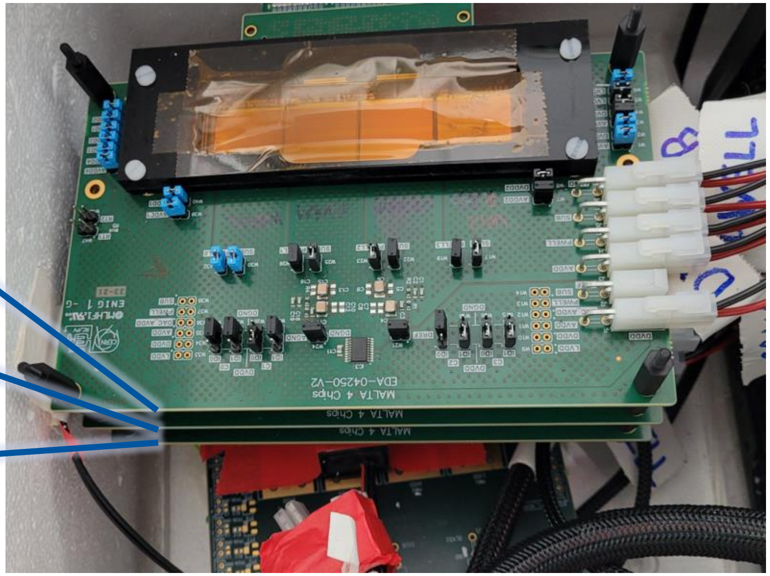
Table top telescope: Preparation for SPS beam tests

Three 4-chip modules tested with a ^{90}Sr source

EP R&D



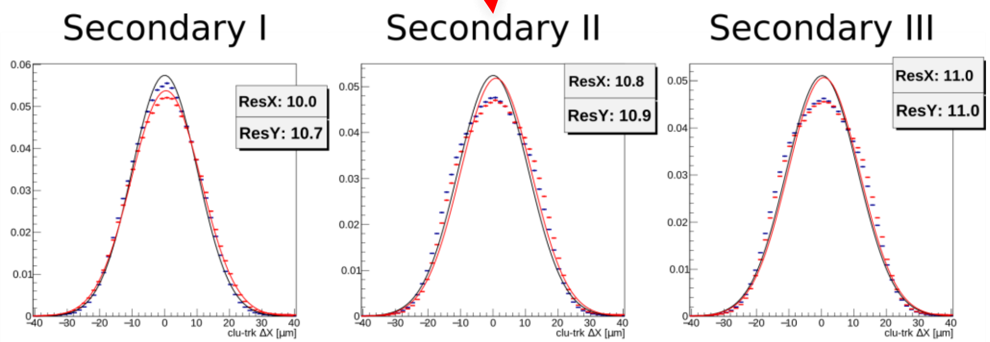
reconstructed particle tracks



- **Three 4-chip modules fully integrated in minimal telescope configuration with 3 planes**
  - Coincidence trigger on top/bottom plane, middle plane acts as DUT
  - Full trigger and readout chain verified
  - Setup used to prepare for smooth integration into SPS beam telescope

SPS beam telescope: 120GeV/c^2 pions

- **First beam June 3-5, 2022 at H6**
- Data taken with two quad modules in the beam
- Wide beam setting used to cover entire MALTA chip (2x2 cm^2) at each secondary chip position
- Data analysis ongoing
  - Some debugging and verification needed



track-cluster residuals on secondary chips

Outlook

- More test beam time will be available later in 2022
- Improvement of the mechanical support for the quad module to allow rotation
- Possible irradiation of quad or dual chip module to demonstrate radiation hardness of the module

EP R&D

Small pitch interconnect
Peter Švihra

Single die ENIG process
Janis Schmidt

Module interconnection studies
Florian Dachs

Module tests
Milou van Rijnbach and Florian Dachs

Flex development and module concepts
Julian Weick

Further modularization studies

Julian Weick

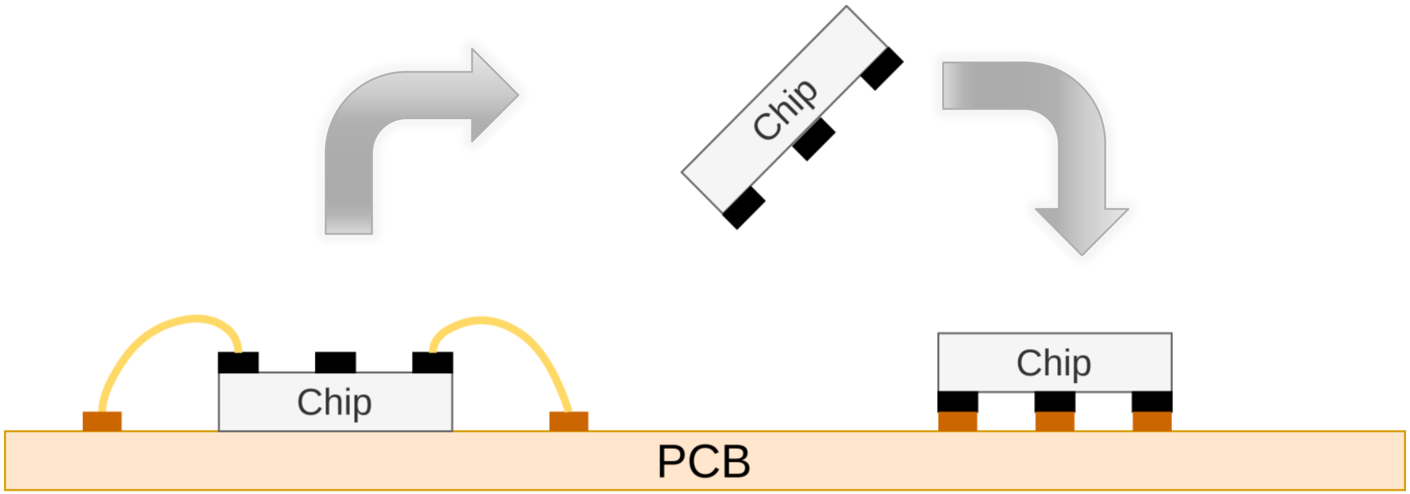
Outline

- New **packaging and interconnection** technologies are studied with the goal to develop a **cheap, light** and **scalable** approach to **modularization**

- Current studies are done with MALTA2 with the perspective to **transfer the results** to other chips

- Key focus areas:
  - Development of a **flip-chip** based module assembly for dense packaging and low material budget
  - Study of **ACF and nanowires** as scalable interconnection techniques
  - **Radiation hardness** studies
  - Integration of **optical signal transmission** on the module level

Module flip-chip mounting

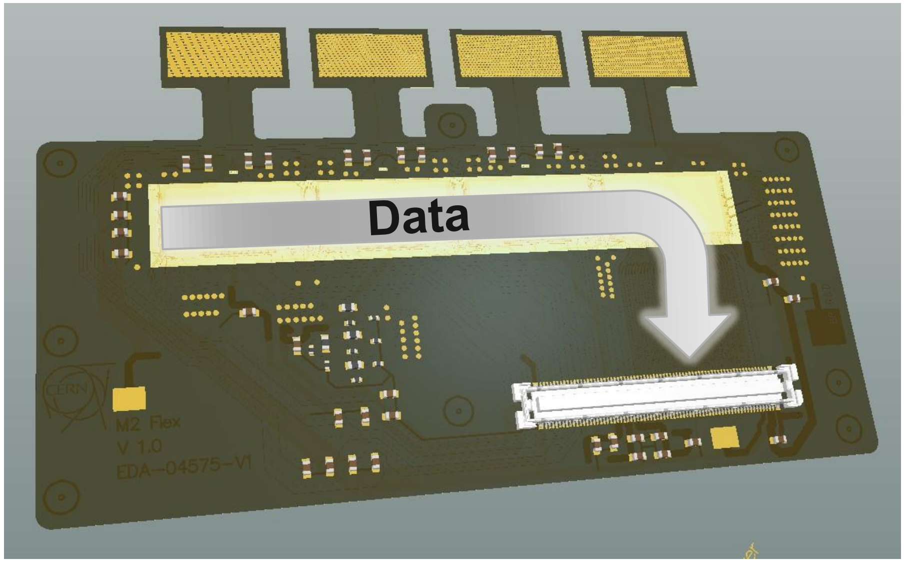


A flip chip mounted module provides:

- **Minimal spacing requirements between the chips**, thus allowing to further reduce the insensitive region between chips (note: a flip chip process can also be applied to a **stitched device**)
- A **scalable interconnection** time also for **large numbers of pads**
- Depending on the interconnection technology also **a mechanical connection** of the module**.**

Data flow and powering

- Use the existing **MALTA2 pads** dedicated for wire bonding (Al pads with 88 x 88 um^2, ~482 pads per chip)
- **Two-layer** layout with debug possibility
- Data **transferred via CMOS** transceivers to master chip as validated in 4-chip board
- **Master chip transmits** Data to DAQ via LVDS
- **Single power domain** for each chip allows to individually tune power parameters

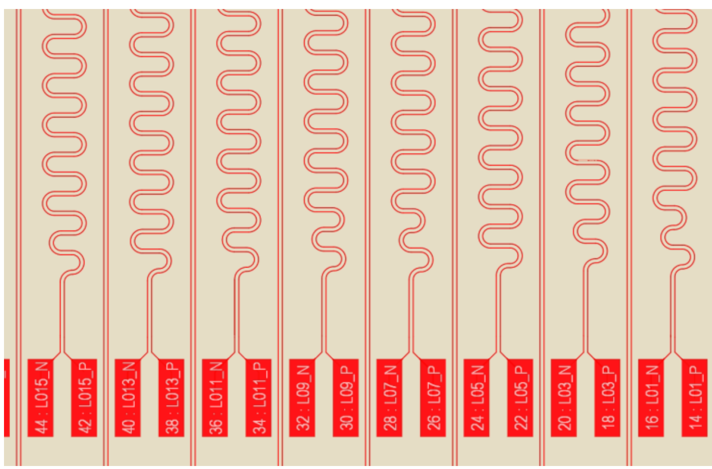


Fine structures

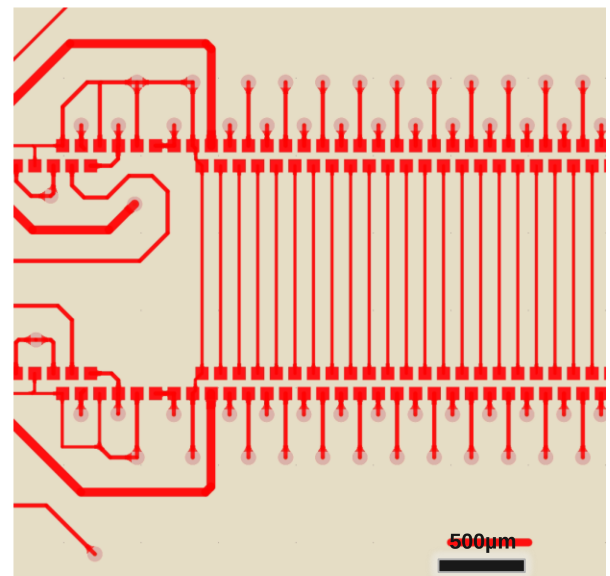
EP R&D

The used techonology enables a small track width and pitch:

- Advanced fabrication technology allows for structures down to 15 µm in track width and clearance
- Thickness of polyamide layer: 10µm
- Thickness of copper layer: 6µm
- Solder stop: 20µm
- **Total thickness ~50µm**



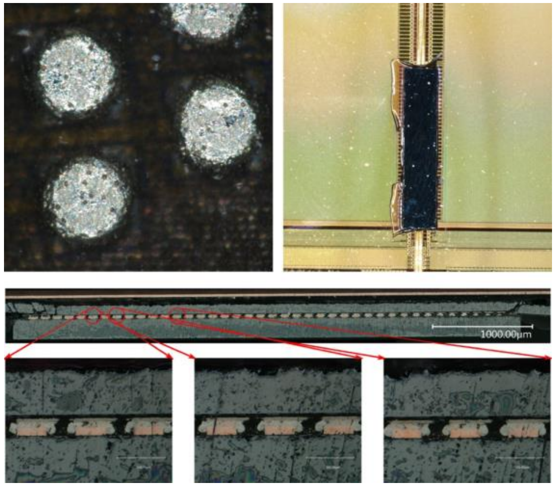
Length matched data output on Master chip on connector with 200 um spacing



Chip2chip CMOS connection

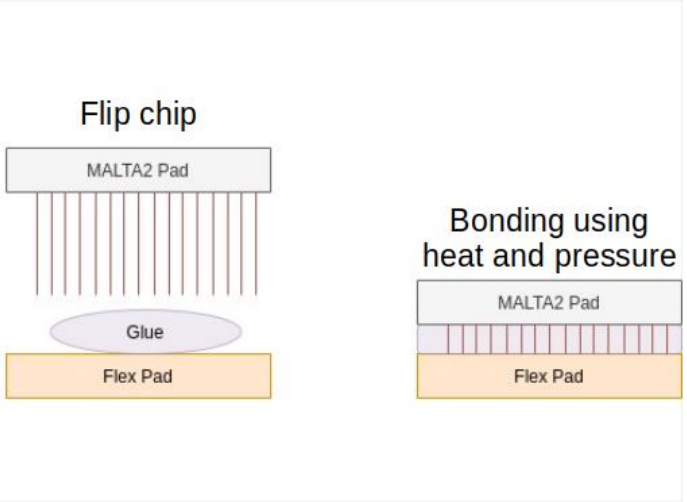
Considered chip-to-flex connection technologies

ACF



- Potentially fast interconnection process
- Suitable for a large number of pads
- Provides mechanical stability
- Ongoing process

Nanowires

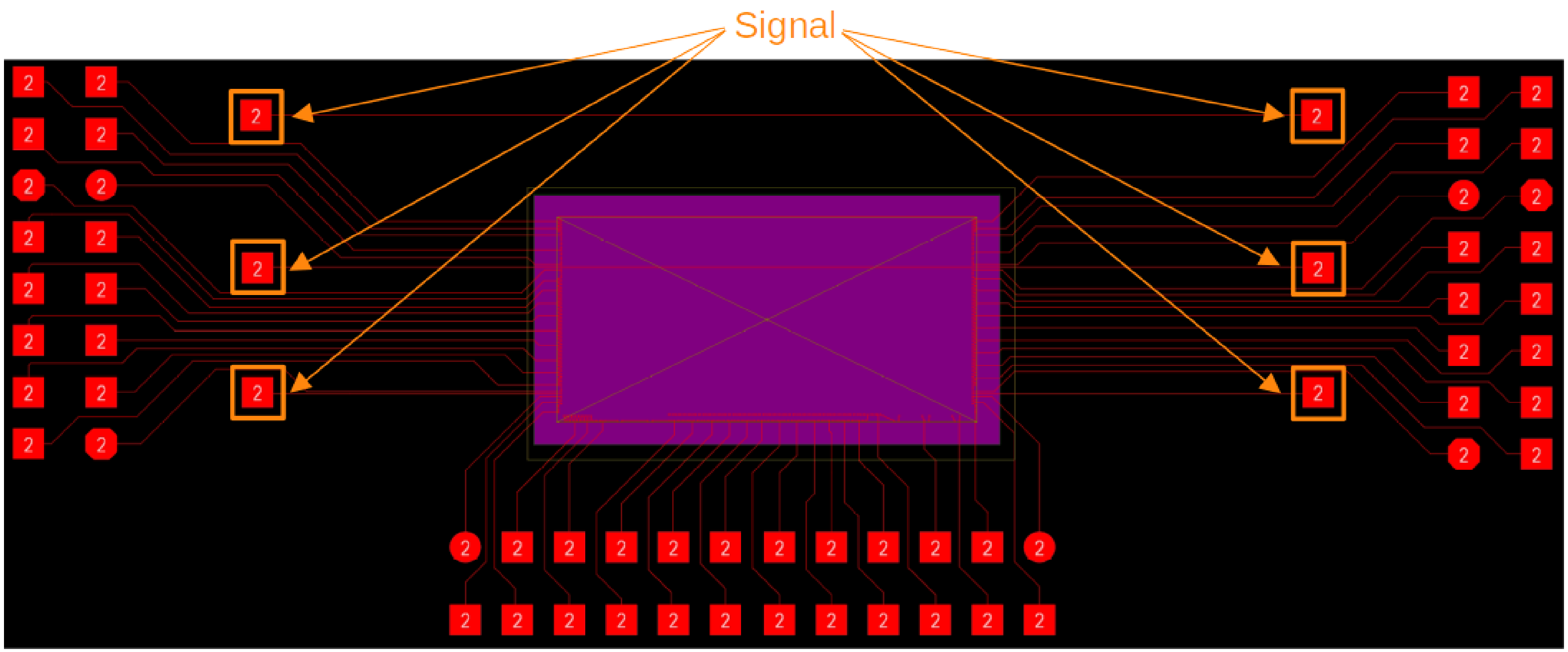


- Scalable process on chip or flex, also compatible with wafer-level processing
- Glue support for additional mechanical stability possible
- Low contact resistance, low parasitic loads

Interconnection test structure

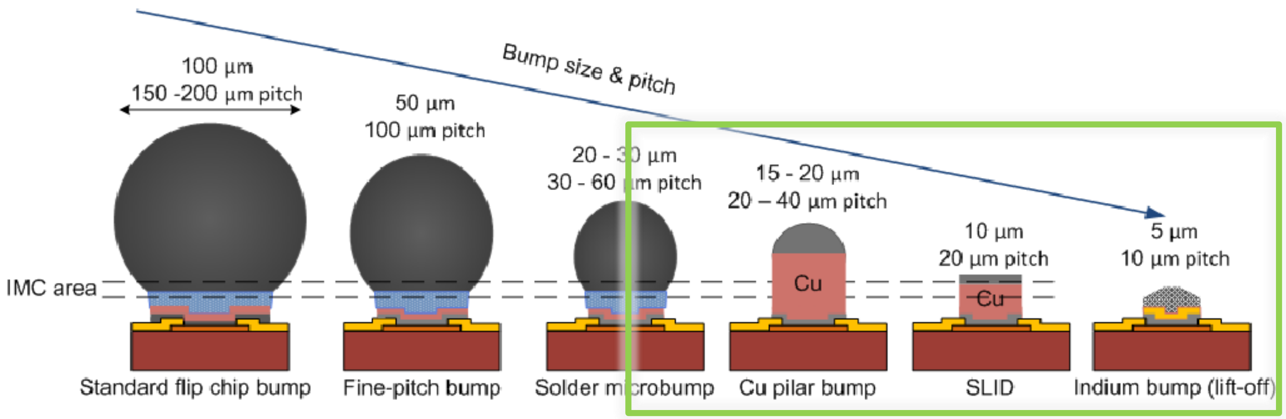
Dedicated test structure on AlN using the fine pitch structuring process of the flex:

1. Assess the **yield in successful** pad to pad interconnection using nano wires and ACF
2. Assess the **short circuit yield** in pad to pad interconnection using nano wires and ACF
3. Evaluate the **signal behavior** and **resistance** of the interconnection
4. Evaluate the **mechanical properties** of the interconnection



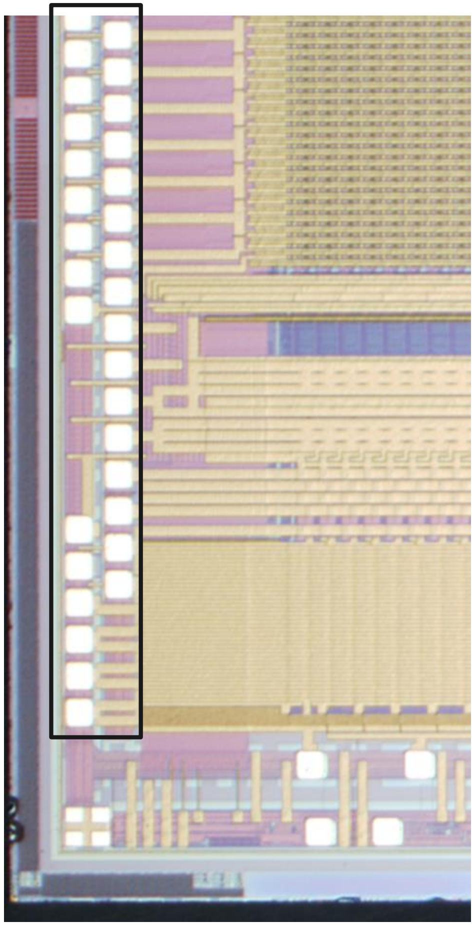
Interconnection technologies

MALTA2 is designed with 32 µm pad gap and 88x88 µm^2 square pads arranged in double rows which makes interconnection challenging.



Evolution of bump size and pitch. Courtesy of T. Tick and S. Vahanen

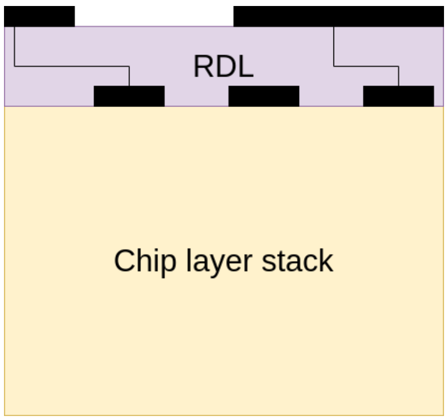
Double rows



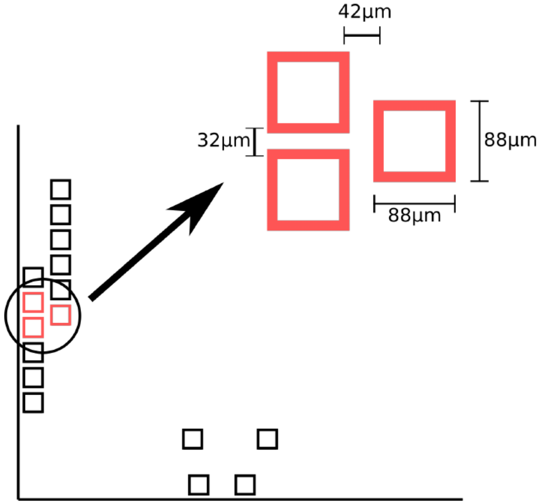
To be able to use commercial low-cost solder processes, a larger pad size and pitch is needed.

MALTA2 Redistribution layer

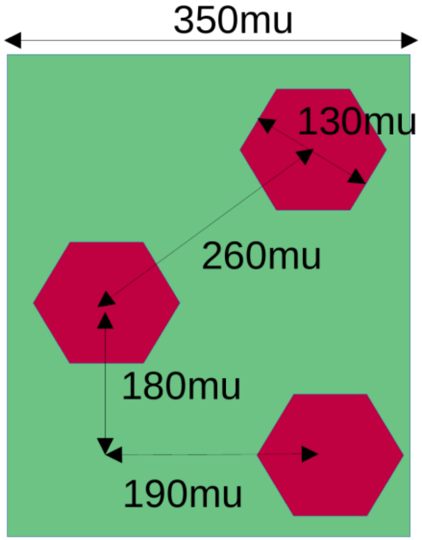
- Present chip pad layout and arrangement is a limitation for many low-cost interconnection technologies
- An RDL (ReDistribution Layer) allows to increase pad size and pitch



Chip with additional RDL



Current pad design



RDL pad design in discussion with Walter Snoeys

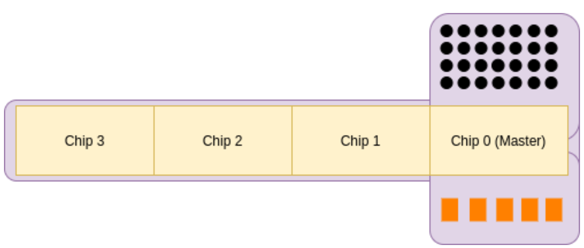
- First evaluation completed and complete design compatible with fabrication ongoing.
- Realization studied in cooperation with TowerJazz and Fraunhofer IZM.

Summary and outlook

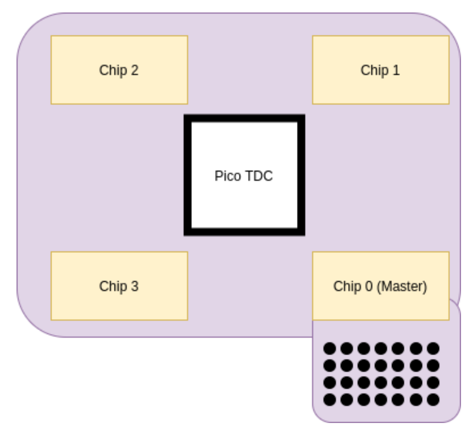
- **Flip chip process** is targeted for packaging modules with MALTA2
- **Flex PCB** demonstrator in **production**
- Evaluation of **ACF and nano wiring** as interconnection technology ongoing
- Development of **redistribution layer** to **simplify** flip-chip packaging ongoing

Outlook:

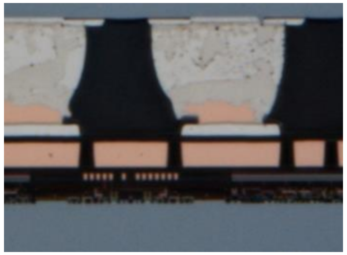
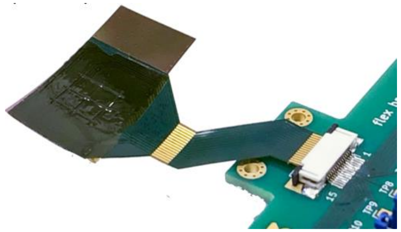
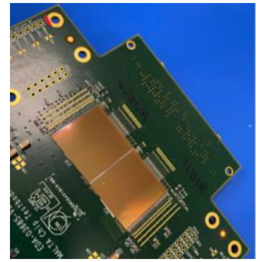
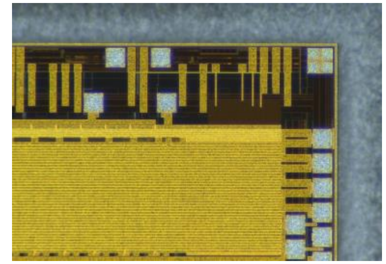
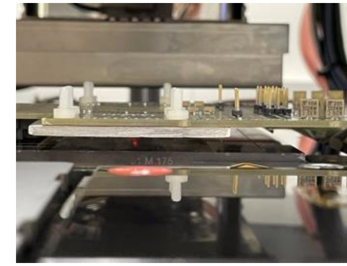
- **Assemble flex PCB** using tested MALTA2 chips and different boding technologies
- **Characterisation** of data transfer, electrical and mechanical characteristics
- **Irradiation tests** on interconnection and modules
- Characterize flex in **test beam**
- **Reflow bonding** using RDL on MALTA2



Dense packaging and **optical signal transmission** demonstration



Timing analysis using **Pico TDC** developed by CERN

EP R&D

Thank you for your attention!