EP R&D

Submissions and Designs in TPSCo ISC 65 nm

Gianluca
On behalf of EP RnD WP1.2 Contributors

Sensor Development Roadmap

EP R&D

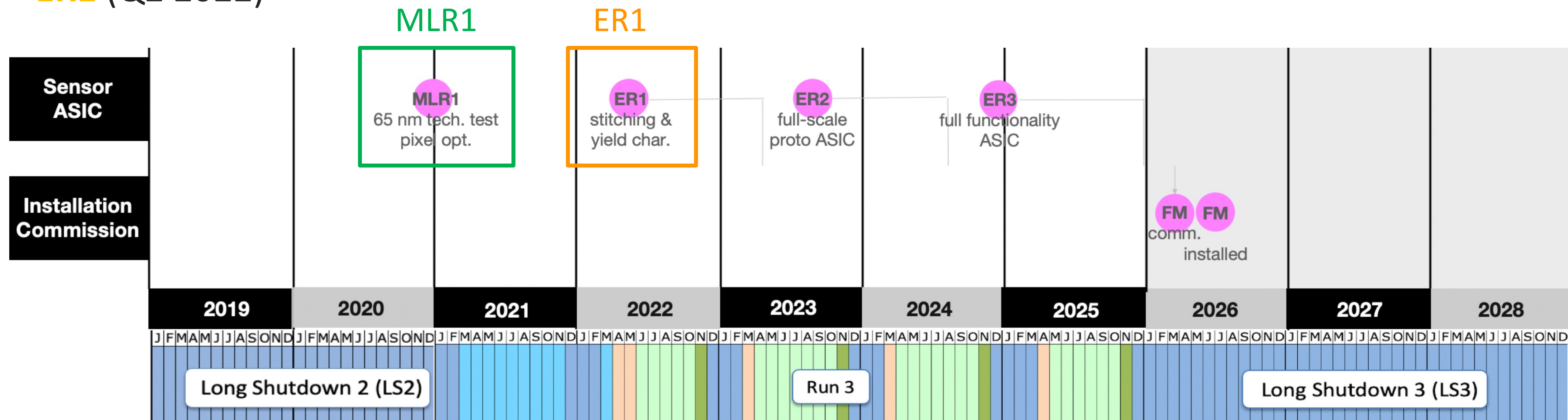
Technology

TPSCo ISC 65 nm CMOS Imaging
300 mm wafers + Stitching

Silicon submissions

MLR1 (Q4 2020)

ER1 (Q2 2022)



MLR1 Submission

EP R&D

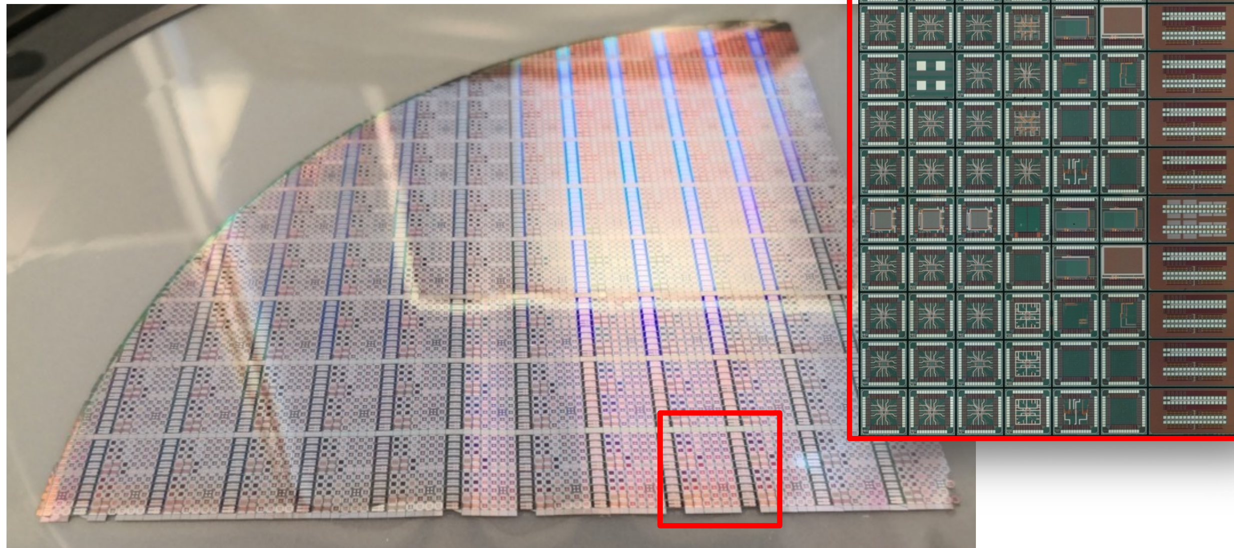
First submission in 65 nm CMOS Imaging, December 2020

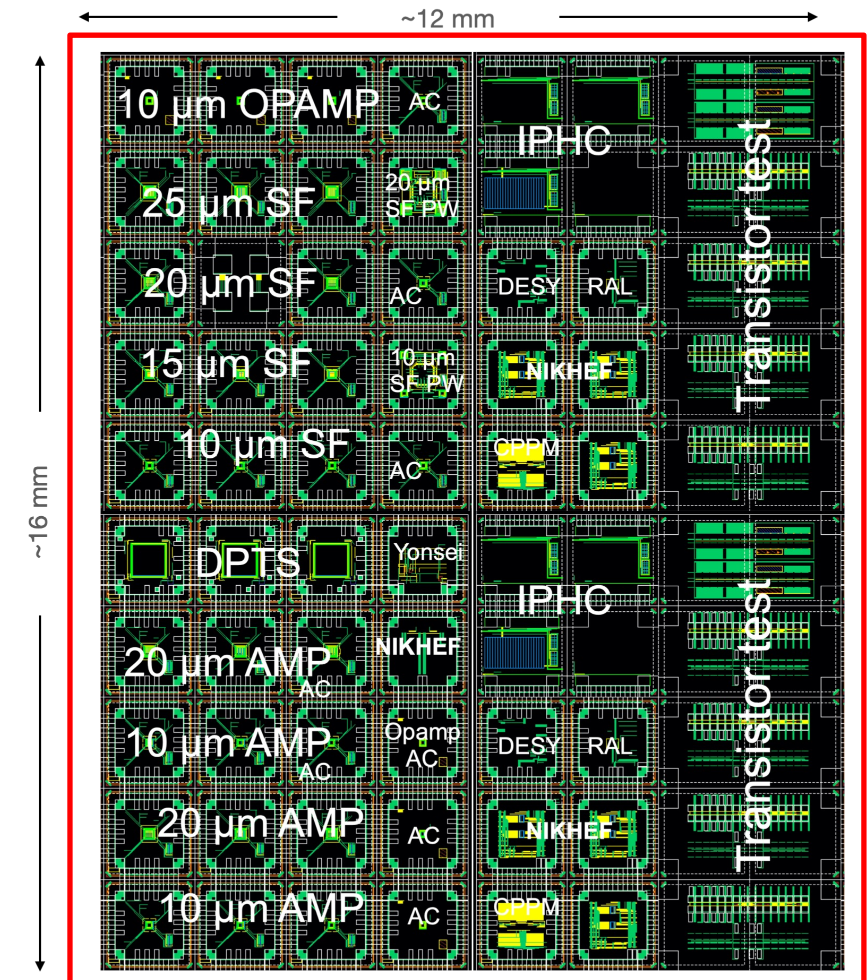
Learn technology features

Characterize devices

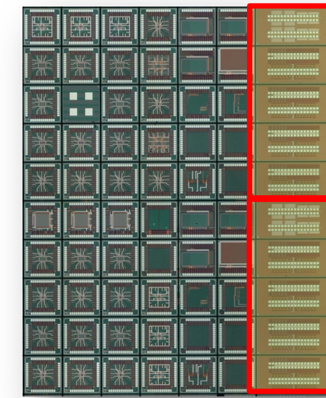
Prototype circuits, blocks and pixel structures

1.5×1.5 mm^2 or 3×1.5 mm^2 test chips





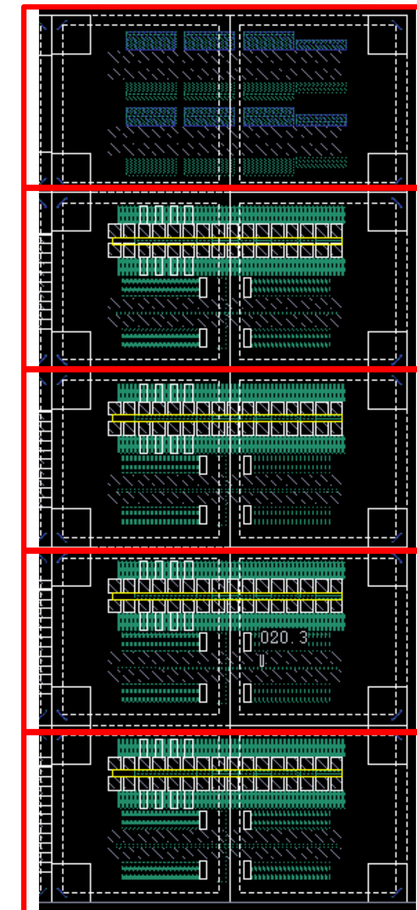
Transistor Test Structures



EP R&D

5 chips with many variants of single transistors

Direct I-V characterization with probe system



Aim

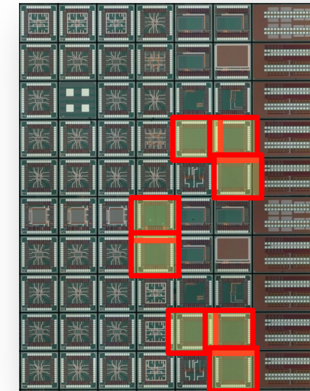
Characterize and verify device response and electrical characteristics with Ionizing Irradiation

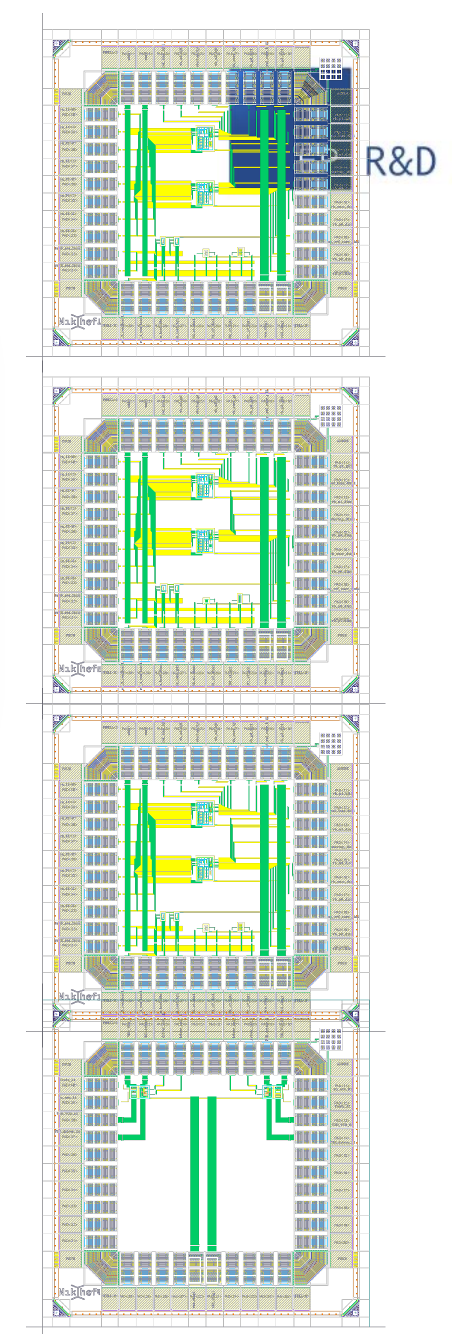
Measure characteristics under different operating conditions, e.g. *after irradiation* and when *reverse biasing* bodies of transistors

Analog Blocks and VCO

Overview

1. Bandgap Reference Prototype, Diode and PNP
2. Bandgap Reference Prototype, DTMOS and diode gated
3. Temperature Sensors Prototypes
4. Voltage Controlled Oscillators Prototypes
5. Amplifier prototype circuits





Aim

Functional and irradiation testing of peripheral analog circuits

Silicon proven Bandgap Reference used in stitched prototypes of ER1
Silicon proven VCO used in 5 GHz PLL prototype in ER1 serializer prototypes
TID tests > 300 Mrad

Ring Oscillators and I/Os

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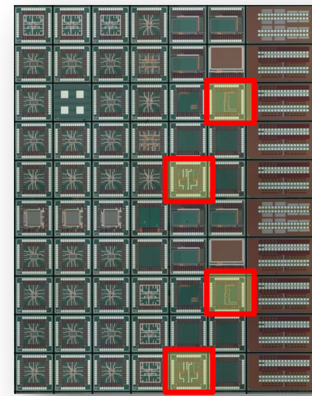
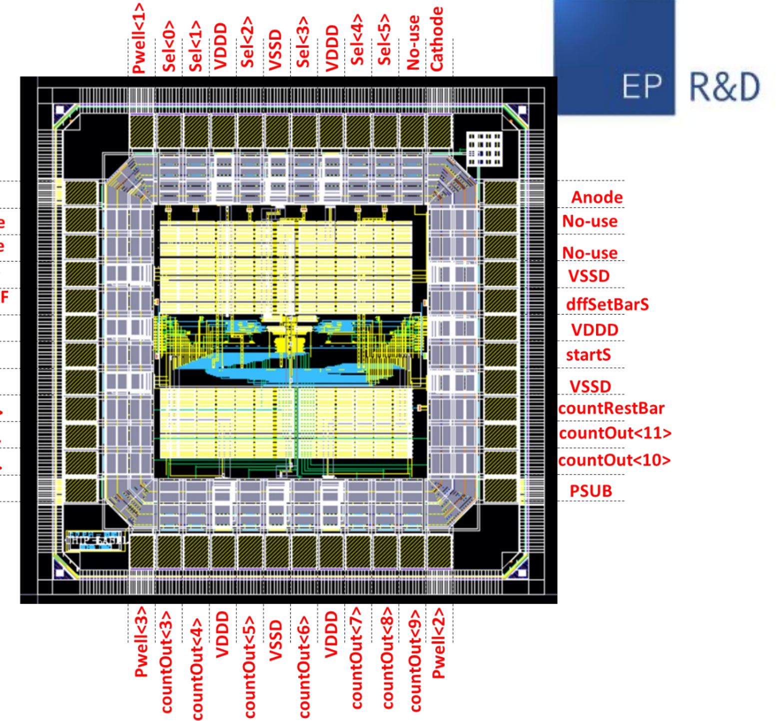




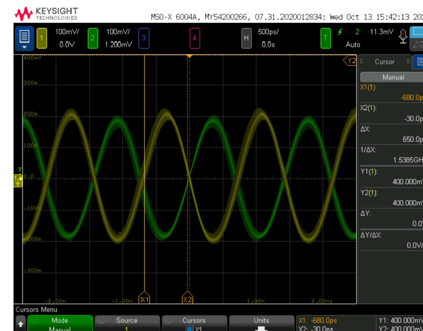
Ring Oscillators

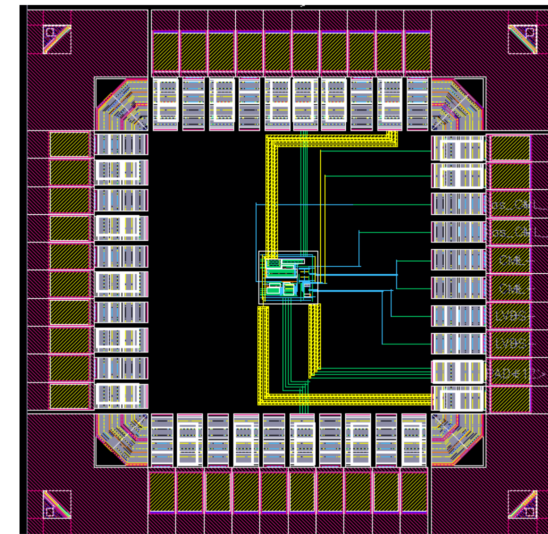
- 24 x 2 ring oscillators
  - Based on different std cells (Inv, Nand, Nor, DFF), different sizes, and two different thresholds
- Aim: test the radiation tolerance of the digital standard cells

TID test >800 Mrad, 12%-15% frequency reduction

Differential I/Os

- High Speed (2 Gb/s) Serial Line Driver
- Differential LVDS Receiver

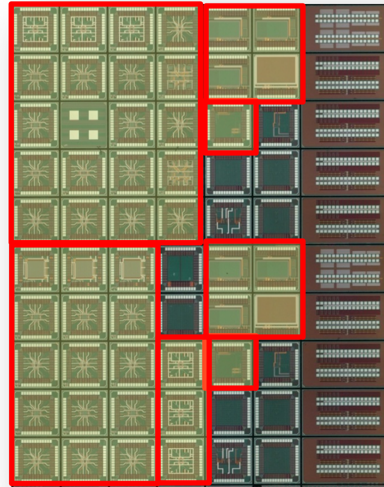




Pixel Prototype Chips

APTS, DPTS, CE65

- Variants of collection diodes
- Variants of Front-End



Front-End prototype

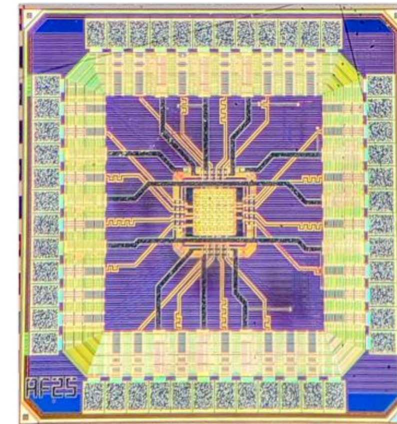
- Charge Shaping Amplifier

Process Optimisation

- Increase margins on sensing performance

Silicon proven pixels and DPTS front-end used as basis for stitched chip sensors in ER1

1.5 mm



APTS

- 4x4 pixel matrix
- 10, 15, 20, 25 µm pitches
- Pixel variants
- Direct analogue readout

DPTS

- 32 ⨯ 32 pixels
- 15 µm pitch
- Asynchronous digital readout
- ToT information

CE65

- 64 ⨯ 32, 15 um pixels
- 48 ⨯ 32, 25 um pixels
- Rolling shutter analog readout
- 3 pixel front-end architectures

Process modifications

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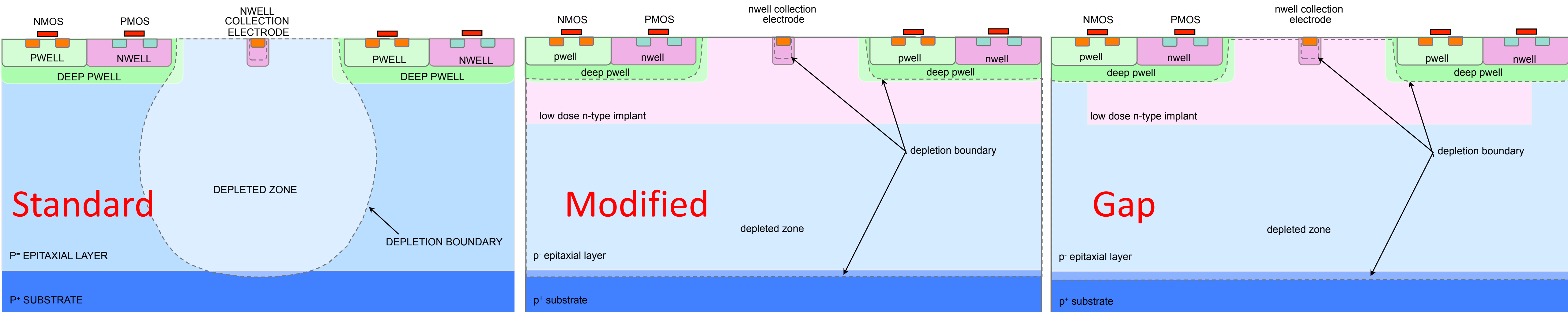
Similar optimization as in 180nm

Implant modifications needed even more in 65 nm for good charge collection



https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed →

← Charge sharing

Executive Summary of MLR1 Test Results

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All chips and pixel prototypes working

Some imperfections and much learning

Transistors Tests Structures

Working as expected and similar to other 65 nm
Technology characterized for HEP

Many building blocks **proven in silicon and tested after irradiation**

Bandgap, DACs, Temperature sensor, VCO, I/Os, Front-ends

Pixel Prototypes

Wealth of results and detailed characterisation ongoing

Process and Sensor layout optimisation

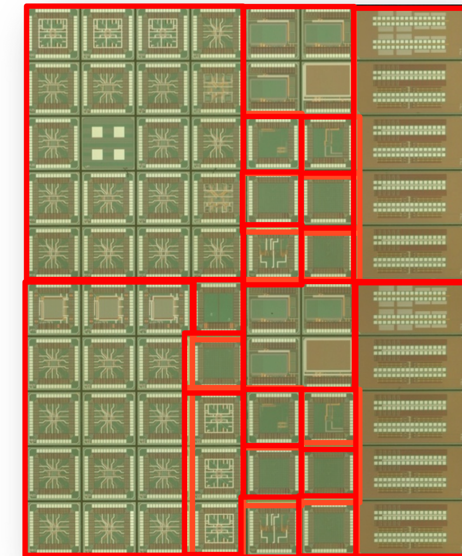
Increased margins on sensor performance and radiation hardness

Validated in TPSCo ISC 65 nm

Reverse Bias

Reduction of input capacitance

Mismatch between measurements and models when transistor bodies are reverse biased outside the nominal range



Towards ER1 – Stitching Interlude

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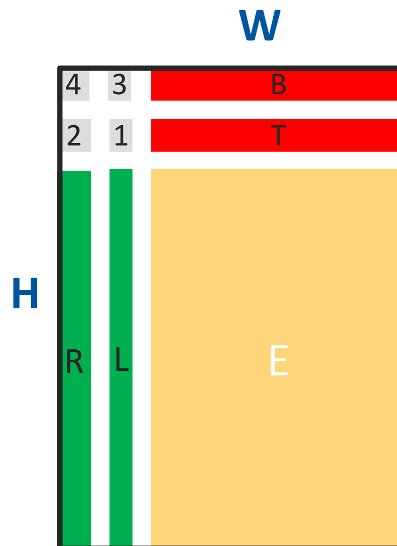
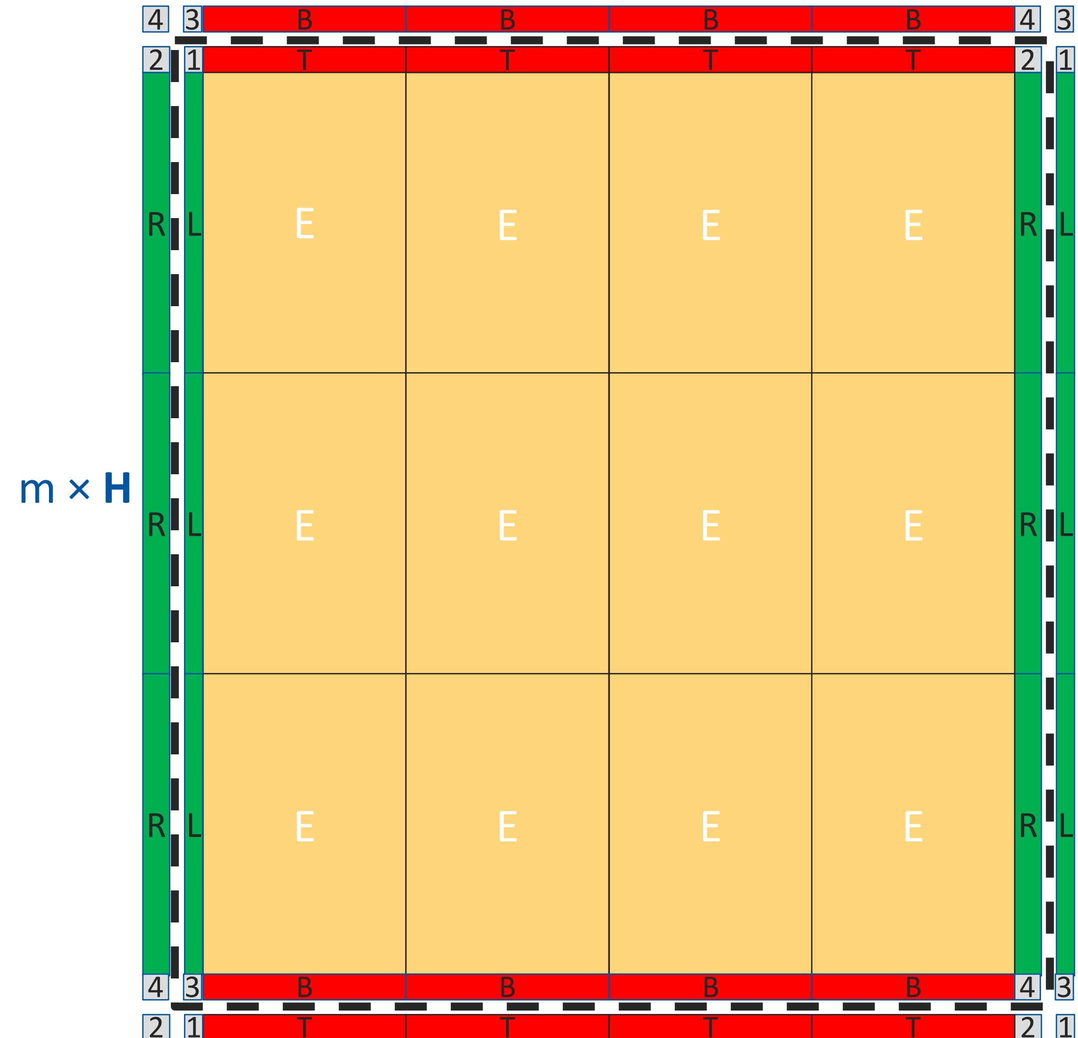
Design Reticle (typ. 2×3 cm)



Circuits on wafer



ER1 Submission

Aim: learn and prove **stitching**

Two large *stitched* sensor chips (MOSS, MOST)

- Different approaches for resilience to manufacturing faults

Small test and development chips

- Pixel Prototypes
- Fast Serial Links

Technology and Support

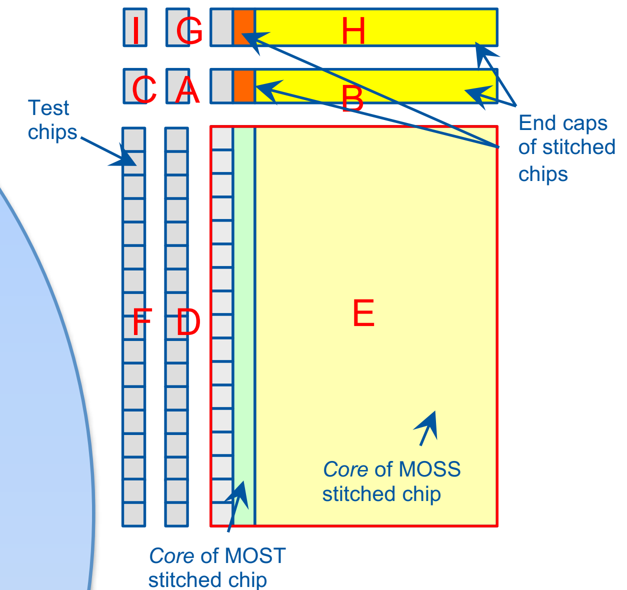
- New metal stack, new I/O libraries, new PDKs

Intense design effort shared by many groups

MOSS (1 of 6)

MOST (1 of 6)

300 mm wafer



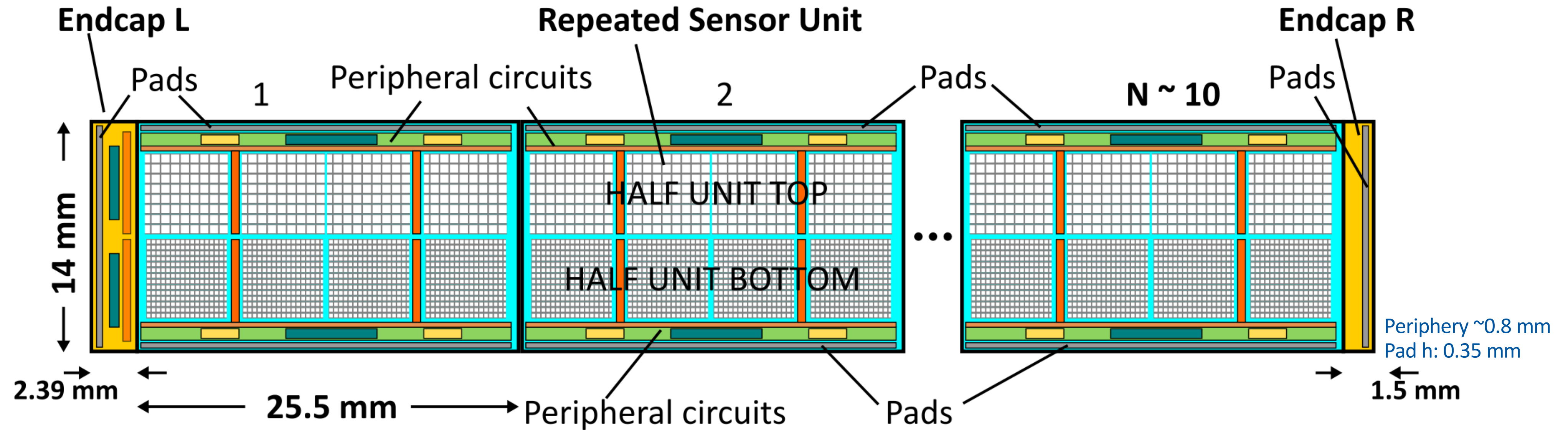
Chips for ER1 submission

EP R&D

Chip	Purpose	Institutes	# of test sites	
MOSS	Stitched sensor prototype. Develop stitching know-how Focus on technology options, power distribution, signal routing, yield	CERN, CCNU, INFN, IPHC, NIKHEF, YONSEI	-	DOING
MOST	Stitched sensor prototype. Develop stitching know-how Study yield with high density layout parts and fine power segmentaton Low power and transmission of timing information over long distance	NIKHEF, IPHC, Heidelberg, CERN, INFN	-	DOING
H2M	MAPS prototype. Port hybrid pixel features to monolithic Investigate MAPS and architectures in non-stitched sensor	CERN, DESY, IFAE	1	DELIVERED (ASSEMBLY AND SIGN-OFF)
CE65v2	Pixel development and optimization vehicle Focus on optimizing pixels and front-end	IPHC	Multiple	DELIVERED (...)
SEU-1, SEU-2	Prototype with memories and flops Measure SEE cross-sections (SEL, SEU)	INFN Bari	2	DELIVERED (...)
LDO, Bandgap	On-chip LDO regulator and analog macro	NIKHEF	1	DELIVERED (...)
PLL , Serializer	Prototype of 10 Gb/s high speed serial transmitter	NIKHEF	2	DELIVERED (...)
PLL, Tx buffer	First blocks for 10 Gb/s high speed transmission	UKRI STFC (RAL)	1	DELIVERED (...)
Pixel test DESY	Pixel sensor and front end prototype	DESY	2	DELIVERED (...)
Pixel test SLAC	Pixel matrix prototype	SLAC	1	DELIVERED (...)
APTS	Analog pixel test structure (re-submission)	CERN, CCNU, IPHC, YONSEI		DELIVERED (...)
DPTS	Digital pixel test structure (re-submission)	CERN, CCNU, YONSEI		DELIVERED (...)
TTS1-5	Transistor test structures (re-submission)	CERN, CCNU		DELIVERED (...)

MOSS Monolithic Stitched Sensor Prototype

EP R&D



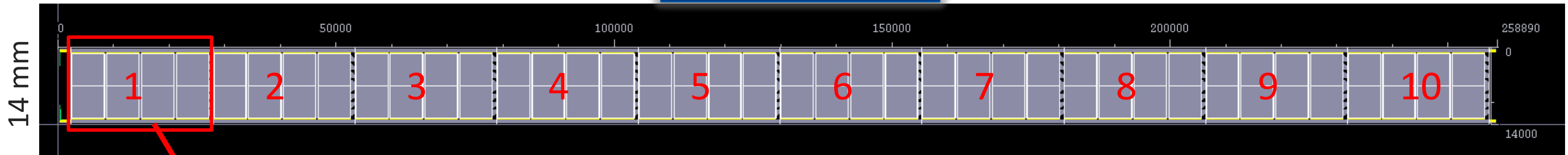
Primary Goals
Learn Stitching technique to make a particle detector
Interconnect power and signals on wafer scale chip
Learn about yield and DFM
Study power, leakage, spread, noise, speed

Repeated units abutting on short edges

- Functionally independent
- Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

MOSS layout snapshots

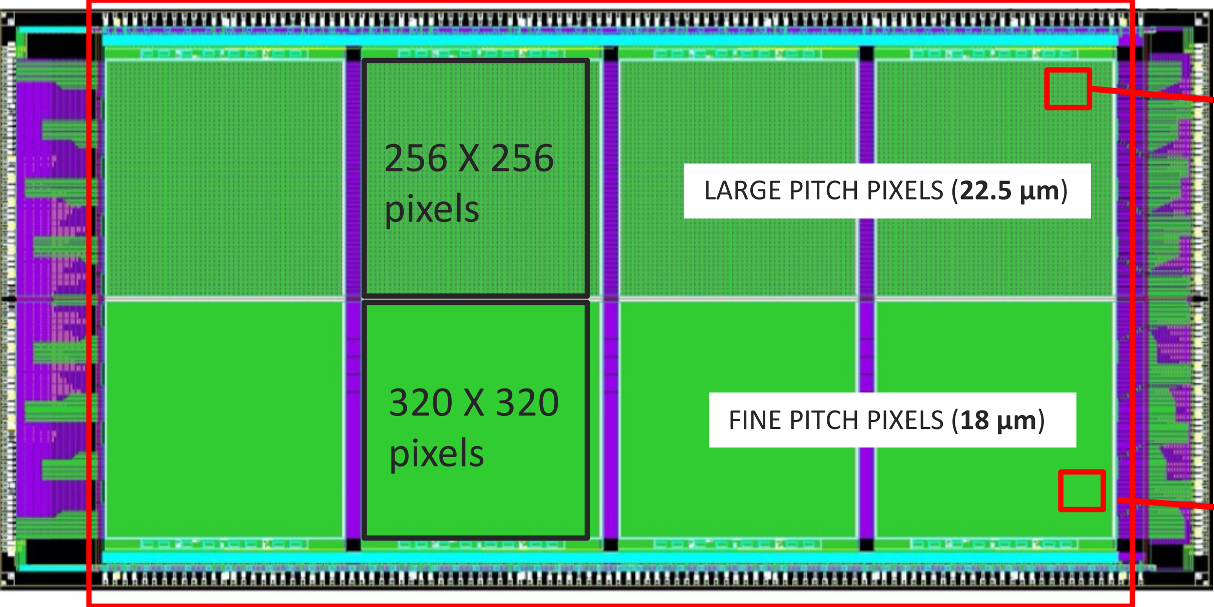
6.72 Mpixels

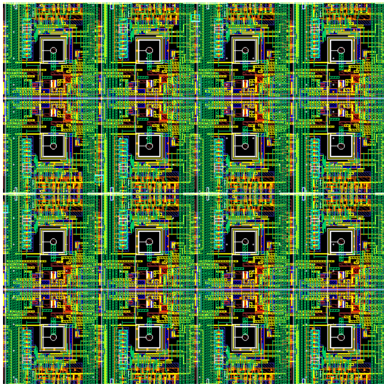


14 mm

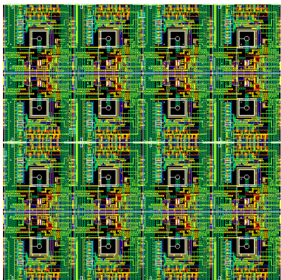
25.9 cm

1 of 10





Pitch
22.5 µm



Pitch
18 µm

MOST chip

Investigate yield when local density is preserved

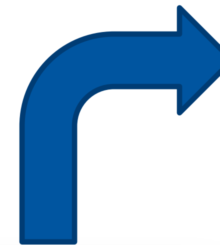
- Global power domains over full chip (Digital/Analog)
- Power gating with high granularity to mitigate defects

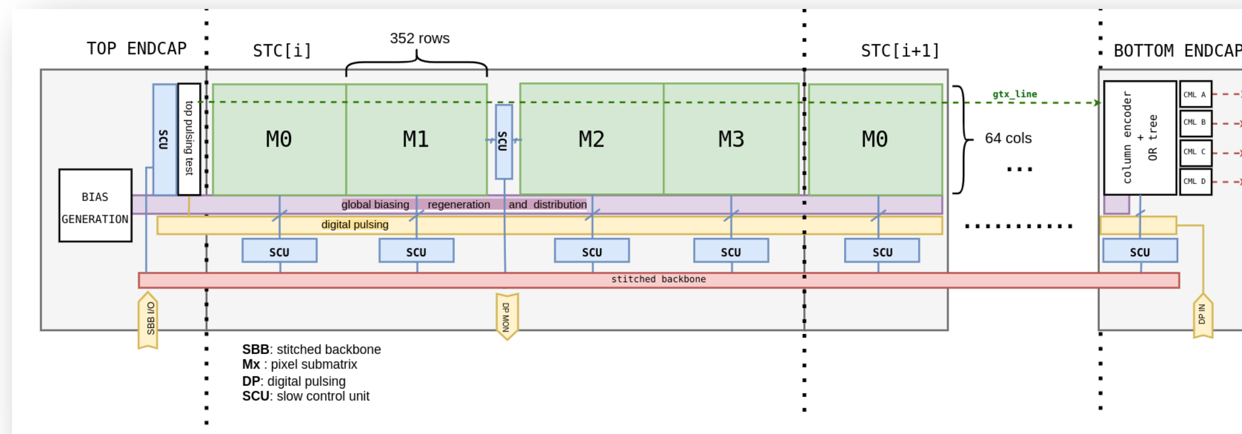
Larger sensor bias achieved by higher power supply

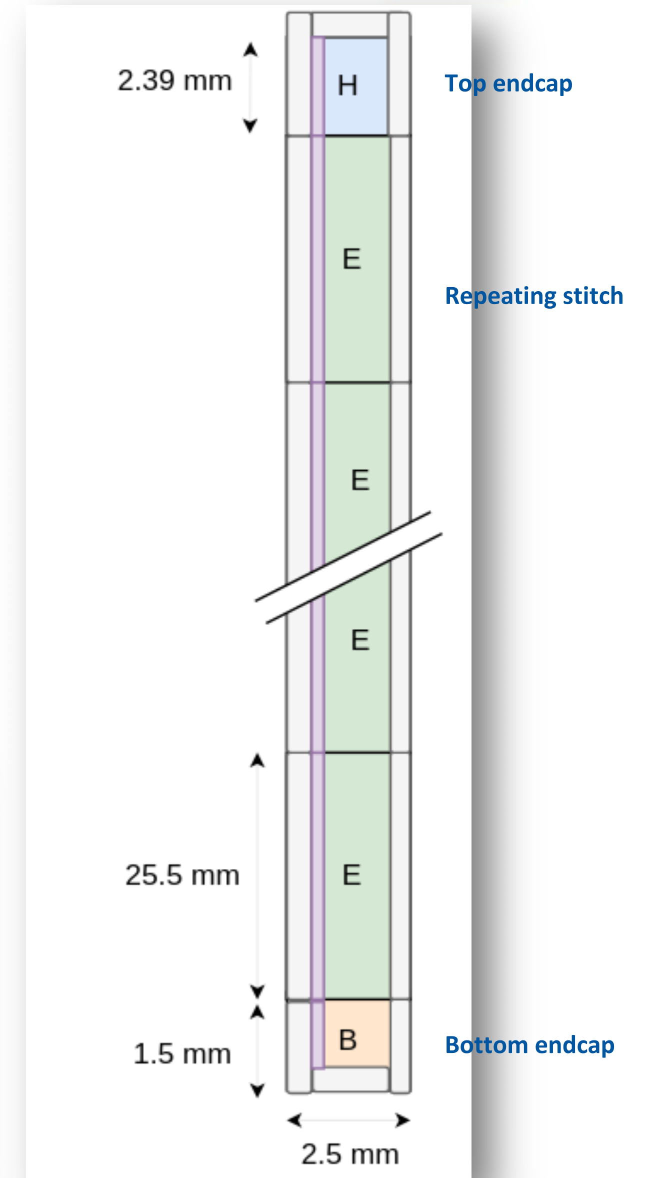
- PWELL tied to ground

Event-driven asynchronous readout

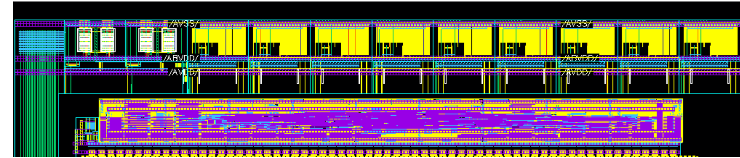
- No global shutter/strobe
- Immediate transmission of hit data over long distance to the periphery
- 4 CML outputs in the bottom endcap

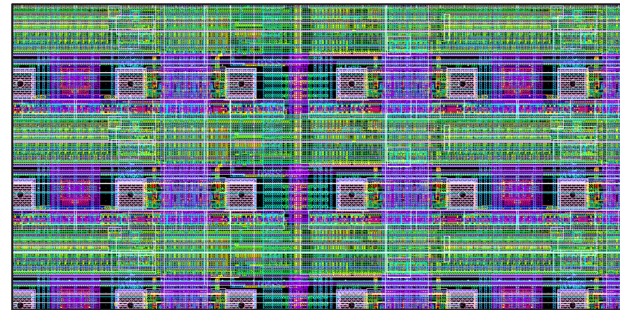


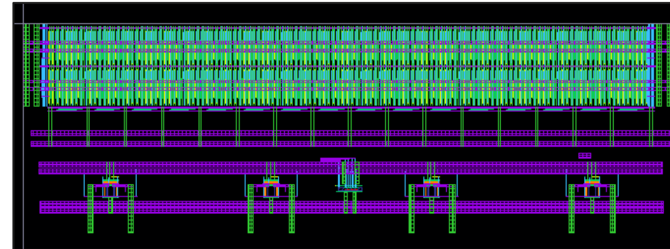


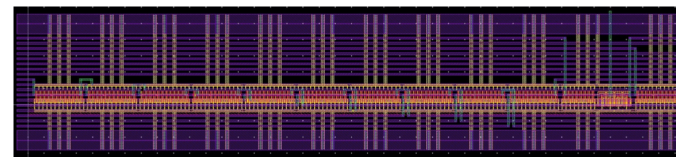


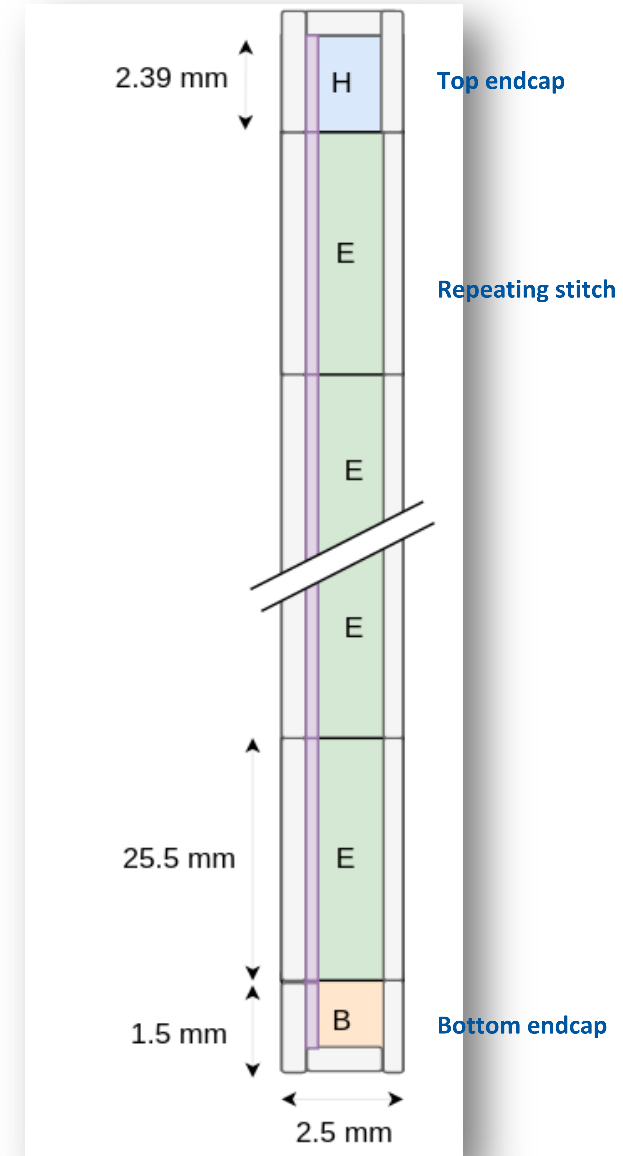
MOST layout snapshots


Detail of the top periphery (biasing generation, slow control, test pulsing)


Detail of the pixel matrix


Detail of the bottom periphery core with the 4 CML outputs


Detail of the stitched backbone buffers



H2M Hybrid to Monolithic

EP R&D

3×1.5 mm^2 chip, 64x16 pixel array, 35 um pitch

Port a hybrid pixel architecture into monolithic process

Prototyping front-end, compact digital library, peripheral blocks, differential I/Os

H2M (Hybrid-to-Monolithic) design

- Development aims:
  - Digital-on-top design flow and methodology
  - Design and testing of a compact digital cell library
  - Porting a hybrid pixel architecture into a monolithic process
  - Compare the system level behaviour with the hybrid embodiment
  - Optimising interconnect and mechanical schemes to minimise the cost per unit area
- The H2M chip:
  - 3 x 1.5 mm^2 chip
  - 64 x 16 square pixels
  - 35 µm pixel pitch
  - 8-bit counter per pixel
  - 4 acquisition modes:
    - Time of Arrival (ToA)
    - Time over Threshold (ToT)
    - Photon counting
    - Triggered binary readout, with configurable strip length

Collection electrode, CSA, discriminator, threshold tuning DAC

8-bit counter, programmable in 4 acquisition modes, synchronising logic, per pixel configuration

35 µm

Column [0]

Front-end

Digital logic

35 µm

64 columns

16 pixels per column

Column [63]

Pixel

Interface between pixels and periphery

1.50 mm

EoC

EoC

Digital periphery (Slow control + readout logic)

Analog periphery (Bandgap + Biasing DACs + unity gain buffers)

Differential-to-CMOS receivers / drivers

I/Os

3.00 mm

iraklis.kremastiotis@cern.ch 2

CE65v2 Pixel Chips

EP R&D

Versatile Pixel Exploratory Chip

Optimization of charge collection node

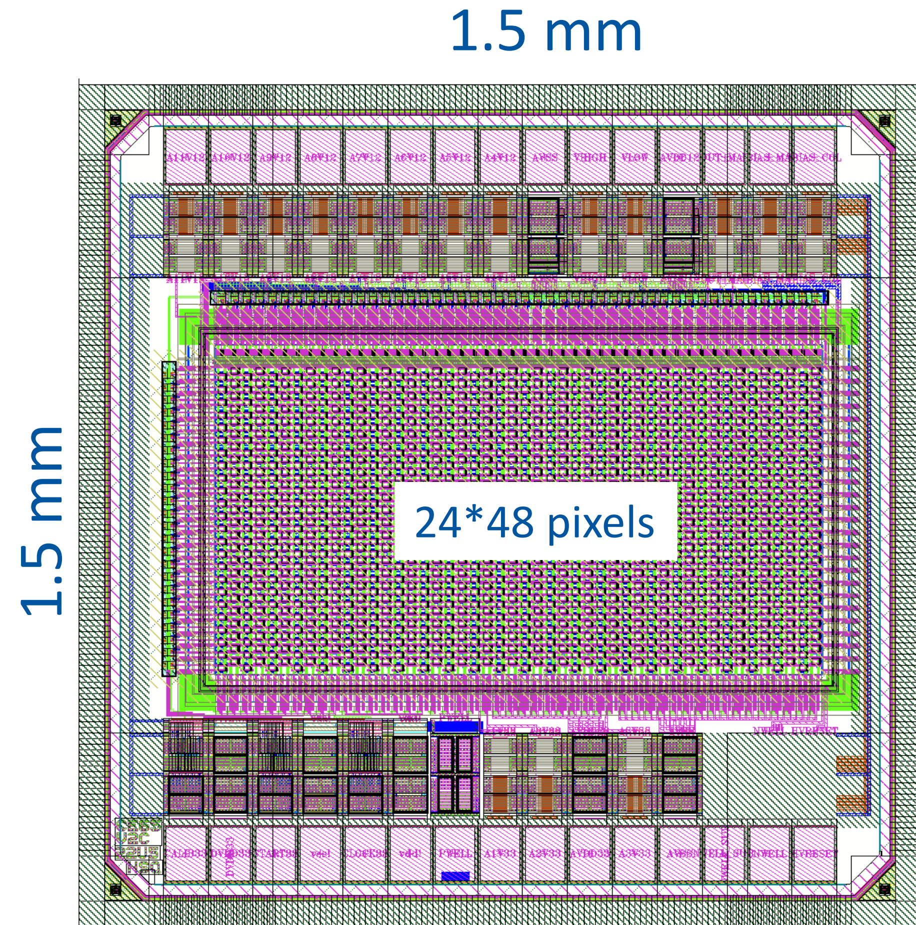
For lab and beam tests

Variants of pixels pitch and geometry

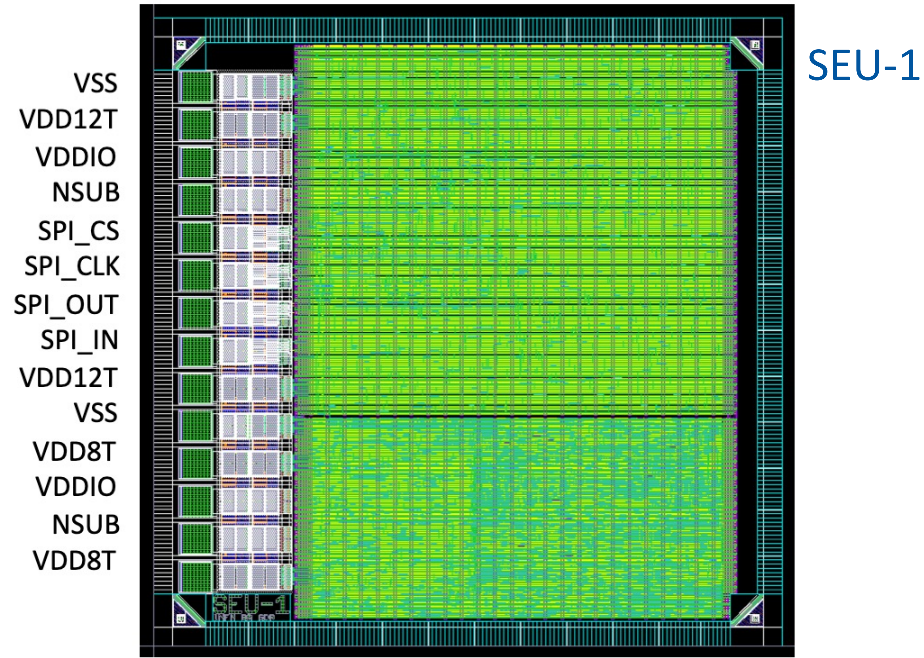
15, 18, 22.5, 18_{hexsq}, 22.5_{hexsq}

Rolling Shutter Readout

Single Multiplexed Analog Output



SEU Test Chips – SEU-1, SEU-2

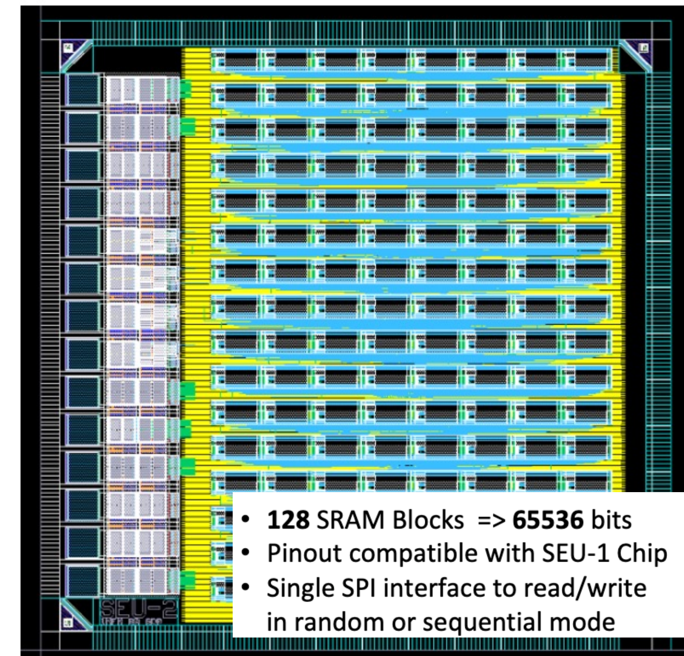


- DIE Size: 1.5 mm x 1.5 mm
- Core Area: 990 um x 1368 um (1.354 mm2)
- 90 um Bonding pitch

5 shift registers containing **10624** Flip-Flops of each of the types:

Library	Cell
Tower 12T LVT	D Flip-Flops with Q Output Only
Tower 12T LVT	D Flip-Flops with Set and Clear
Tower 12T LVT	Multiplexed Scan D Flip-Flops with Q Output Only
CERN 8T LVT	D Flip-Flops with Q Output Only
CERN 8T LVT	D Flip-Flops with Set and Clear

SEU-2



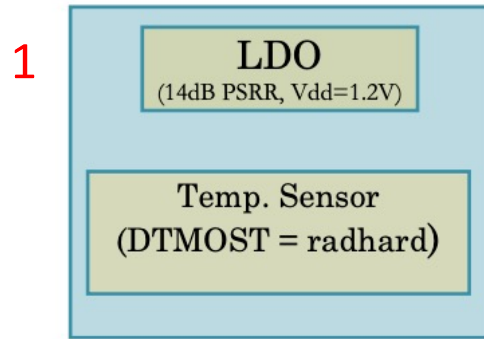
PLL, LDO, Temp Sens, High Speed TX

NWO Netherlands Organisation for Scientific Research

Test chips to be prepared for the MLR2 (ER1) submission

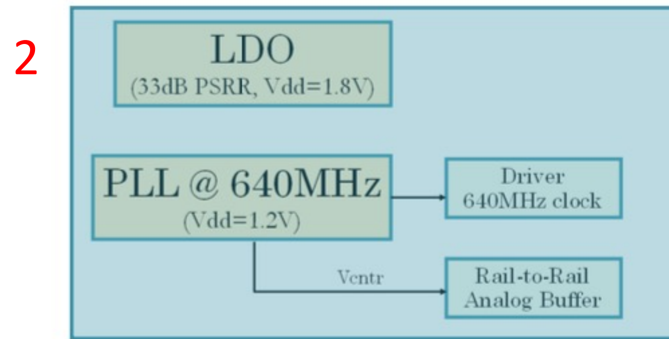
Test chip1: (to be completed in February 2022)

1



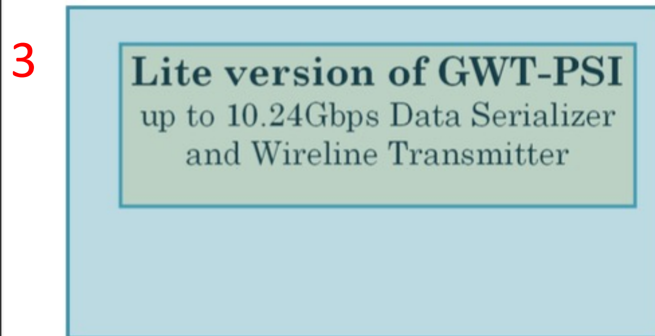
Test chip2: (completed in December 2021)

2



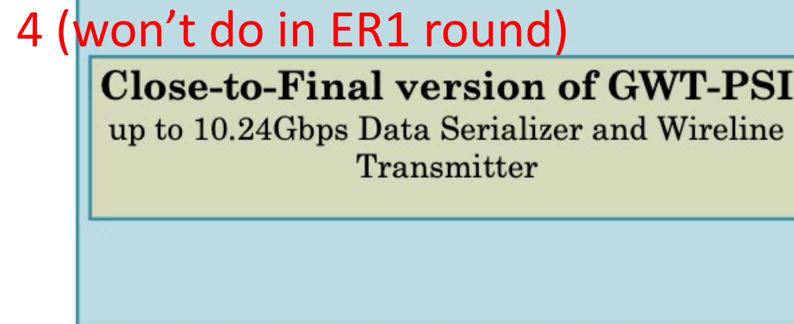
Test chip 3: (in progress)

3



Test chip 4: (under consideration)

4 (won't do in ER1 round)



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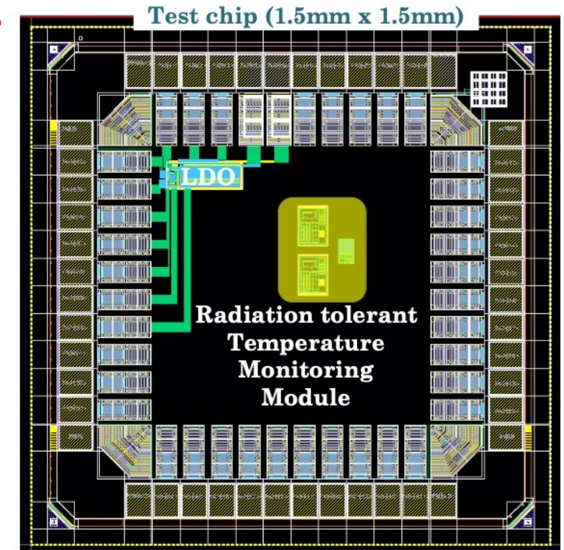
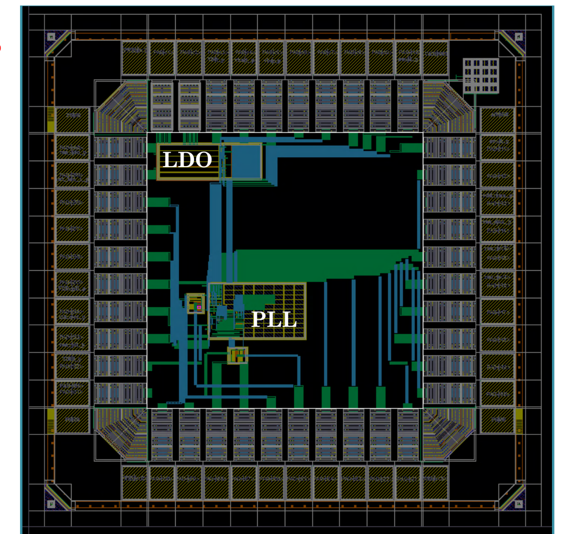
1



2



Prototype PLL, Differential I/Os, Digital Blocks

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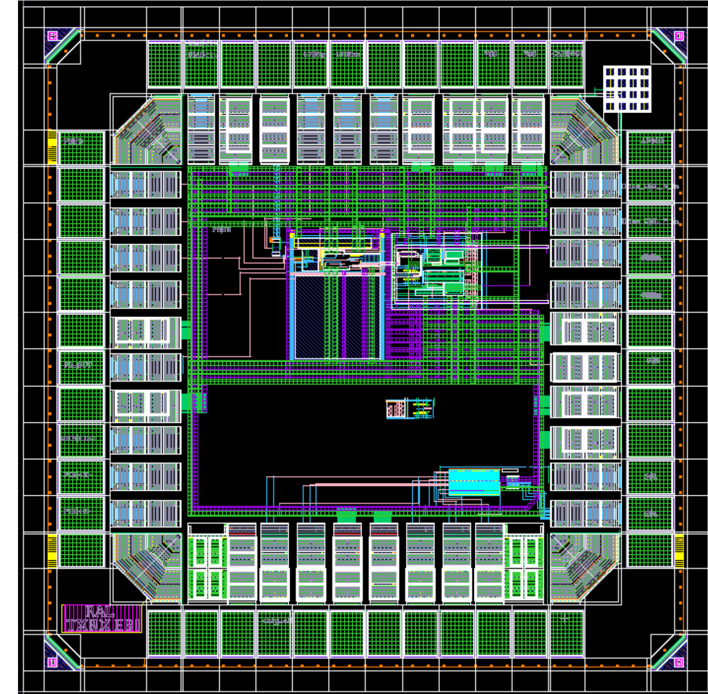
Dual mode 10 GHz PLL

CML driver

PRBS Generator, I2C interface block



UKRI Science and Technology Facilities Council

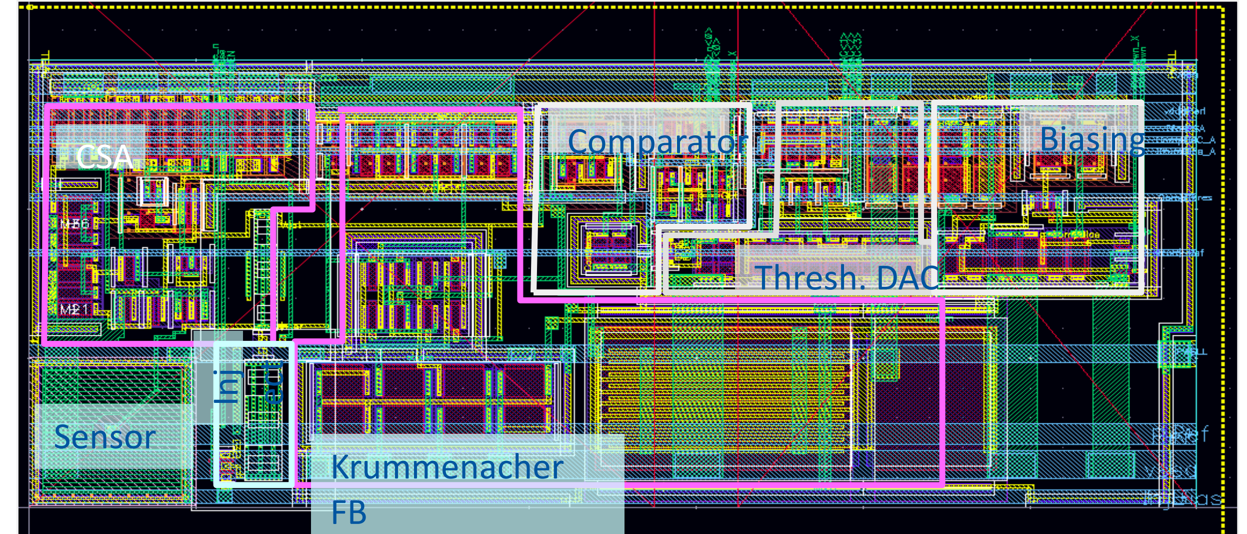
CSA Front-End Prototypes

EP R&D

Front-End for H2M chip

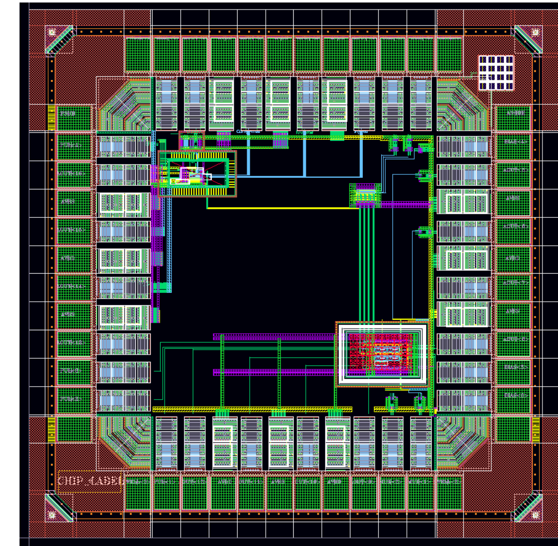
Evolution of *MLR1 CSA prototype*

Charge Shaping Amplifier, Krummenacher FB, Comparator, Threshold DAC



Front-End Prototype Chip

Analog CSA FE and 4×4 pixel matrices



Standard Cell Modification for DFM

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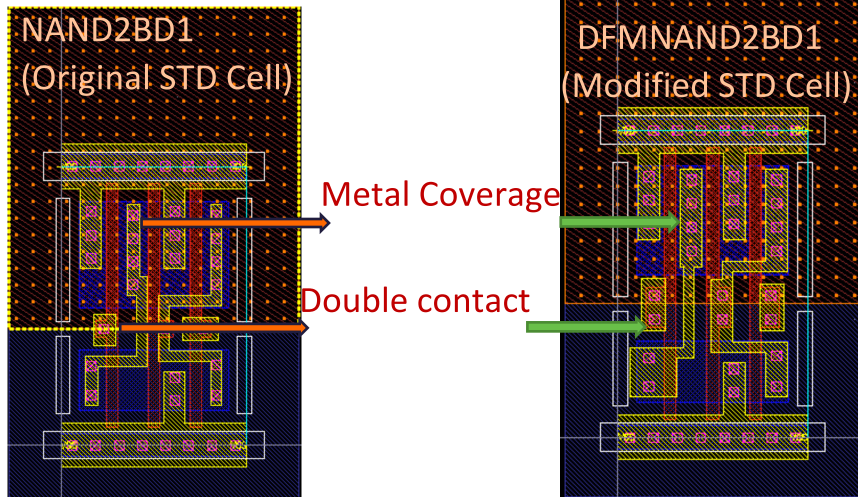
Modification of the layout of 50 Standard Cells

- Respect Design For Manufacturability, Yield Enhancement rules
- Mitigate the impact of manufacturing faults
- Cells to be used in MOSS and MOST stitched designs

Joint Effort RAL, IPHC, INFN, CERN



Function	Description	Cell name
TIE CELL	Tie cell	DFMTIEH
		DFMTIEL
ANTENNA	Antenna diode	DFMANT3
DECOUP	Decoupling	DFMFILLER9C
		DFMFILLER10C
		DFMFILLER20C
FILLER	Filler cell	DFMFILLER1
		DFMFILLER2
		DFMFILLER3
		DFMFILLER4
		DFMFILLER5
		DFMFILLER8
		DFMFILLER16
		DFMFILLER30
ENDCAP	End Cap cell	DFMGDMY

Function	Description	Cell name
BUFFERS	Inverting Buffers	DFMINVD1
		DFMINVD2
		DFMINVD4
		DFMINVD8
BUFFERS	Non-Inverting Buffers	DFMBUFD1
		DFMBUFD2
DELAY BUFFERS	1X Delay	DFMDL01D1
	2X Delay	DFMDL02D1
CLOCK	Buffers	DFMCLKBUFD1
		DFMCLKBUFD16A
		DFMCLKBUFD4
		DFMCLKBUFD8
CLOCK	Inverters	DFMCLKINVD1
		DFMCLKINVD16A
		DFMCLKINVD2
		DFMCLKINVD4
		DFMCLKINVD8
CLOCK	2-Input NAND	DFMCLKNAND2D4
CLOCK-GATING	Latch Based Clock Gating Cells	DFMGCLRD4
GATES	Logic Functions	DFMAND2D1
		DFMAOI22D1
		DFMNAND2BD1
		DFMNAND2D1
		DFMNOR2BD1
		DFMNOR2D1
		DFMOAI22D1
		DFMOR2D1
		DFMXOR2D1
GATES	2-to-1 Multiplexers with Inverted Output	DFMMXI2D1
FLIP-FLOPS	D Flip-Flops with Q Output Only	DFMDFFHQD1
		DFMDFFHQD4
	D Flip-Flops with Clear and Q Output Only	DFMDFFRHQD1
		DFMDFFRHQD4
LATCHES	Latches with Active-High Enable	DFMLAHD1
		DFMLAHSD1

Summary

EP R&D

MLR1 submission

- Large variety of prototype circuits and pixel arrays
- Building blocks proven in silicon, being utilized in ER1 designs
- Post-irradiation tests
- Acknowledgement and credits to many designers and scientists working on the characterization

ER1 submission

- Smaller prototype chips completed
- Working to close designs of stitched sensors (MOSS/MOST)
- Internal full wafer GDS file assembly ongoing

Selection of MLR1 results in the following presentation by Magnus