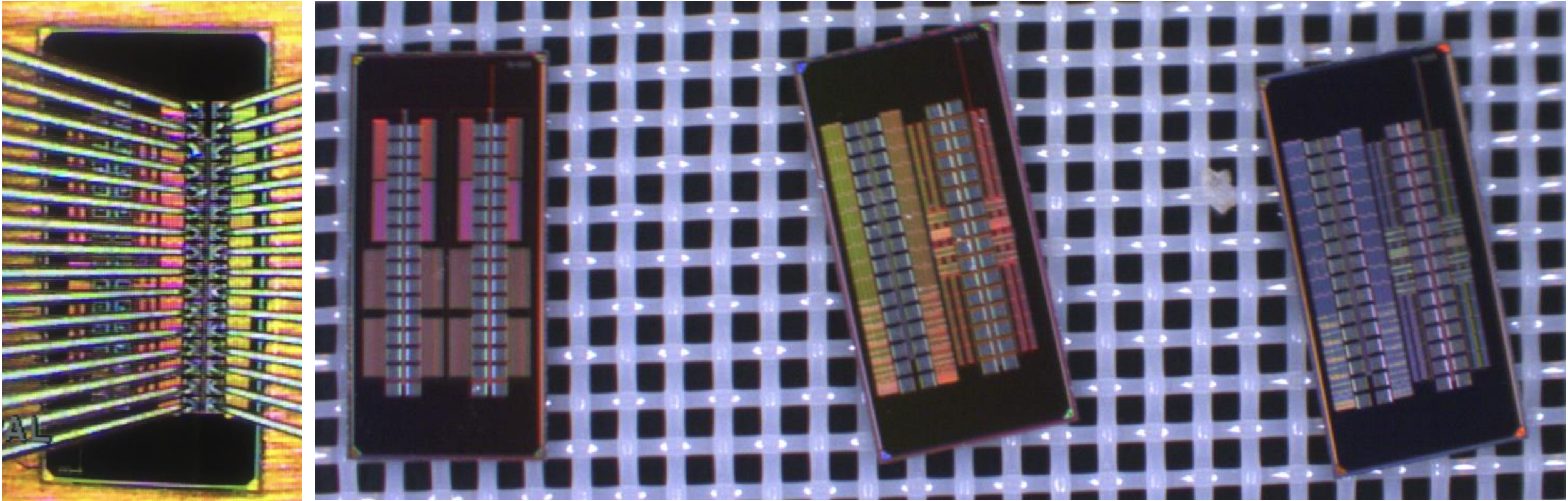


MEASUREMENTS

Transistor measurements

Giulio Borghello, Wenjing Deng, Ana Dorda Martin, Geun Hee Hong, Gennaro Termo

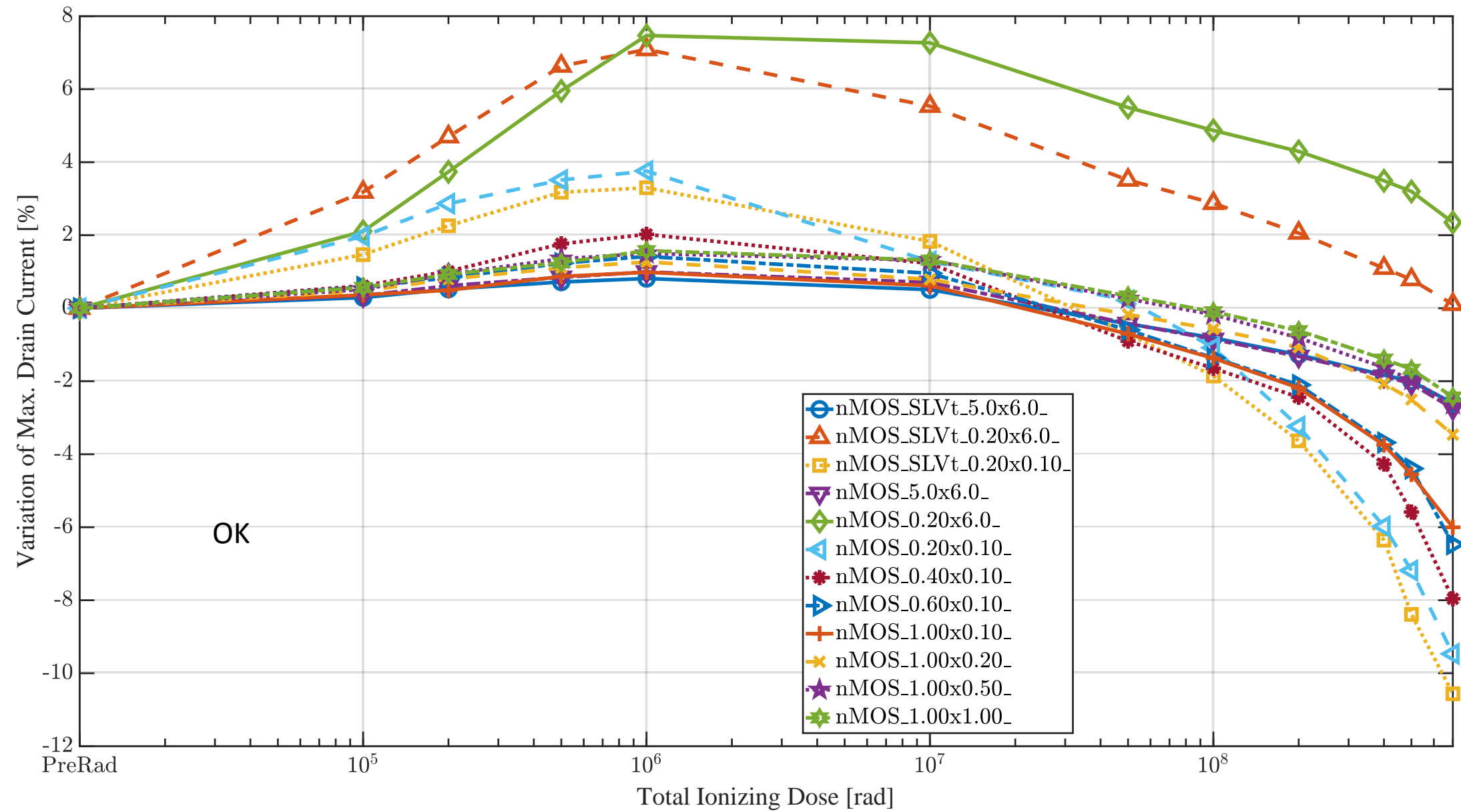


5 test chips

- 4 traditional transistor test structures with different transistor flavors
- 1 gate leakage test structure

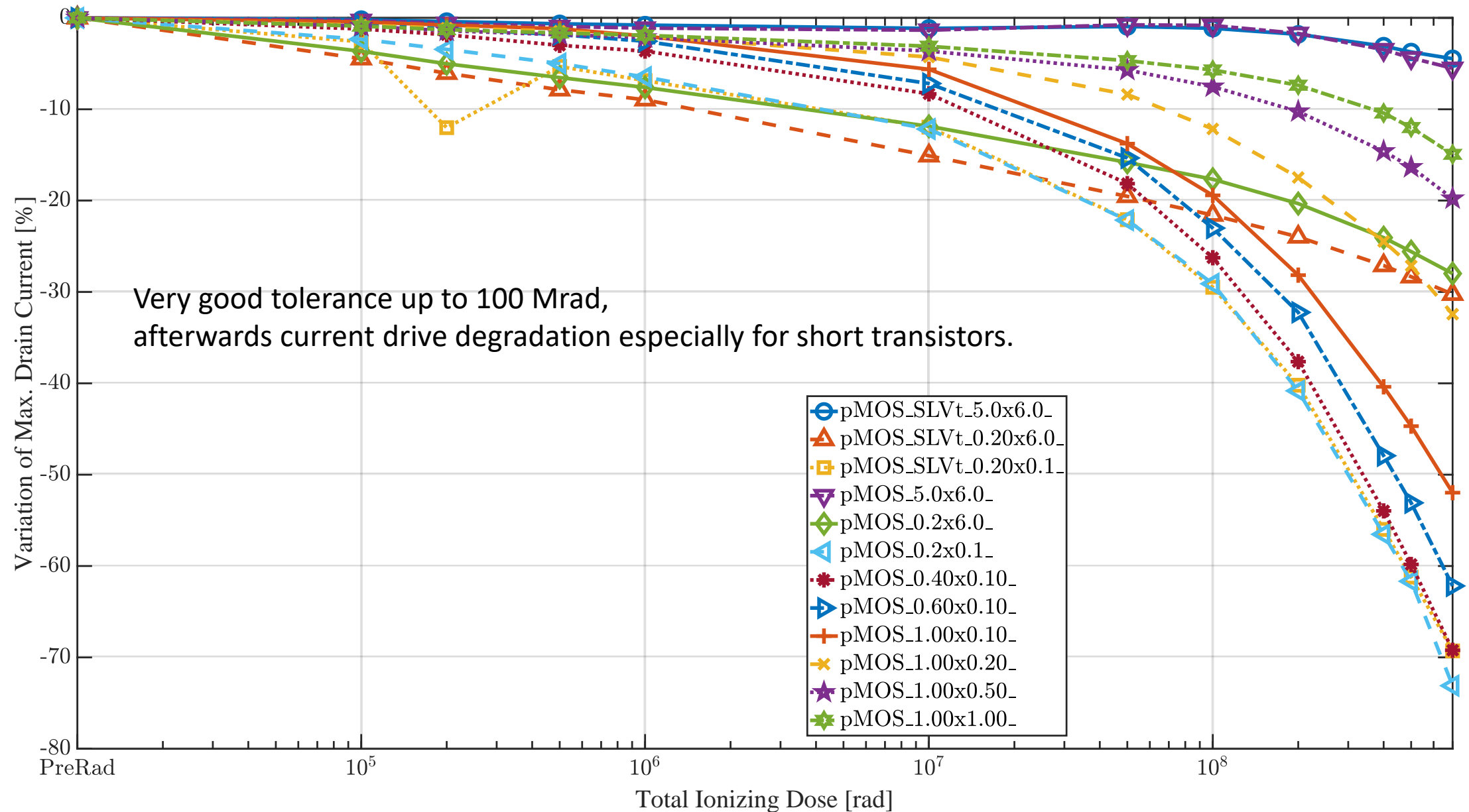
1.2 NMOS transistor 10keV X-ray irradiation measurements

Giulio Borghello, Wenjing Deng, Ana Dorda Martin, Geun Hee Hong, Gennaro Termo



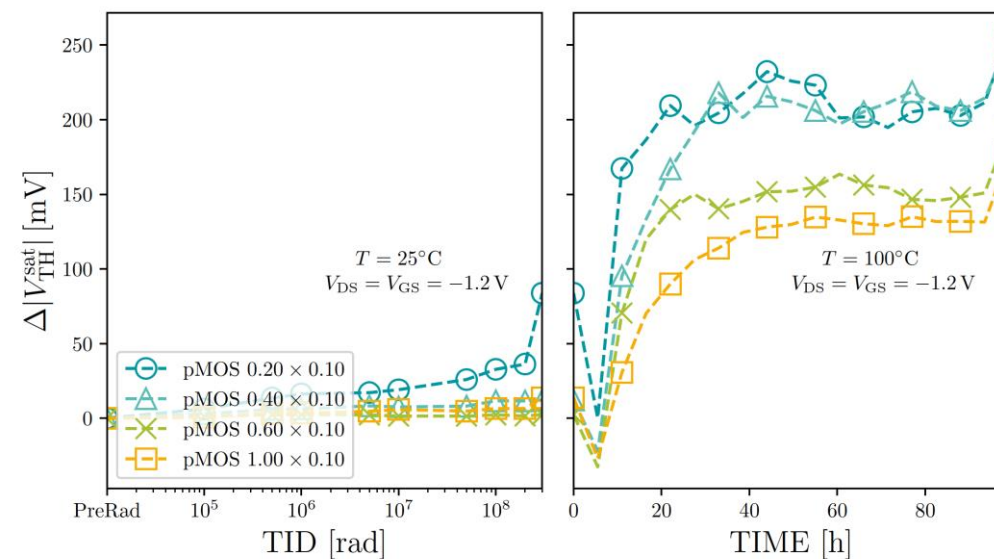
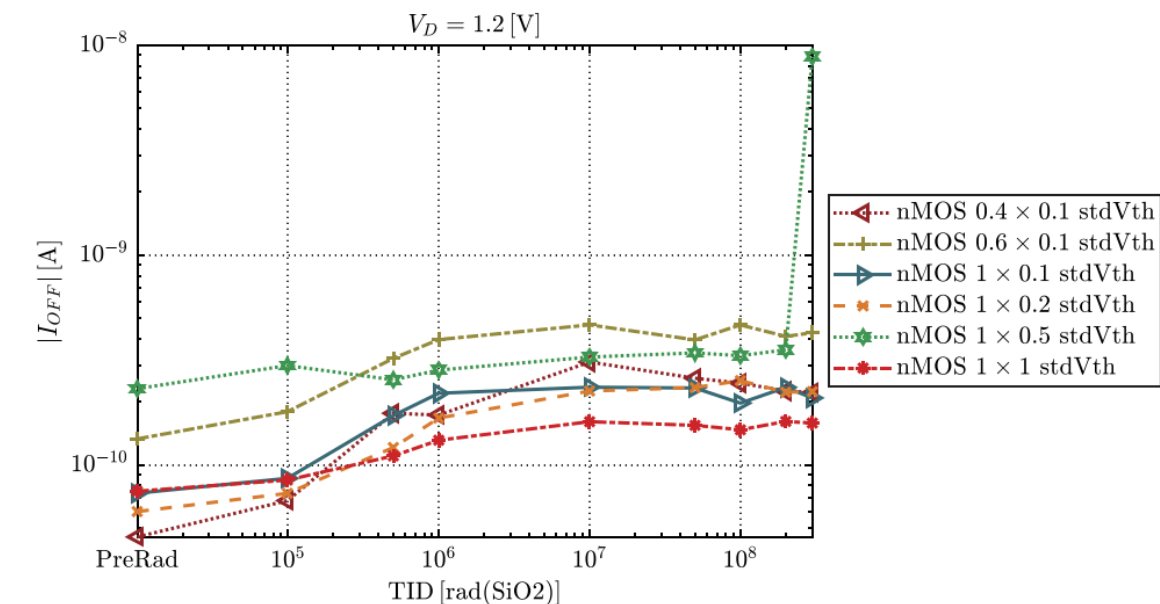
1.2 V PMOS transistor 10keV X-ray irradiation measurements

Giulio Borghello, Wenjing Deng, Ana Dorda Martin, Geun Hee Hong, Gennaro Terzo



Summary transistor 10keV X-ray irradiation measurements

Giulio Borghello, Wenjing Deng, Ana Dorda Martin, Geun Hee Hong, Gennaro Termo



Irradiation measurements

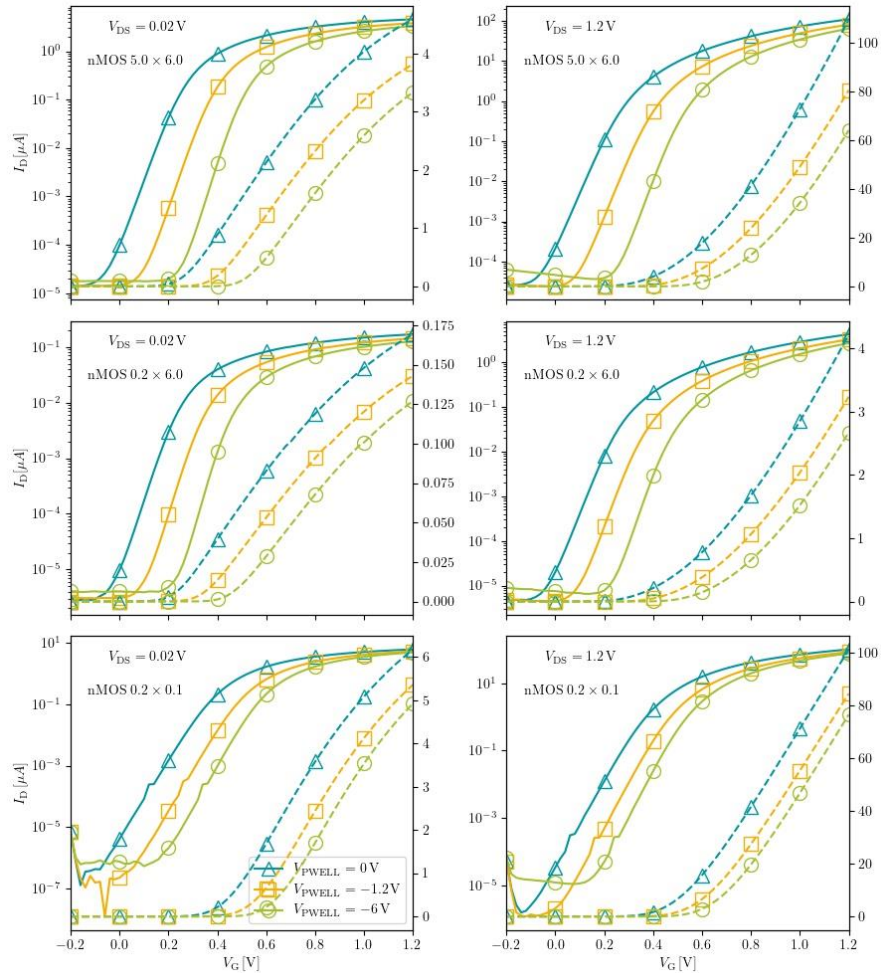
- 1.2 V NMOS transistors OK up to 1Grad, leakage increase less than an order of magnitude for $W > 600$ nm
- 1.2 V PMOS transistors OK up to 100 Mrad, beyond severe current degradation especially for short transistors
- Thicker oxide transistors some what weaker, according to oxide thickness
- Special cases, eg ~ 200 mV threshold shift during post-rad anneal for very narrow PMOS transistors
- In general in line with other 65 nm technologies

Special modeling study

- Observing deviation of V_{th} between model and experiment for reverse substrate biases larger than 1.2 V (not within 'normal' transistor operating range). Detailed study ongoing

Bulk bias measurements

Ana Dorda Martin

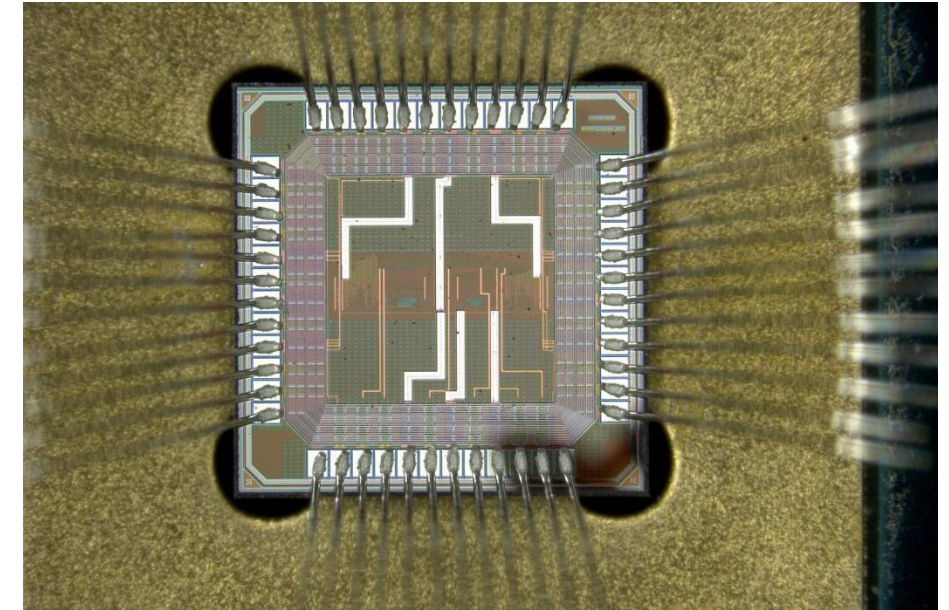
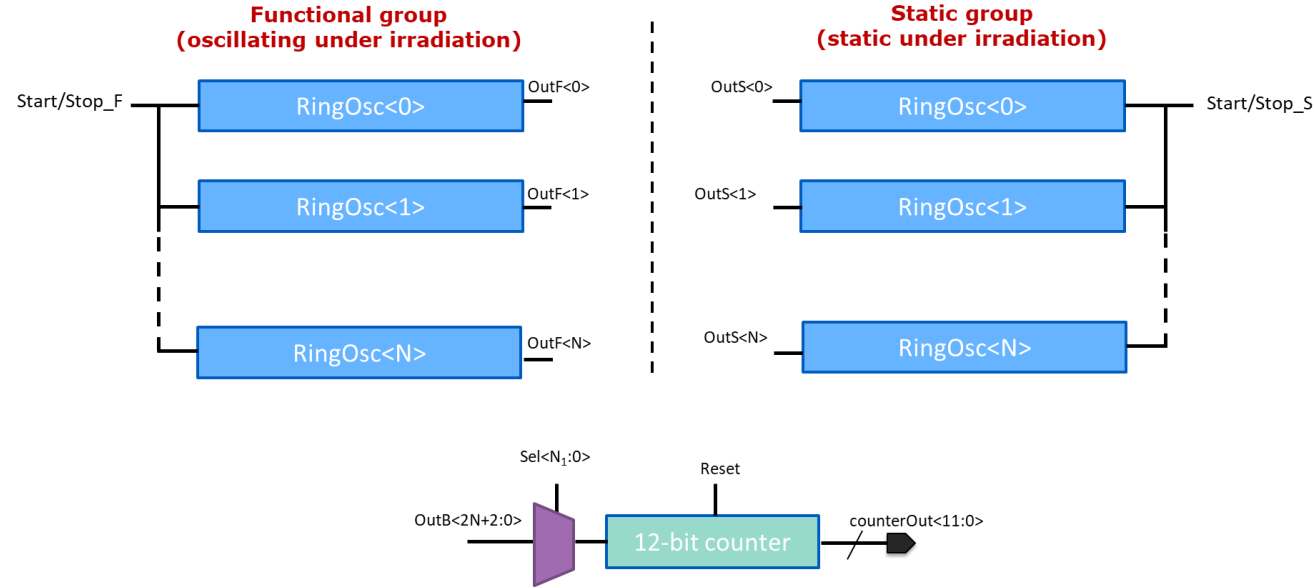


- Preliminary measurements of VTH shows a variation up to +260 mV (@ VPWELL = -6 V) with respect to nominal (@ VPWELL = 0 V).
- Relation with transistor size is under study.

Transistor	VPWELL [V]	VTH_lin [mV]	VAR_VTH_lin [mV]	VTH_sat [mV]	VAR_VTH_sat [mV]
nMOS_5.0x6.0	0	259.9	-	223.4	-
	-1.2	389.3	+129.4	354.7	+131.3
	-6	517.5	+257.6	487.1	+263.6
nMOS_0.20x6.0	0	224.6	-	181.8	-
	-1.2	339.1	+114.5	301.7	+119.9
	-6	456.8	+244.7	426.5	+244.7
nMOS_0.20x0.1	0	427.7	-	315.2	-
	-1.2	544.2	+116.4	413.7	+98.5
	-6	623.6	+195.9	483.2	+168

Ringoscillator measurements

CPPM: Pierre Barrillon, Marlon Barbero, Denis Fougeron, Alexandre Habib and Patrick Pangaud



Low V_T		Super Low V_T	
Size Min	Size+	Size Min	Size+
INV0_LVT	INV4_LVT	INV4_SLVT	INV8_SLVT
NOR1_LVT_A	NOR4_LVT_A	NOR4_SLVT_A	NOR8_SLVT_A
NOR1_LVT_B	NOR4_LVT_B	NOR4_SLVT_B	NOR8_SLVT_B
NAND0_LVT_A	NAND4_LVT_A	NAND4_SLVT_A	NAND4_SLVT_A
NAND0_LVT_B	NAND4_LVT_B	NAND4_SLVT_B	NAND4_SLVT_B
DFF1_LVT	DFF4_LVT	DFF1_SLVT	DFF4_SLVT

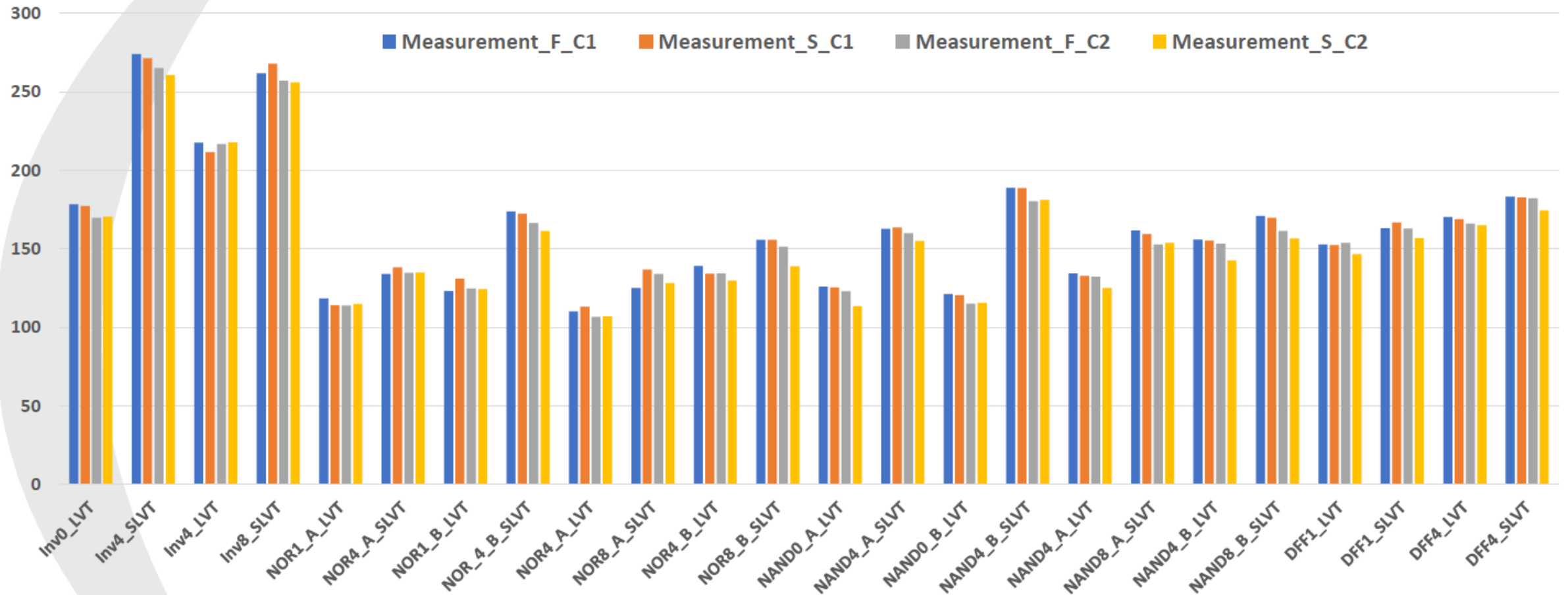
- CPPM contributed to MLR1 with a Ring Oscillator test chip to characterize the standard cells of the TJ 65 nm technology.
- The chip contains 48 ring oscillator based on different standard cells.
- 2 banks of 24 Rows each with the purpose of testing two approaches while irradiating:
 - Functional: the oscillation is enabled
 - Static: the oscillation is disabled

Ringoscillator measurements

CPPM: Pierre Barrillon, Marlon Barbero, Denis Fougeron, Alexandre Habib and Patrick Pangaud



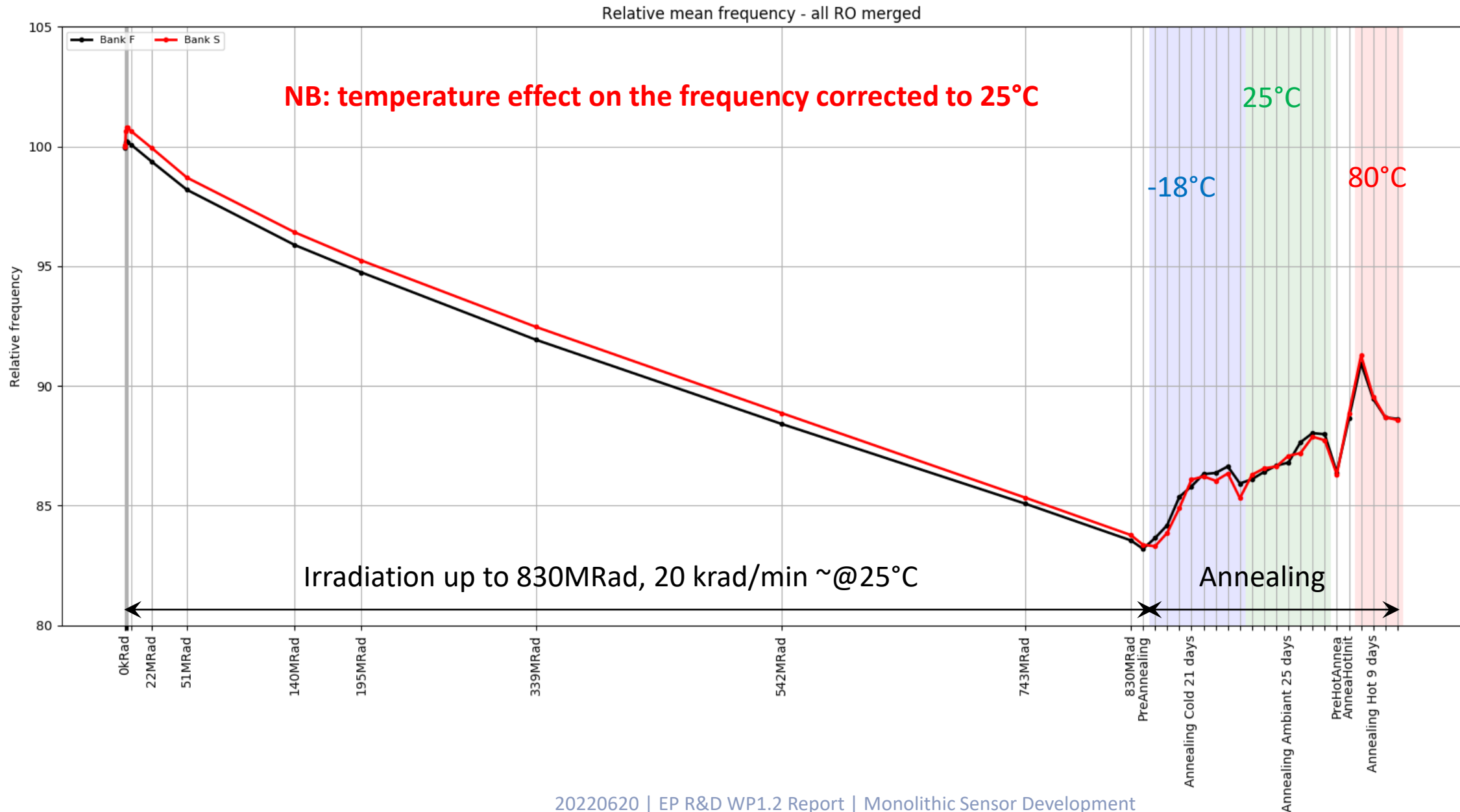
24 flavors oscillating in good agreement with simulations



The measurements are consistent between the 2 measured chips

Ringoscillator measurements, all averaged and merged

CPPM: Pierre Barrillon, Marlon Barbero, Denis Fougeron, Alexandre Habib and Patrick Pangaud



Ringoscillator measurements, summary



CPPM: Pierre Barrillon, Marlon Barbero, Denis Fougeron, Alexandre Habib and Patrick Pangaud

48 ring oscillators have been irradiated for 4 weeks at 20 krad/min and a total dose of 830 Mrads

- The chip continued to work with no issues spotted
- No real difference between static (quiet during irradiation) and functional (oscillating during irradiation)

Oscillation frequency dropped during irradiation by 12 to 25 %

- Compatible with measurements on similar technologies (same node size)
- Smaller cells (lower transistor width W) seem more affected than bigger cells (higher W). Coherent with transistor measurements

Annealing in progress, some effects observed

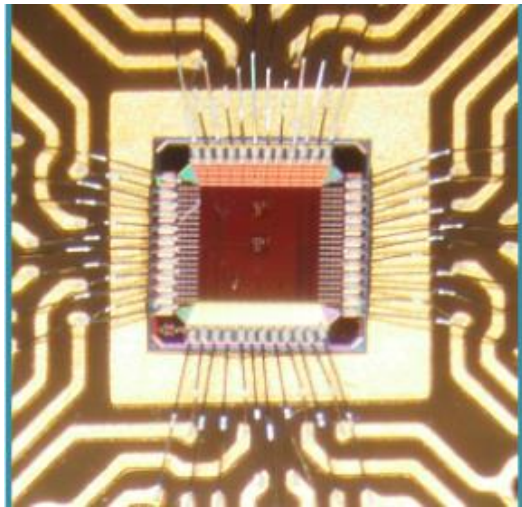
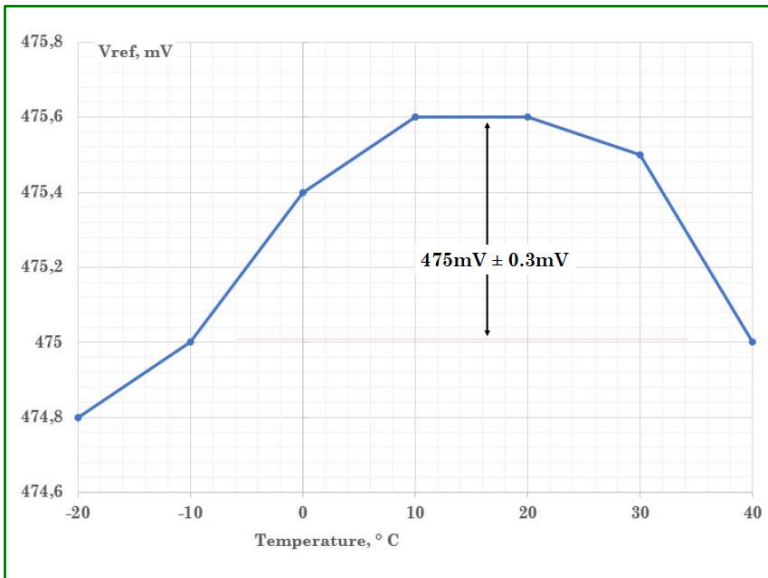
- Will do 2nd chip for consistency
- Results to be presented at TWEPP

IP Block measurements bandgap, T-sensor, VCO: all functional

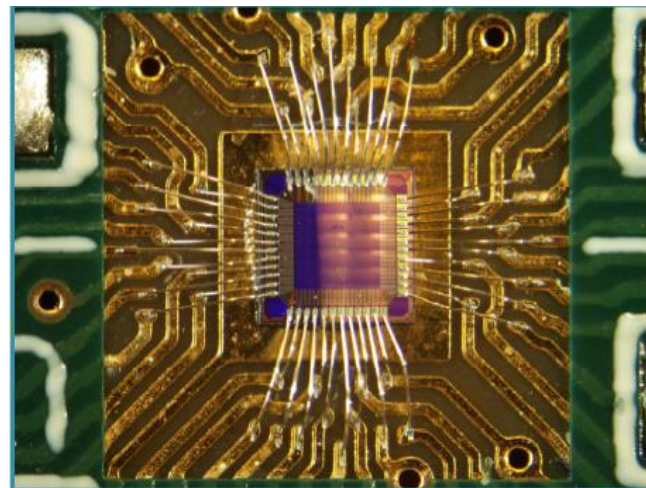
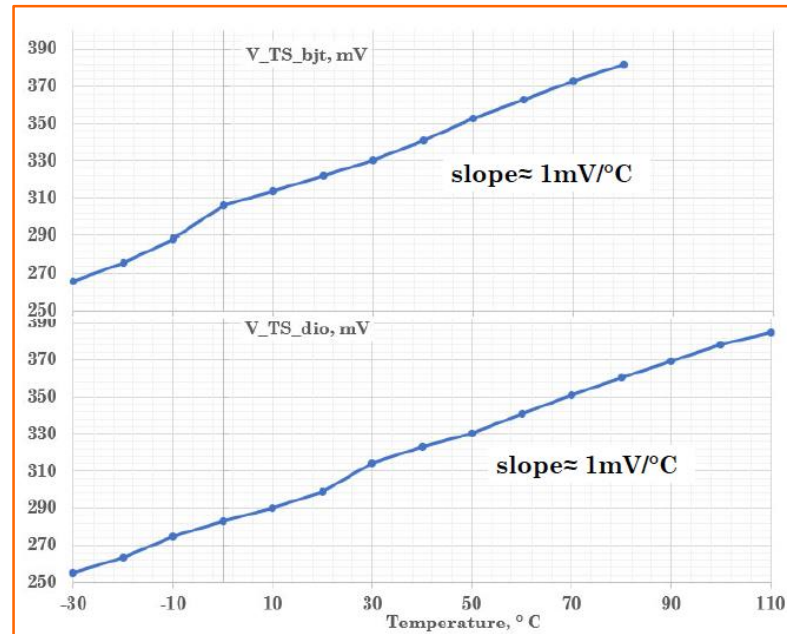
NIKHEF: V. Gromov, D. Gajanana, A. Yelkenci, A. Grelli, R. Kluit, M. Rossewij



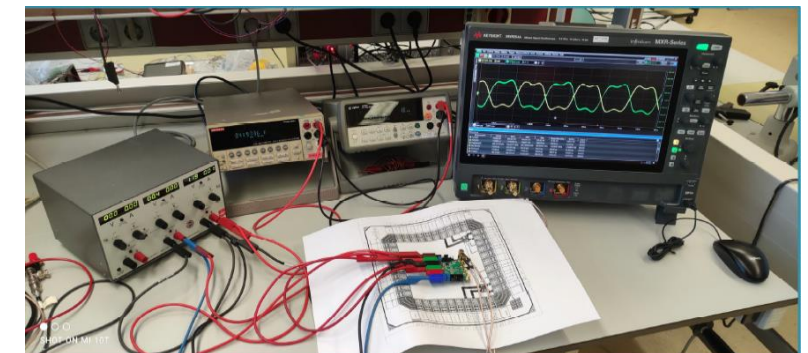
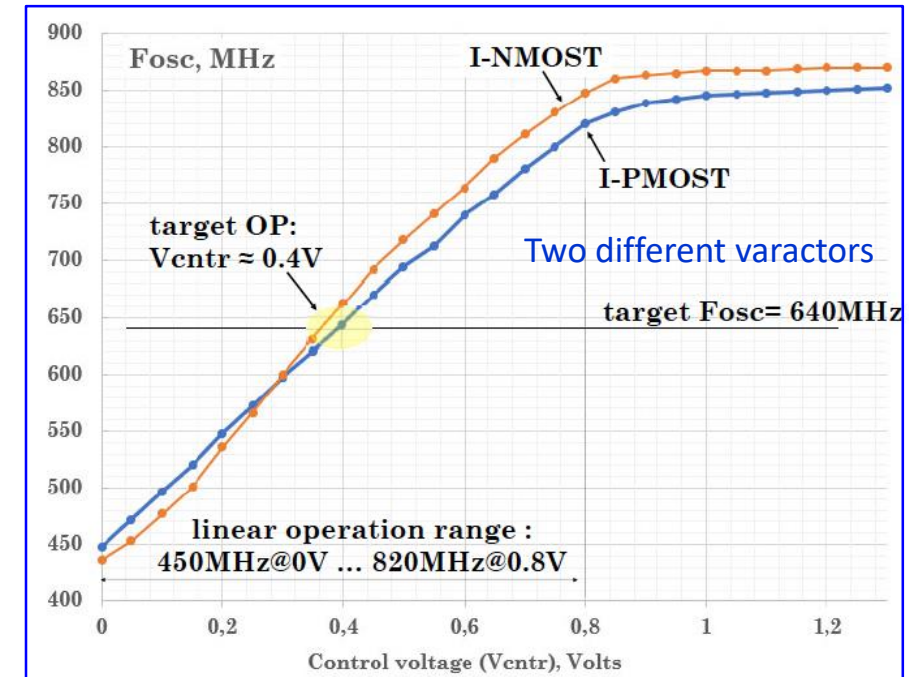
Bandgap



Temperature sensor



Voltage Controlled Oscillator (VCO)



IP Block measurements bandgap, T-sensor, VCO: irradiation results

NIKHEF: V. Gromov, D. Gajanana, A. Yelkenci, A. Grelli, R. Kluit, M. Rossewij

10 keV X-rays 6.5 Mrad/hour

Bandgap

- Standard process: BG 1, 2 24 hours -> 150 Mrad,
- Modified process BG 3, 4: 48 hours -> 300 Mrad

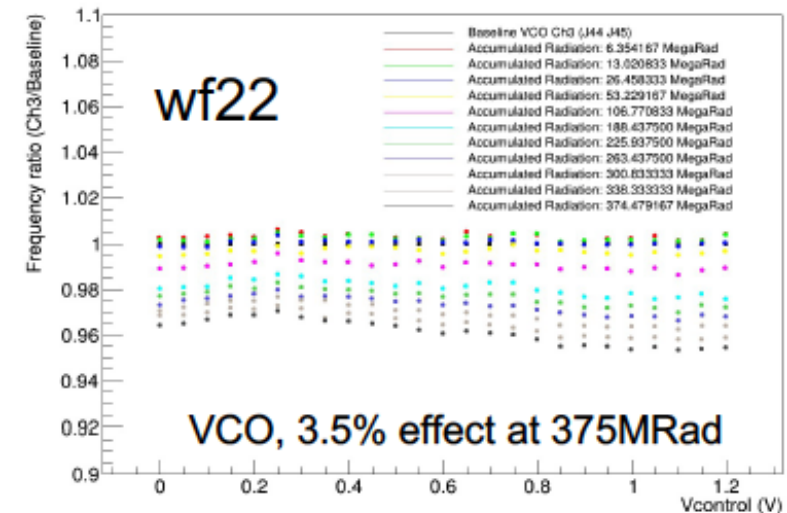
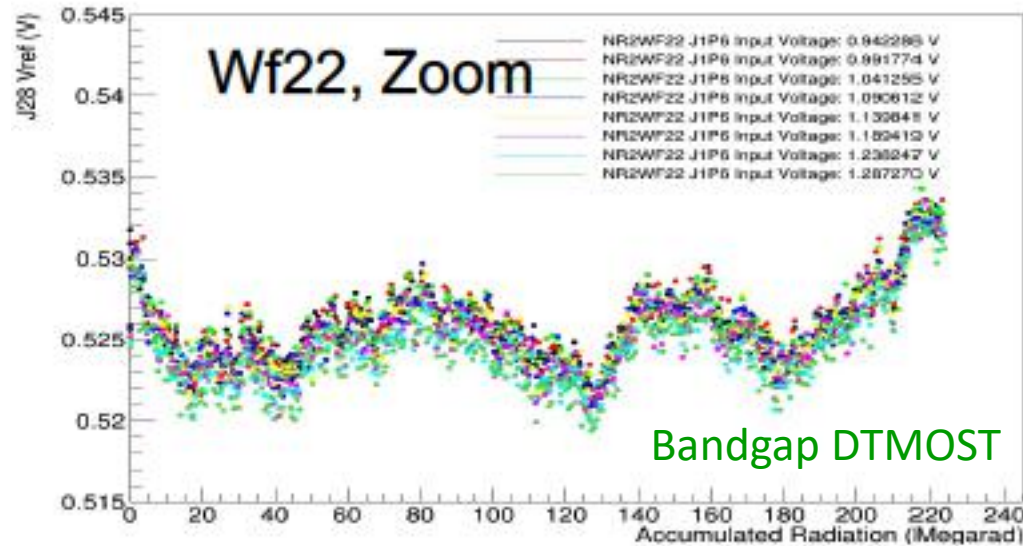
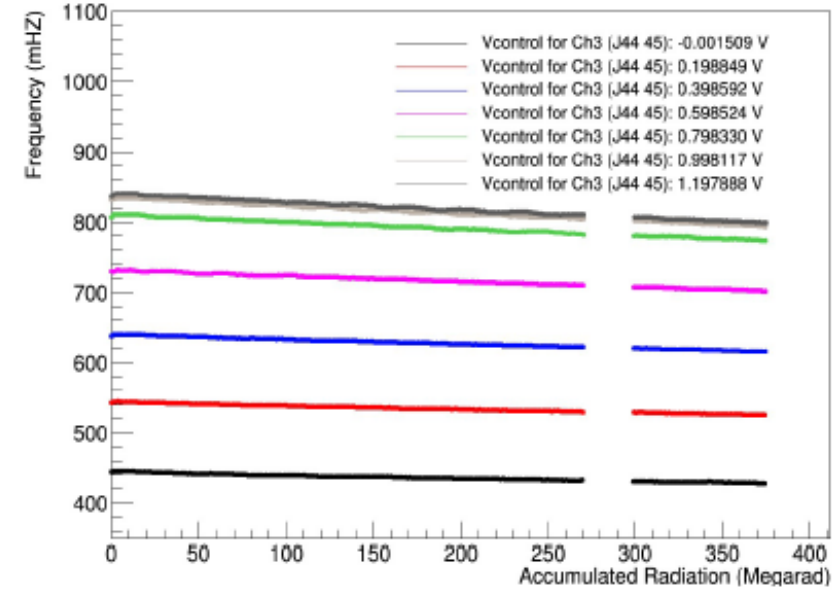
VCO

- Modified process 60hours -> 375 Mrad

T-sensor

- Modified process 15 hours -> ~100 Mrad

VCO, 375MRad

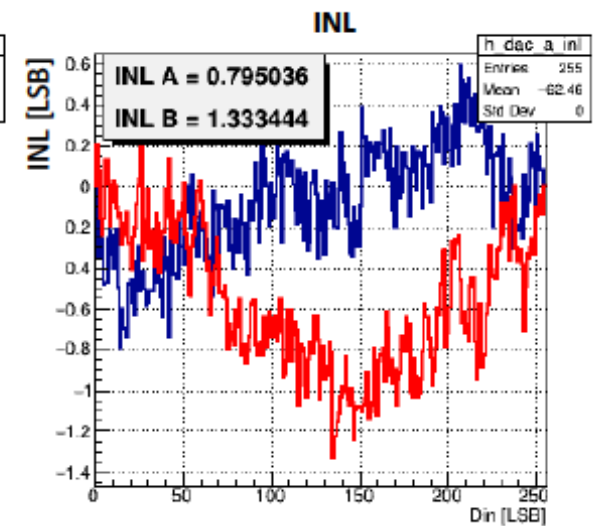
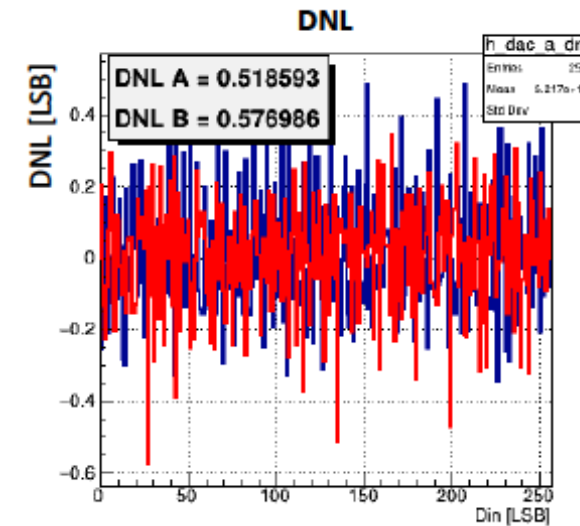
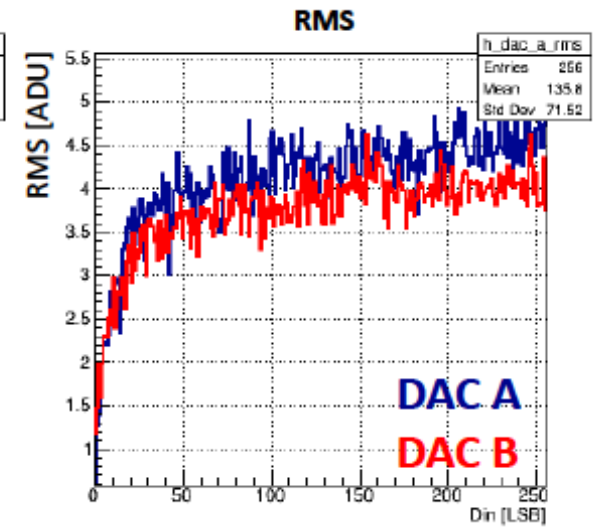
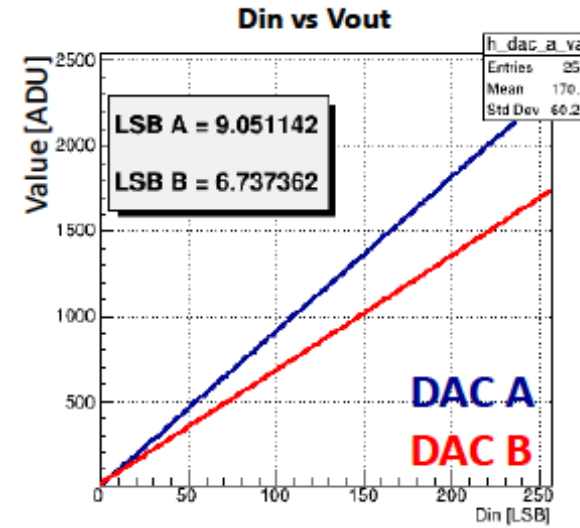


IP Block measurements DAC

IPHC: I. Valin, S. Bugiel, A. Dorokhov, C. Colledani, C. Hu et al.

	DAC A	DAC B
Resolution	8 bit	8 bit
LSB [nA]	40	40
Reference current [uA]	-0.8	-10.72
Power [uW] (*)	13	13
Area [um x um]	133x253	143x253

Both DACs fully functional



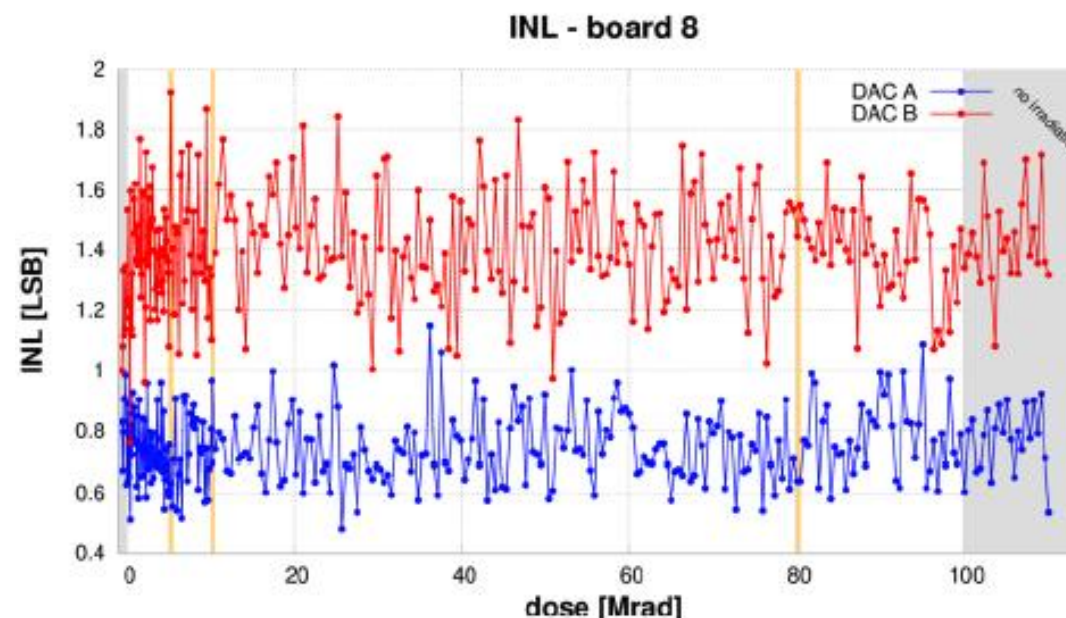
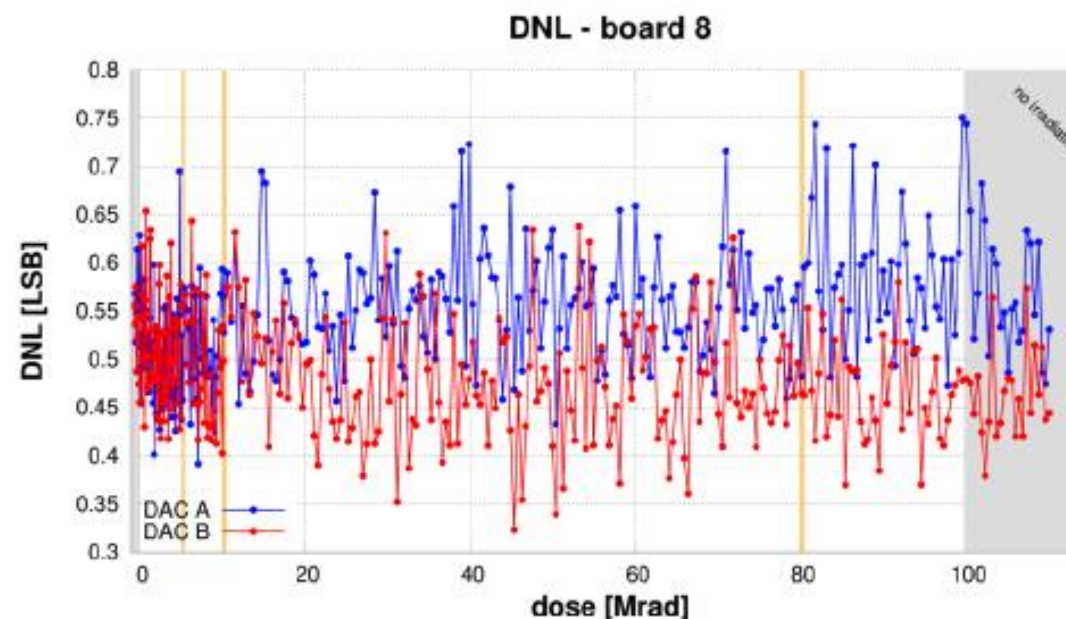
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Reference current [uA]	-0.8	-10.72
Power [uW] (*)	13	13
Area [um x um]	133x253	143x253

Both DACs remain functional after irradiation, Irradiation up to 100 Mrad in this example

10 keV X-rays 6.5 Mrad/hour



Transistor measurements in line with other 65 nm technologies

- Total ionizing dose tolerance very good up to 1 Grad for 1.2 V NMOS transistors, and up to 100 Mrad for PMOS transistors, after which significant drain current degradation sets in especially for short channel devices
- Higher voltage transistor radiation tolerance scales with gate oxide thickness
- In general **no showstoppers**, some more sensitivity with small W PMOS transistors

Leads to tested tolerance to in excess of 100 Mrad and well beyond for some sample circuits :

- Ring oscillators
- Bandgaps, temperature sensors, voltage controlled oscillators and DACs