28nm Analog front-end for hybrid sensors

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Requirements for PicoPix chip

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Matrix size	256×256	335×335
Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

PicoPix a demo chip for Velopix2

Designed as a "**real**" small scale prototype of the large Velopix2:

- Analog FE
- Local DCO
- Pixel data clustering
- Pixel readout
- SEE robust architecture
- Clock distribution using dDLL approach (as in Timepix4)
- High-speed links:
- On-chip Bandgap and biasing DACs
- UVM Functional verification

Slow Control protocol can be simplified → reused from Medipix4/Timepix4?

Why?

- Avoid to get false expectations on final design.
- If this design is successful the large scale chip should be simple and minimizes risk (time and money).
- PicoPix is a readout chip for fast timing and compatible with small pitch fast sensors.

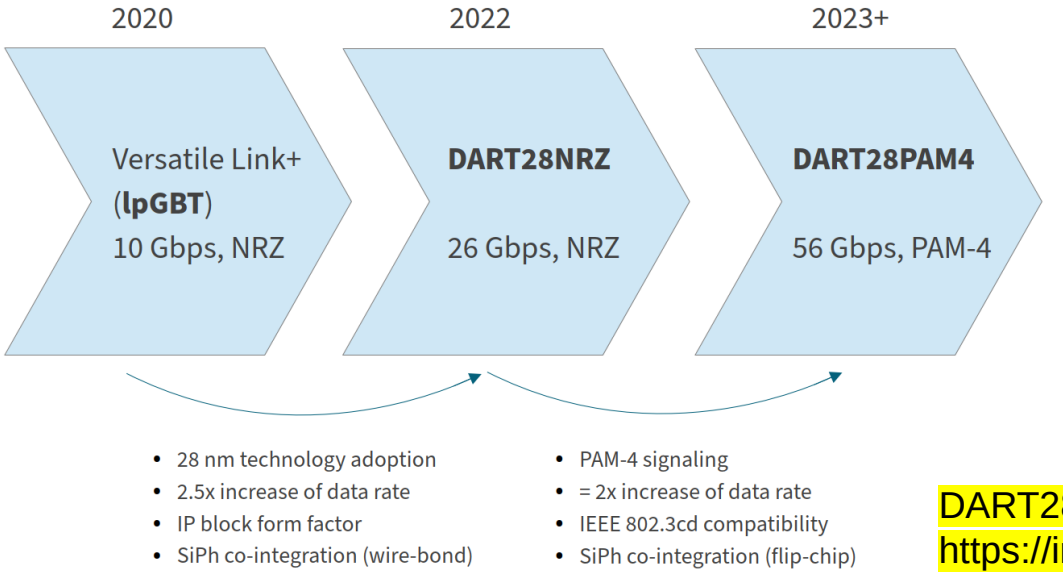
Slide courtesy: X. Llopart.

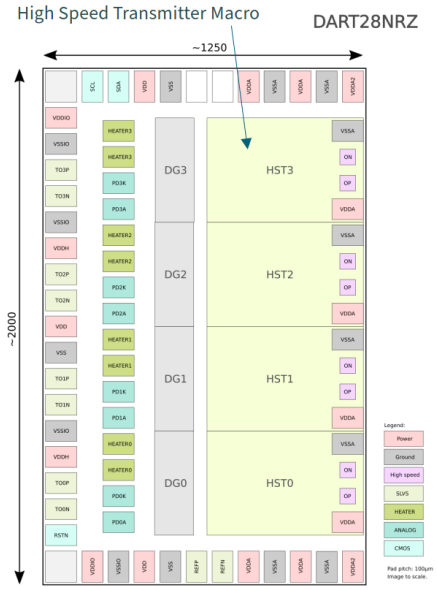
IP blocks and high speed links in 28nm

- **Close collaboration with EP R&D WP5**
  - IP blocks to be used for PicoPix ASIC.
  - Adopting the technology (technology overview, designers guide).
  - Documentation.

  Many thanks to R. Ballabriga, F. Bandi, M.Piller, S. Emiliani.

- **High speed links in 28nm in EP R&D WP6:**





DART28 (S.Bieregel)
https://indico.cern.ch/event/1138500/

28nm TSMC HPC+ CMOS technology

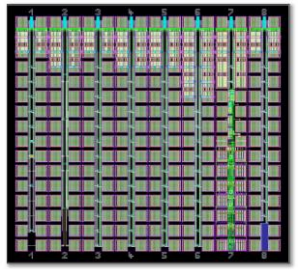
Overview:

- Front-End Features:
  - 0.9V core transistors (thin oxide) and 1.8 I/O transistors (thick oxide)
  - Triple well, Deep N-Well (to isolate P-Wells)
  - Multiple Vt transistors (but only five different flavors in the same design: ulvt, lvt, reg, uhvt)
  - Only vertical poly (PO) is allowed → No ELTs
- Back-End Features:
  - 9 copper layers plus last metal layer in AlCu pad

Radiation hardness:

- First indications shows that this technology is suitable for rad-hard designs
  - But no ELTs are possible
- Tested up to 1 Grad with 30-50% Isat ON max degradation in core transistors

  Better than TSMC 65nm
- More results with the test chip



TID28

Slide courtesy: X. Llopart.

Fundamental limits to time resolution in analog front-end

Fundamental Limits to Noise and Time Resolution in Highly Segmented Hybrid Pixel Detectors: Lessons Learnt on the Timepix4 Analog Front-end Design

R. Ballabriga, J. A. Alozy, F. N. Bandi, G. Blaj, M. Campbell, P. Christodoulou, V. Coco, A. Dorda, S. Emiliani, K. Heijhoff, E. Heijne, T. Hofmann, J. Kaplon, A. Koukab, I. Kremastiotis, X. Llopart, M. Noy, A. Paterno, M. Piller, J. M. Sallesse, V. Sriskaran, M. van Beuzekom, L. Tlustos

***Abstract*—The Timepix4 ASIC is a hybrid pixel detector readout chip designed in the framework of the Medipix4 Collaboration. The chip was manufactured in 65 nm CMOS process, and consists of a four side buttable matrix of 448 × 512 pixels with 55 µm pitch. The analog front-end has a gain of ~36 mV/ke⁻ when configured in *High Gain Mode*, and ~20 mV/ke⁻ when configured in *Low Gain Mode*. The Equivalent Noise Charge (ENC) is ~68 e^-_{rms} and ~80 e^-_{rms} in *High Gain Mode* and in *Low Gain Mode* respectively. This paper describes the analog front-end of the Timepix4 chip, and the models and calculations that led to the circuit optimization for low noise and low jitter. It also covers the design choices in the design of the detector readout electronics. The calculations presented here are validated with measurements and used to analyze the performance limits in terms of jitter and noise for charge sensitive amplifiers in high granularity pixel detectors.**

to a time resolution of ~ 60 ps_{rms}. Timepix4 can operate in data driven mode, in which the hit pixel sends off chip its coordinates, the measured energy and time information. In this mode of operation, the incoming hits can be time stamped within a ~ 200 ps time bin and the maximum flux the chip can deal with is ~ 3.6 $MHz\,mm^{-2}\,s^{-1}$. The chip can also operate in photon counting mode with a frame-based data readout. In this mode, the chip can deal with up to ~ 5 $GHz\,mm^{-2}\,s^{-1}$. The data readout is done via a programmable number of serializers (from 2 to 16) each running at a configurable frequency between 40 Mbps and 10 Gbps.

The analog front-end consists of a Charge Sensitive Amplifier (CSA) in which the value of the feedback capacitance is programmable in order to optimize the dynamic range

Submitted to journal

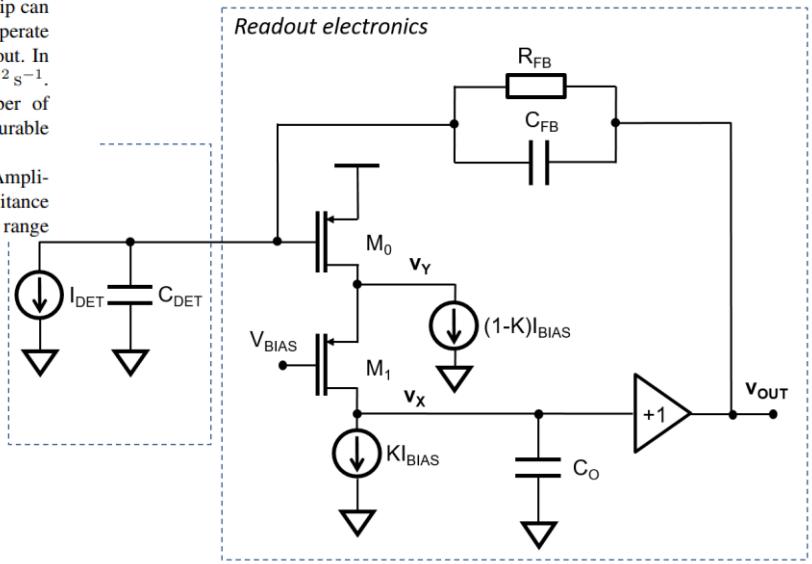


Figure 3: Simplified schematic of the charge sensitive amplifier.

Plot courtesy: R. Ballabriga.

Fundamental limits to time resolution in analog front-end

$$Jitter = \frac{qENC_{Total}}{\frac{dv_{out}(t)}{dt} C_{FB}}$$

Series noise (does not depend on gm!)
(scaling techno does not really help)

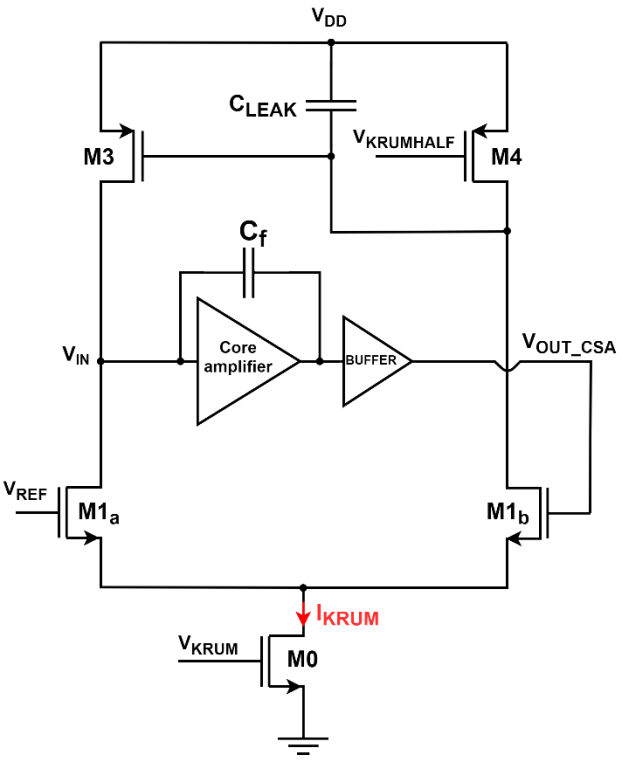
$$ENC_S = \sqrt{\frac{K_B T \Gamma (C_I + C_{FB}) C_{FB}}{\beta C_O q^2}} \qquad (21)$$

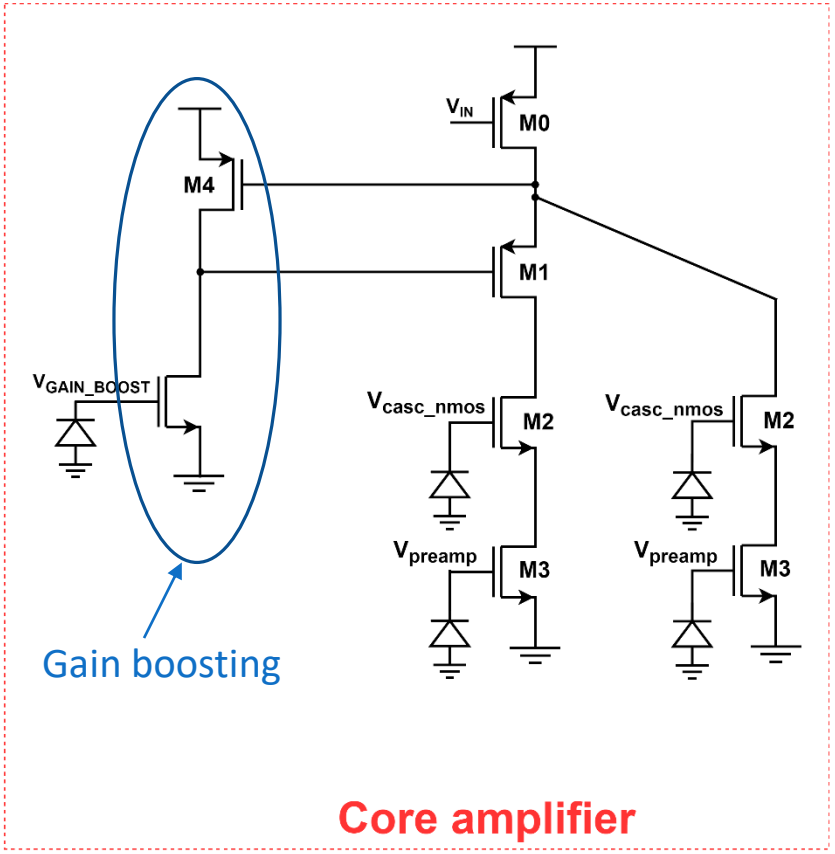
Slope

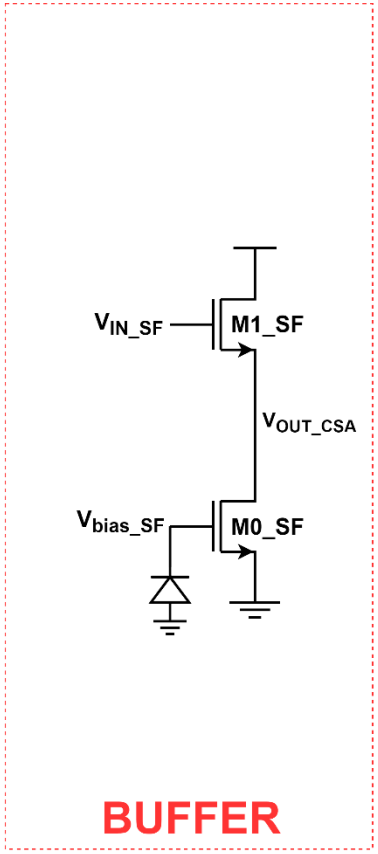
$$\frac{dv_{out}(t)}{dt} = \frac{Q_{in} g_m}{C_O (C_{IN} + C_{FB})} \frac{\frac{Q_{in}}{C_{FB}} - V_{th}}{\frac{Q_{in}}{C_{FB}}}$$

Design parameters	Comments
C_o	• Increasing the output capacitance lowers the series noise at the expense of degrading the jitter (Minimize its contribution in the layout phase!)
g_m	• Increasing the power consumption leads to larger slope value. • Below 1 W/cm² the ASIC can operates without extra active cooling. • More power can lead to an increase of the temperature and temperature induced leakage current: Shot noise!!
$C_{IN} + C_{FB}$	• Must be minimized to improve the jitter performance. • Redistribution layer add extra parasitic input capacitance. • 3D detectors: large intrinsic capacitance (~ 110 fF for 55 µm pitch pixel).
$Q_{IN}/C_{FB} \gg V_{TH}$	• For low input charges the slope of the signal is small: worst jitter performance!

Analog front-end for PicoPix

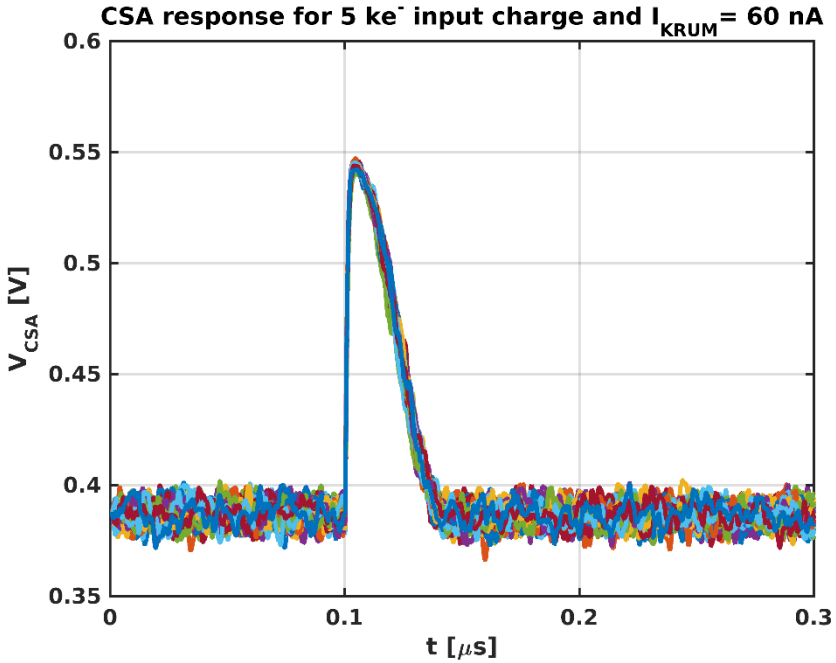


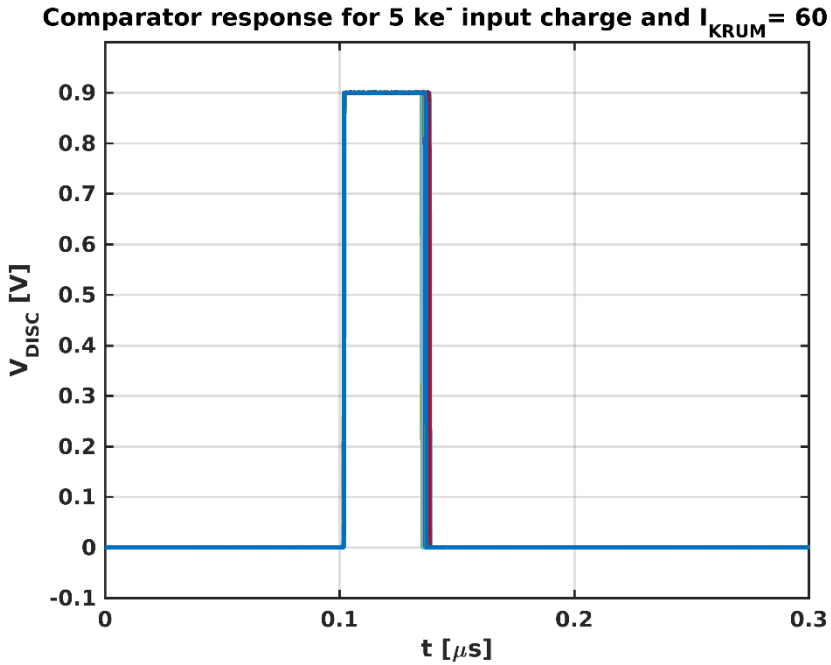




- CSA based on Krummenacher scheme with a feedback capacitance of ~3 fF: DC leakage compensation and programmable discharge time.
- Gain boosting to increase the DC gain of the core amplifier.

Analog front-end for PicoPix



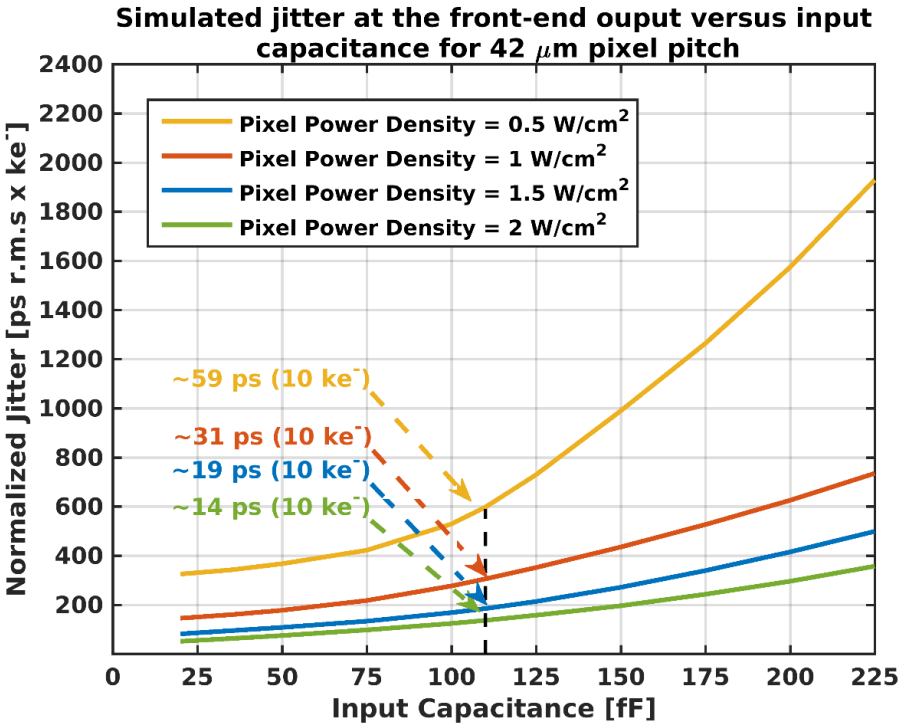


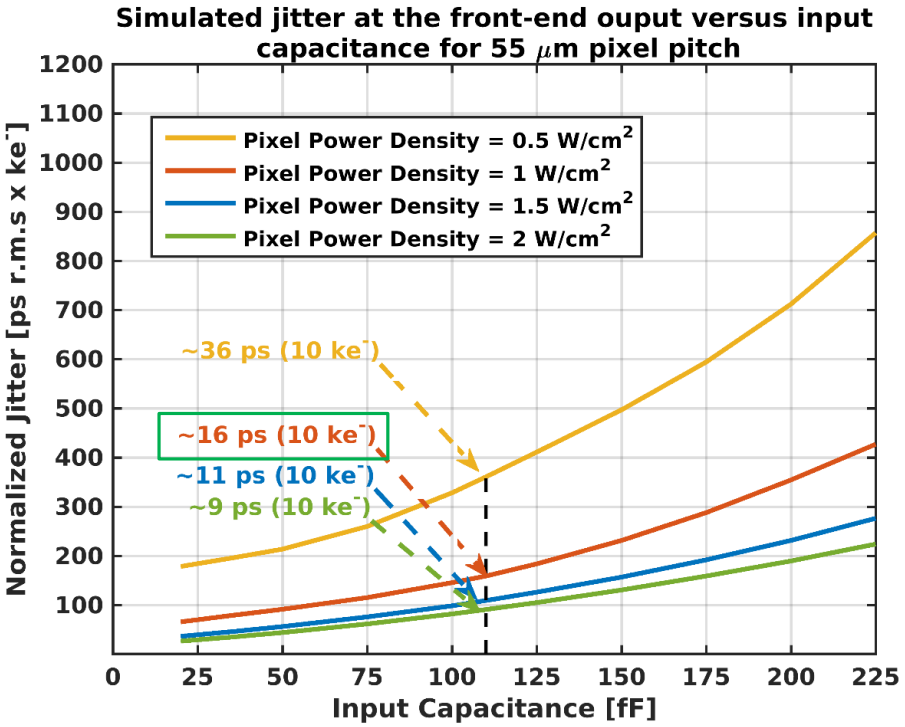
$I_{LEAK/pixel}$	$I_{krum} = 40\ nA$	$I_{krum} = 60\ nA$	$I_{krum} = 80\ nA$	$I_{krum} = 100\ nA$
300 pA	$ENC = 116\ e^-$	$ENC = 120\ e^-$	$ENC = 125\ e^-$	$ENC = 129\ e^-$
1 nA	$ENC = 117\ e^-$	$ENC = 121\ e^-$	$ENC = 125\ e^-$	$ENC = 129\ e^-$
5 nA	$ENC = 119e^-$	$ENC = 122\ e^-$	$ENC = 126\ e^-$	$ENC = 130\ e^-$
10 nA	$ENC = 121\ e^-$	$ENC = 124\ e^-$	$ENC = 127\ e^-$	$ENC = 131\ e^-$

NB: 110 fF is the total pixel capacitance obtained with 3D-trench sensor.
DOI: 10.1088/1748-0221/15/09/P09029

- $Pixel\ pitch = 55\ \mu m$
- $C_{IN} = 110\ fF$
- $C_{IN} = 3\ fF$
- $Gain = 40\ mV/ke^-$
- $I_{krum} = 60\ nA$
- $Discharge\ time = 41\ ns\ for\ 5\ ke^-$
- $Analog\ power\ density = 1\ W/cm^2$
- $Current\ I_{BIAS}(M0) = 5.7\ \mu A$
- $I_{LEAK/pixel} = 300\ pA$

Simulated jitter at front-end output versus input capacitance





- $Pixel\ pitch = 42\ \mu m$
- $I_{LEAK/pixel} = 300\ pA$
- $I_{KRUM} = 60\ nA$

- $Pixel\ pitch = 55\ \mu m$
- $I_{LEAK/pixel} = 300\ pA$
- $I_{KRUM} = 60\ nA$

Simulation using schematic view!!

NB: 110 fF is the total pixel capacitance obtained with 3D-trench sensor.
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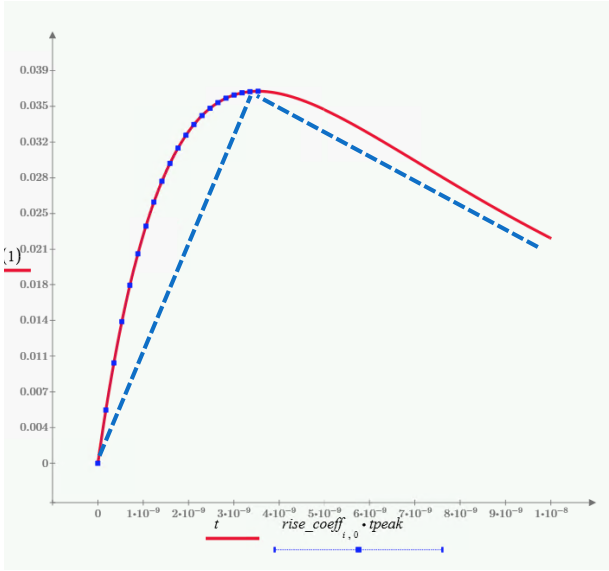
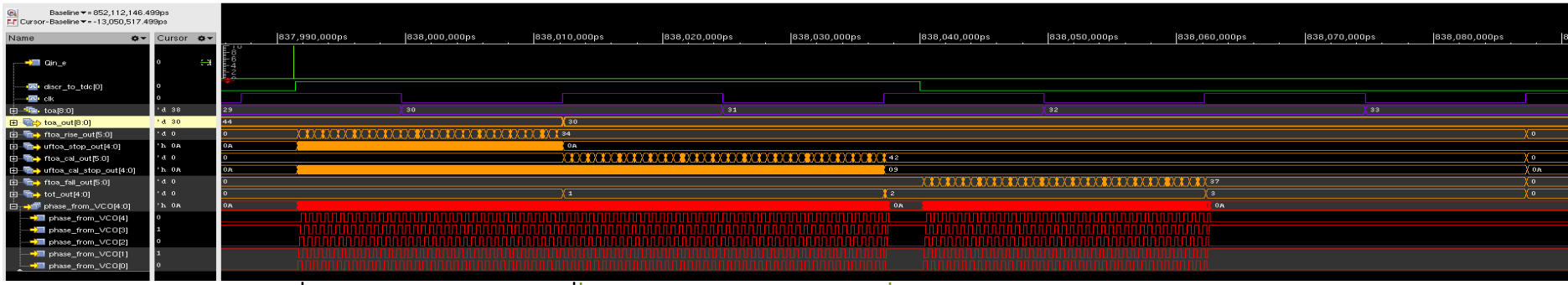
First RTL simulations

- Modified pixel model (from Medipix4) represents more realistically the rise-time slope → **critical to extract correct timing.**
  - Model includes analog pile-up.
  - Fall time is a constant slope.
- Used pixel model, new free-running DCO with calibration and Timepix4 adapted TDC logic.
  - Peak time=3.2ns, ENC=100e-rms, constant fall time of 5ns/ke.
- Simulation time of ~few seconds.





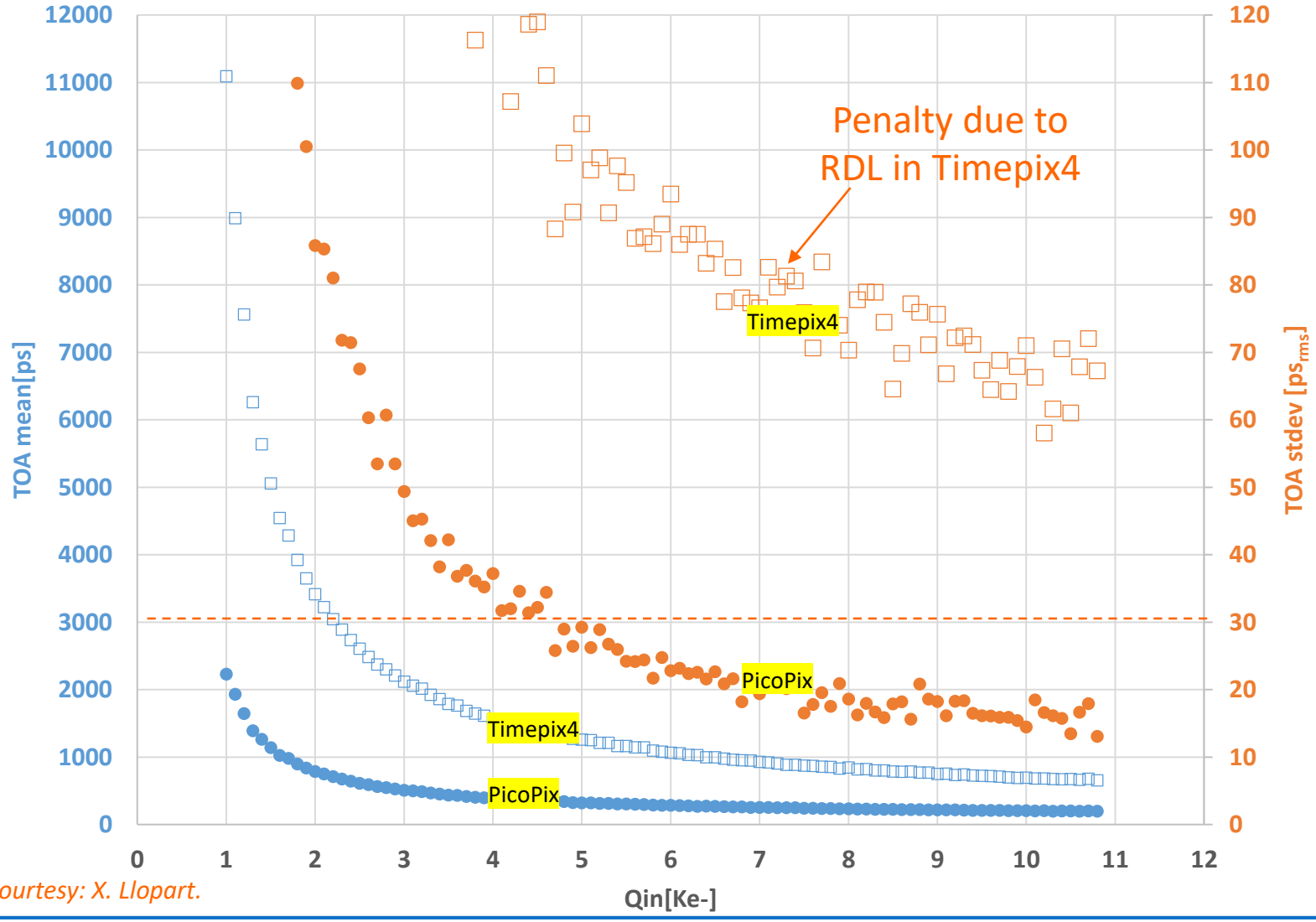
Rise Time mesurmement

DCO Calibration mesurmement

Fall time mesurmement

Slide courtesy: X. Llopart.

Comparison with Timepix4 and PicoPix



Slide courtesy: X. Llopart.

Thank you

Requirements

Technology:

- CMOS 28 nm – 9 metal

Analog supply voltage:

- 900 mV

System configuration:

- Pixel pitch → 55 µm x 55 µm | 42 µm x 42 µm

Matrix pixel:

- Different options might be available

Polarity:

- Optimized for electron collection

Power consumption:

- Total power consumption less than 1 W/cm². If 50 % goes to the analog pixel and 50% to the digital pixel, the maximum current consumption per analog front-end is 16.8 µA for 55 µm pixel pitch and 9.8 µA for 42 µm pixel pitch.

Peaking time:

- < 10 ns

Minimum threshold:

- ~ 500 e- which is possible with ENC < 75 e- (depends on the input capacitance)

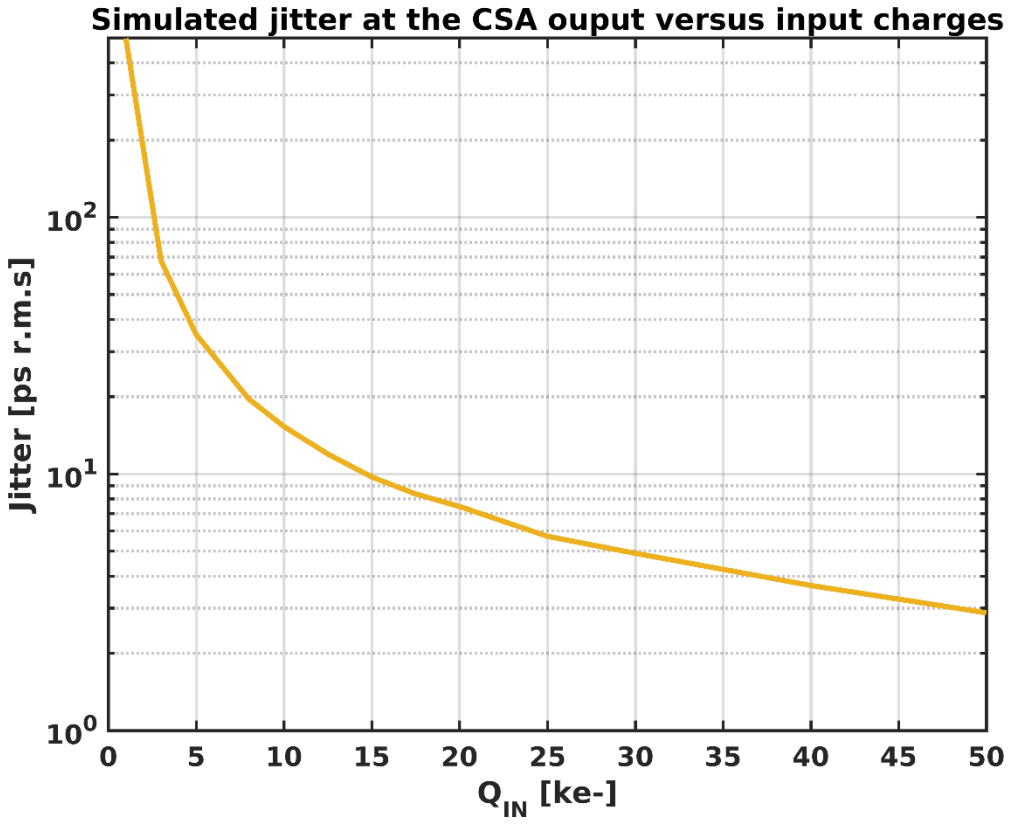
Number of thresholds:

- 1

Tuning DAC dynamic range:

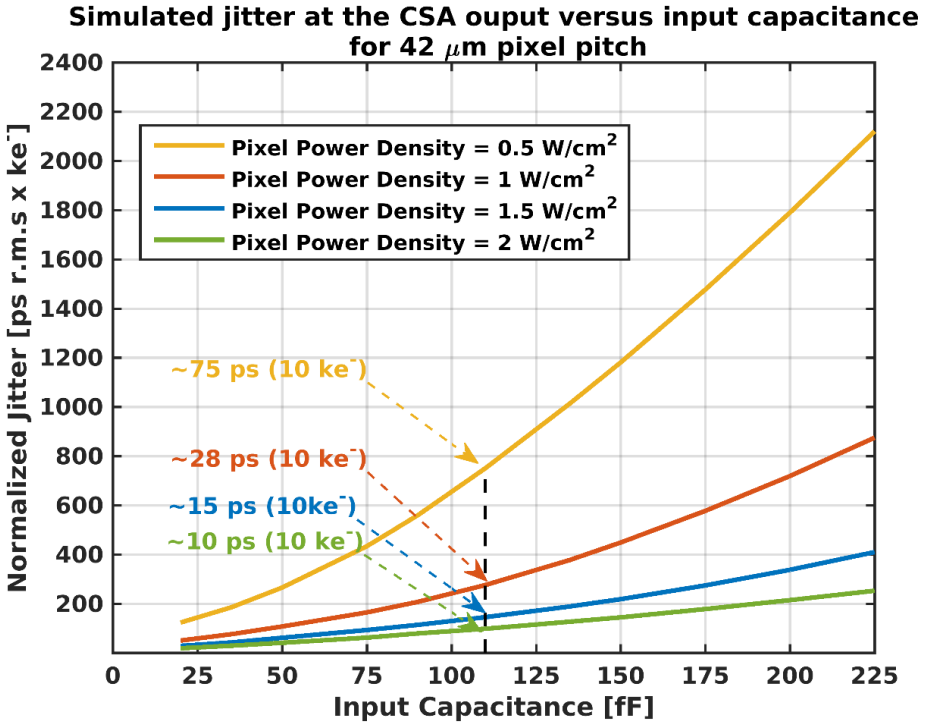
- 5 bits

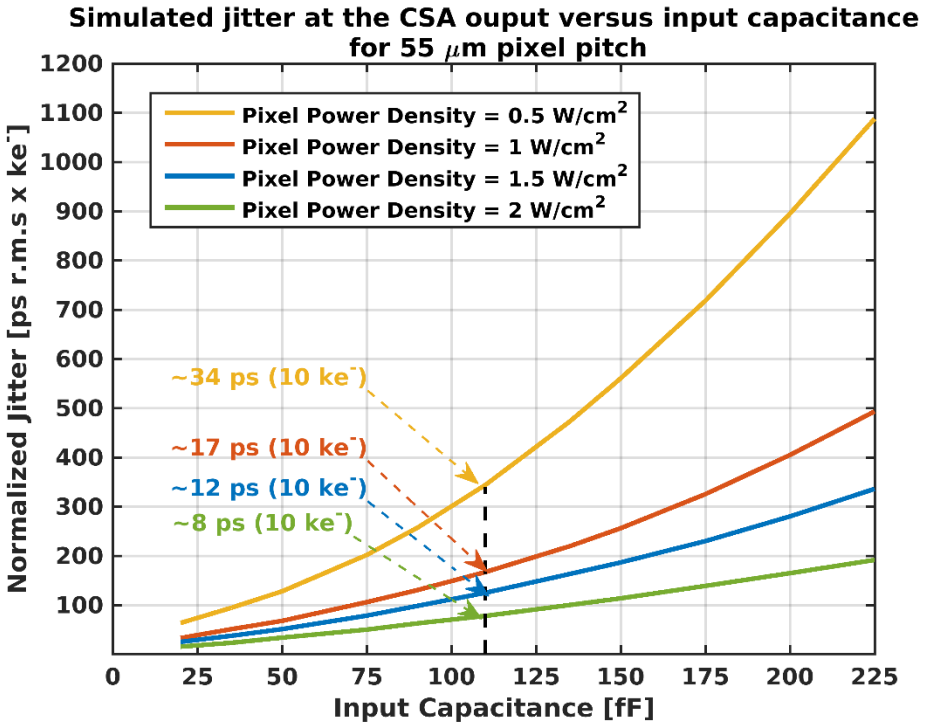
Simulated jitter at CSA output versus input charges



- $Pixel\ pitch = 55\ \mu m$
- $C_{IN} = 110\ fF$
- $Analog\ power\ density = 1\ W/cm^2$
- $Current\ I_{BIAS}(M0) = 5.7\ \mu A$
- $I_{LEAK/pixel} = 300\ pA$

Simulated jitter at CSA output versus input capacitance





- $Pixel\ pitch = 42\ \mu m$
- $I_{LEAK/pixel} = 300\ pA$

- $Pixel\ pitch = 55\ \mu m$
- $I_{LEAK/pixel} = 300\ pA$

NB: 110 fF is the total pixel capacitance obtained with 3D-trench sensor.
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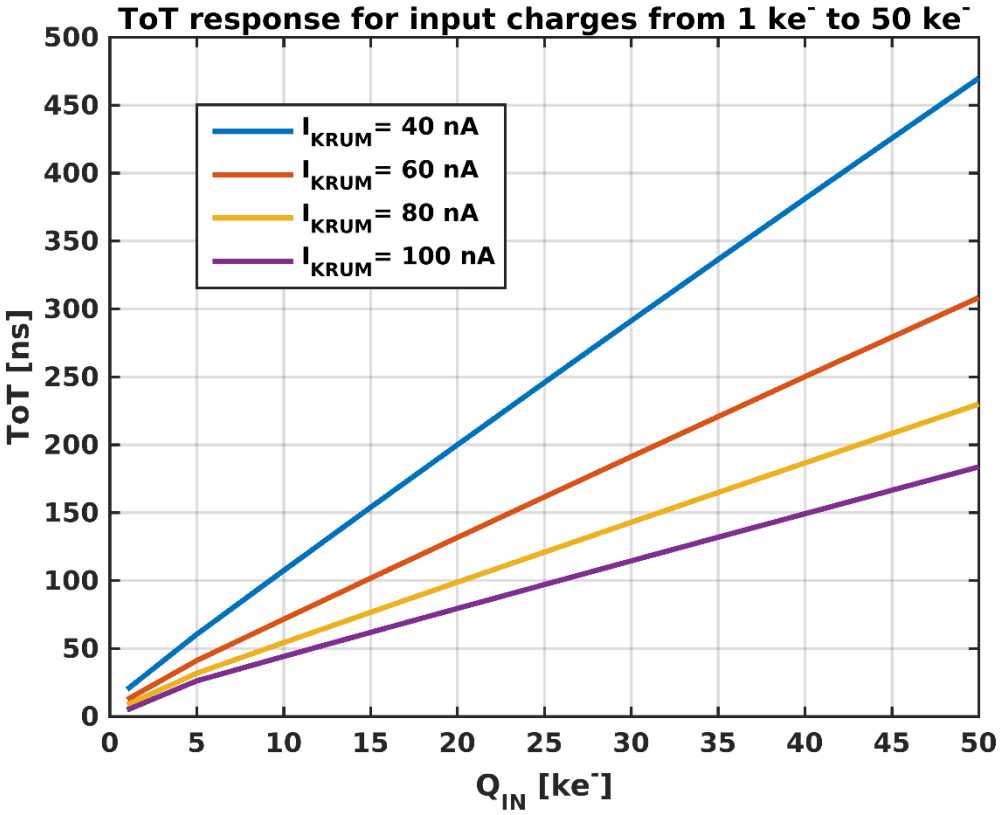
Simulated jitter at CSA output versus input charges



$Pixel\ pitch = 55\ \mu m$
$C_{IN} = 110\ fF$
$Analog\ power\ density = 1\ W/cm^2$
$Current\ I_{BIAS}(M0) = 5.7\ \mu A$
$I_{LEAK/pixel} = 300\ pA$
$V_{THR} = 500\ e^-$

NB: 110 fF is the total pixel capacitance obtained with 3D-trench sensor.
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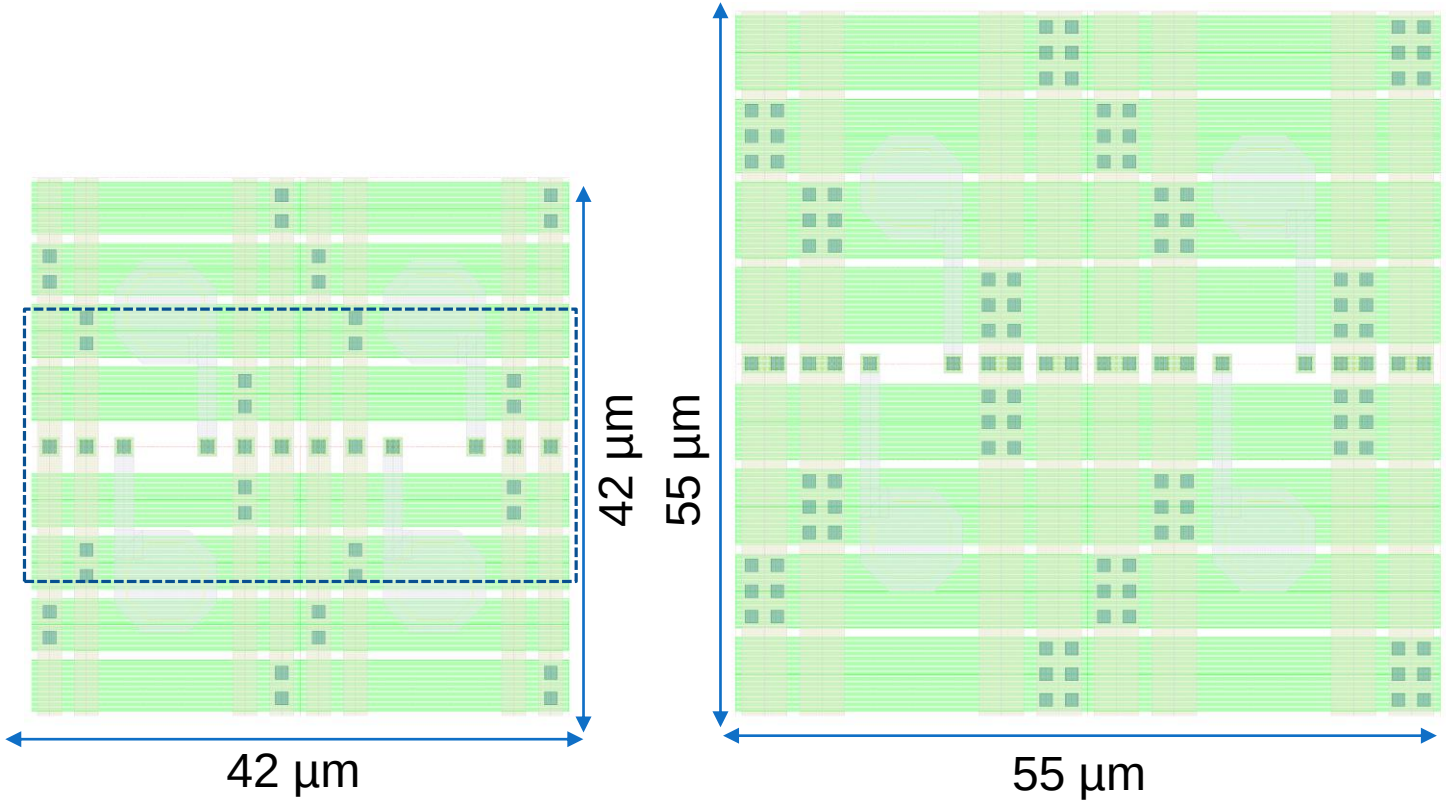
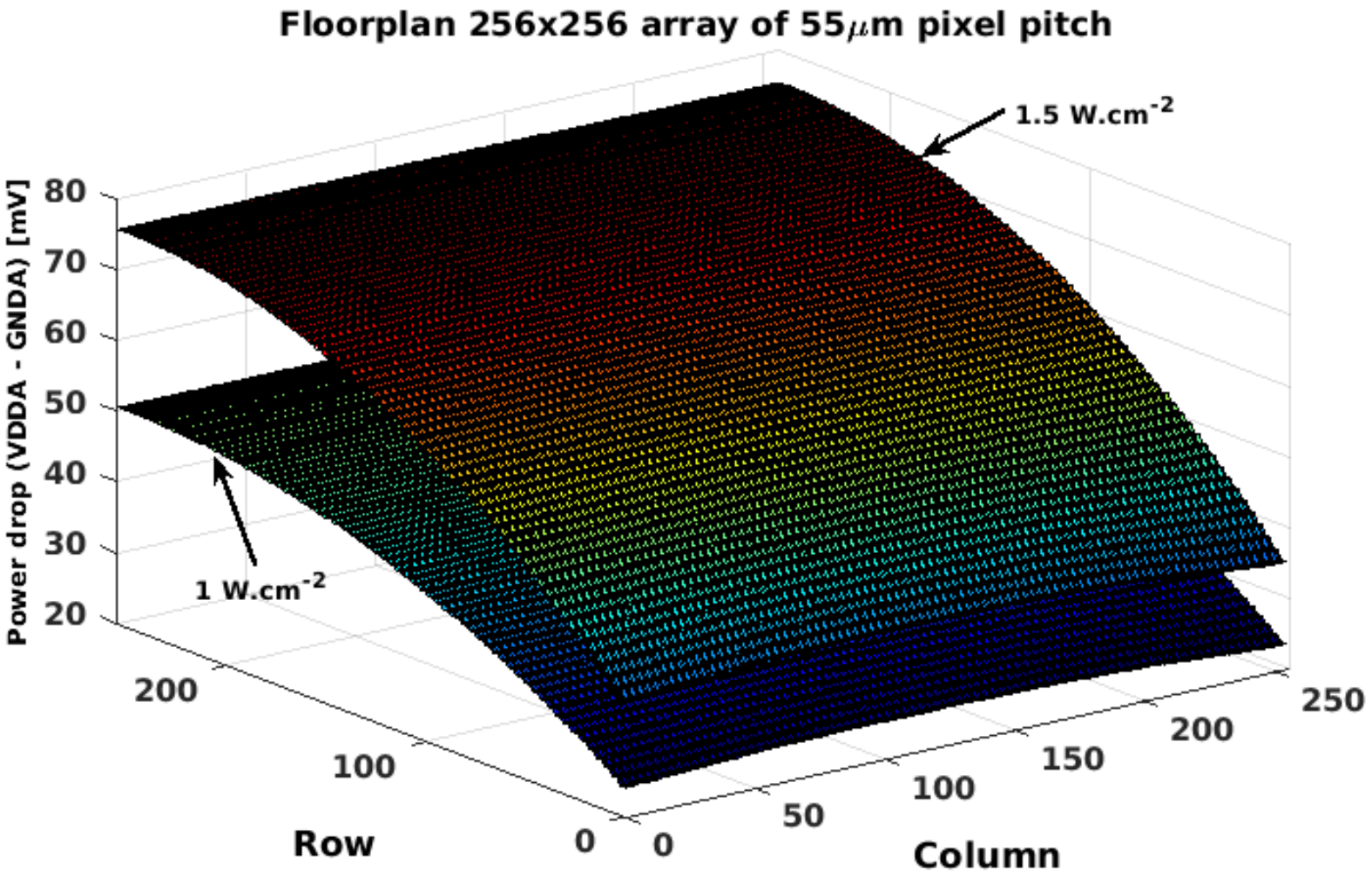
2x2 pixels floorplan



Pixel pitch	42 µm	55 µm
Pad opening	16 µm	16 µm
M9 width (horizontal power distribution)	8.3 µm	11.75 µm
AP width (vertical power distribution)	3.75 µm	7 µm
M8 width (vertical power distribution)	3.75 µm	7 µm

Power distribution scheme



Free running on-pixel DCO?

Explored the idea of the on-pixel free-running DCO:

- With 3-4 bits oscillation control
- Using 7T cells with extracted parasitic

Advantages:

- No control voltage distributed along the column
- Top down mismatch due to radiation can be minimized
- Faster oscillation times and lower dynamic power → better time resolution

Disadvantages:

- Requires DCO calibration measurement → data bandwitdth!

	freq	Phases	LSB	Area	power
Timepix4	640 MHz	8	195ps	~350µm^2	~500µW
Free-running DCO in 28nm	1.5-2.5 GHz	10	66-40ps	~70µm^2	~150µW

Slide courtesy: X. Llopart.

Parameter				Slow	Fast	Typical
VDD				810m	990m	900m
tcbn28hpcplusb...				rc_cworst	rc_cbest	rc_typical
tcbn28hpcplusb...				rc_cworst	rc_cbest	rc_typical
temperature				80	-40	25
toplevel.scs				ass_ps	aff_pf	att_pt

Output	Pass/Fail	Min	Max	Slow	Fast	Typical
thr		405m	495m	405m	495m	450m
freqVCO_2		1.449G	3.325G	1.449G	3.325G	2.287G
uftoa_bin		30.07p	69.02p	69.02p	30.07p	43.72p
Start_bin		10.5p	24.47p	24.47p	10.5p	15.6p
uftoa0		30.62p	69.88p	69.88p	30.62p	44.16p
uftoa1		29.53p	68.17p	68.17p	29.53p	43.3p
uftoa2		30.63p	69.89p	69.89p	30.63p	44.16p
uftoa3		29.52p	68.17p	68.17p	29.52p	43.3p
uftoa4		30.62p	69.87p	69.87p	30.62p	44.16p
uftoa5		29.52p	68.17p	68.17p	29.52p	43.29p
uftoa6		30.63p	69.89p	69.89p	30.63p	44.16p
uftoa7		29.52p	68.17p	68.17p	29.52p	43.3p
uftoa8		30.63p	69.88p	69.88p	30.63p	44.15p
uftoa9		29.51p	68.1p	68.1p	29.51p	43.27p
uftoaT		300.7p	690.2p	690.2p	300.7p	437.2p
freqVCO	fail	1.449G	3.325G	1.449G	3.325G	2.287G
uftoaI		30.07p	69.02p	69.02p	30.07p	43.72p
start_off	fail	-65.09 %	-64.32 %	-64.54 %	-65.09 %	-64.32 %
uftoa0_off	pass	997.3 m%	1.826 %	1.246 %	1.826 %	997.3 m%
uftoa1_off	pass	-1.816 %	-978.3 m%	-1.234 %	-1.816 %	-978.3 m%
uftoa2_off	pass	992.5 m%	1.852 %	1.267 %	1.852 %	992.5 m%
uftoa3_off	pass	-1.84 %	-978.2 m%	-1.235 %	-1.84 %	-978.2 m%
uftoa4_off	pass	986.5 m%	1.827 %	1.238 %	1.827 %	986.5 m%
uftoa5_off	pass	-1.83 %	-986.5 m%	-1.234 %	-1.83 %	-986.5 m%
uftoa6_off	pass	1.004 %	1.841 %	1.261 %	1.841 %	1.004 %
uftoa7_off	pass	-1.826 %	-970.1 m%	-1.234 %	-1.826 %	-970.1 m%
uftoa8_off	pass	981.2 m%	1.85 %	1.252 %	1.85 %	981.2 m%
uftoa9_off	pass	-1.885 %	-1.049 %	-1.325 %	-1.885 %	-1.049 %
Power		75.49 uW	260.7 uW	75.49 uW	260.7 uW	147.8 uW