WP6: High Speed Links

EP R&D

WP6 High Speed Links

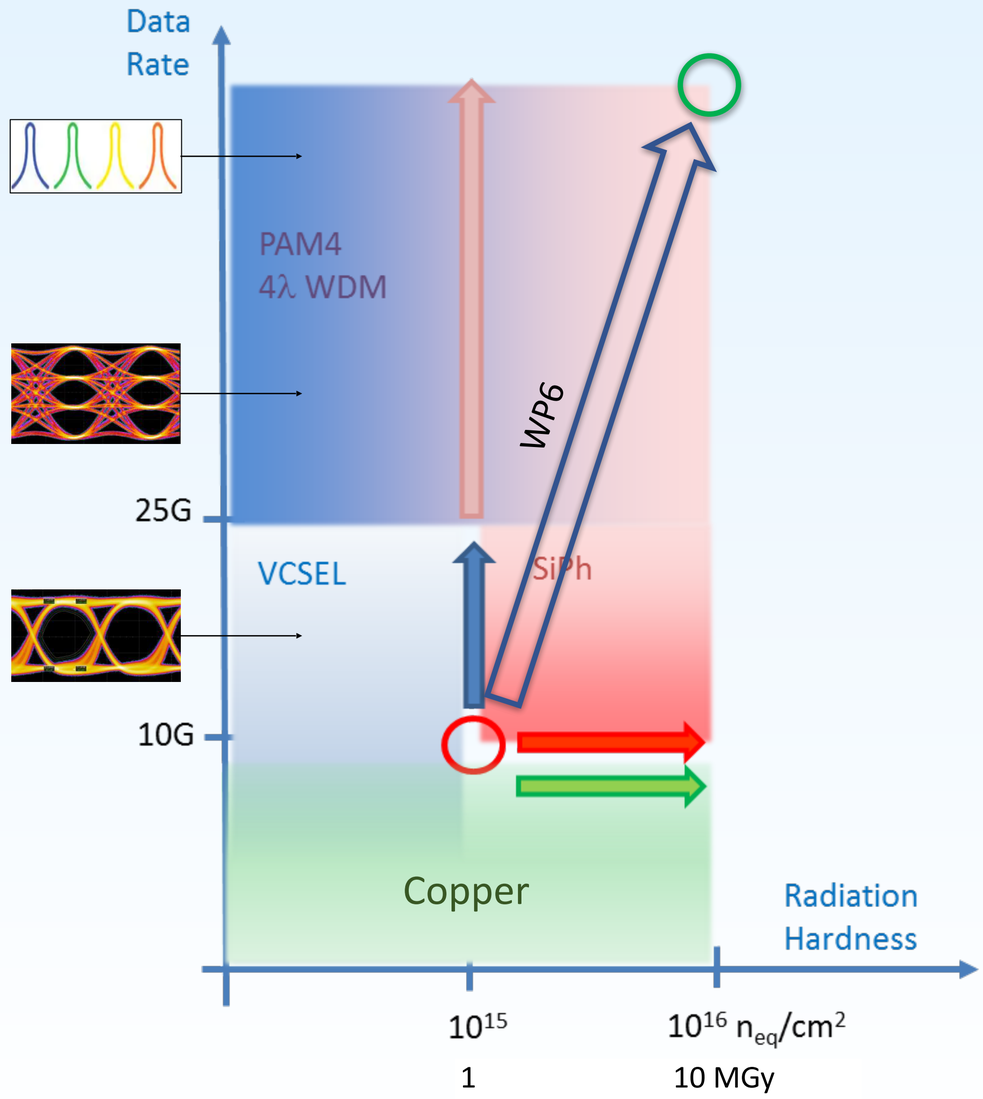
presented by
Jan Troska & Mateusz Baszczyk
on behalf of the WP6 team

WP6 Goals

- Provide the future HEP systems with:
  - High bandwidths: ~50 Gbps / lane
  - High radiation tolerance
  - Low power, low mass

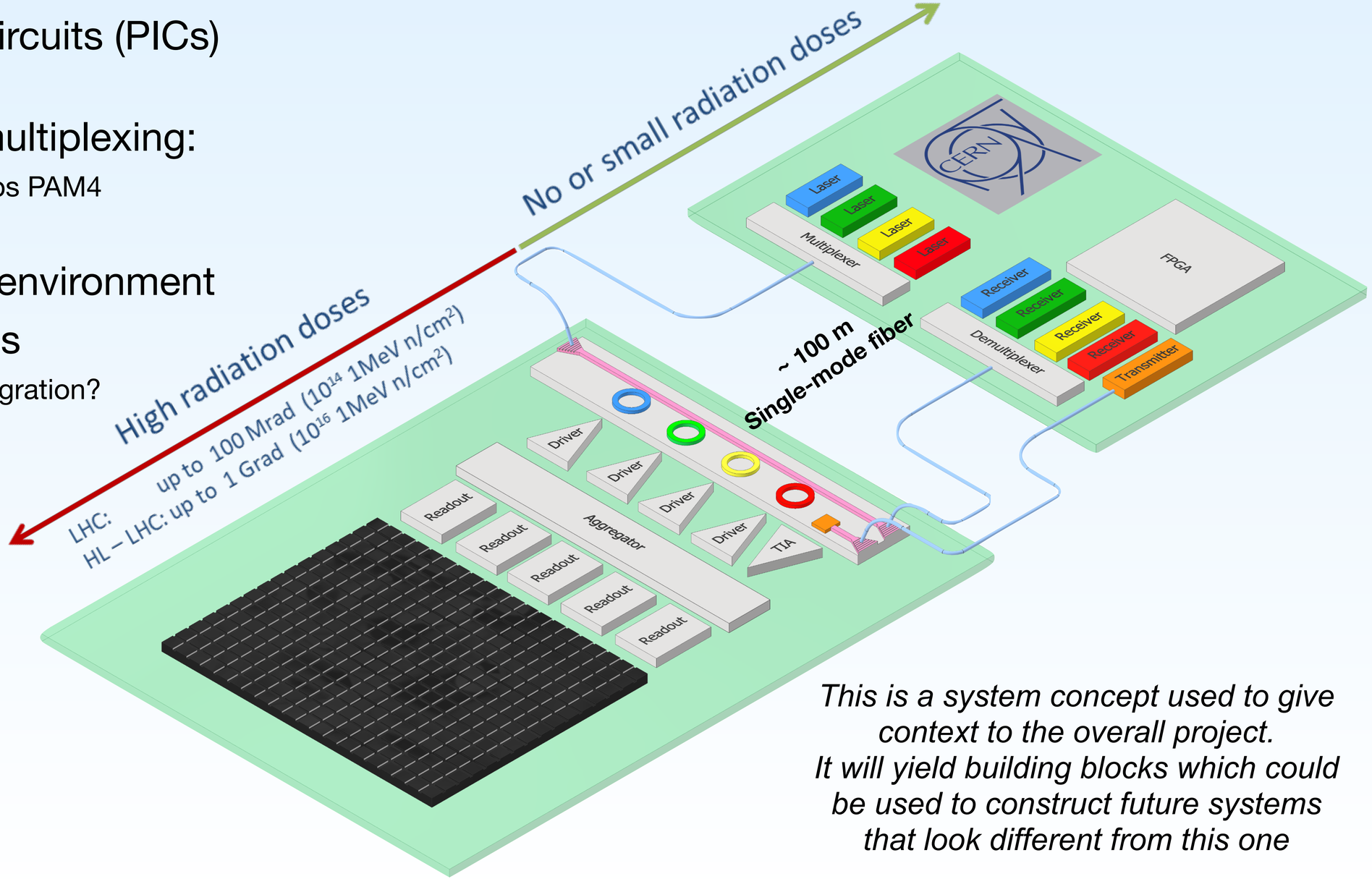
c.f. ECFA roadmap

- FPGAs
  - Compatible with the state-of-the-art
- ASICS
  - Advanced technologies 28nm CMOS
  - High order modulation formats (PAM4)
  - Drivers for SiPh optoelectronics
- Optoelectronics
  - Silicon Photonics (SiPh)
  - External Modulators
    - Ring & MZ
- Wavelength Division Multiplexing (WDM)



Future HEP Link Architecture

- Photonic Integrated Circuits (PICs)
  - RadHard “promise”
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ / 50 Gbps PAM4
  - Fibre: 100 Gbps / 200 Gbps
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?

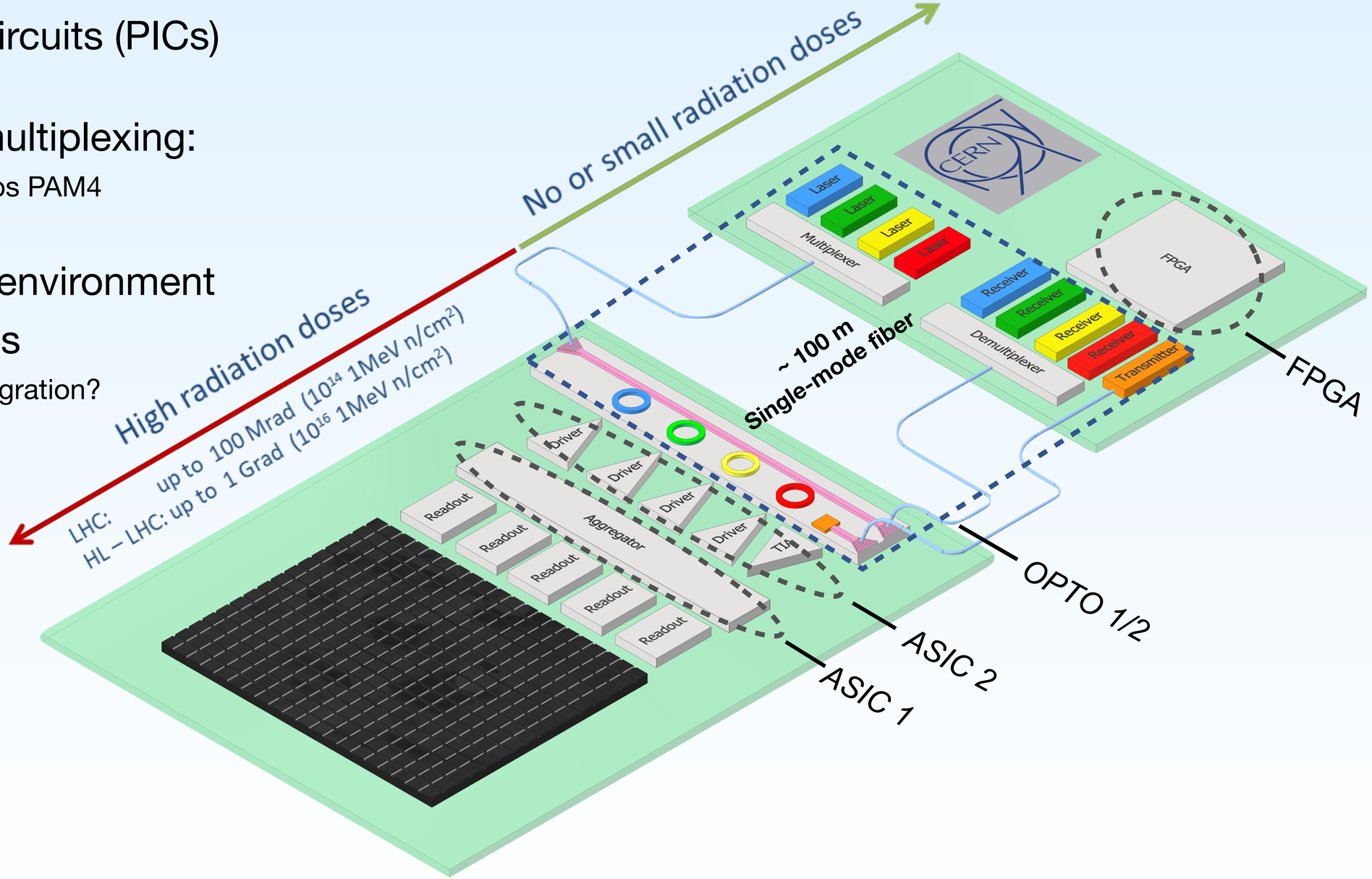


This is a system concept used to give context to the overall project.
It will yield building blocks which could be used to construct future systems that look different from this one

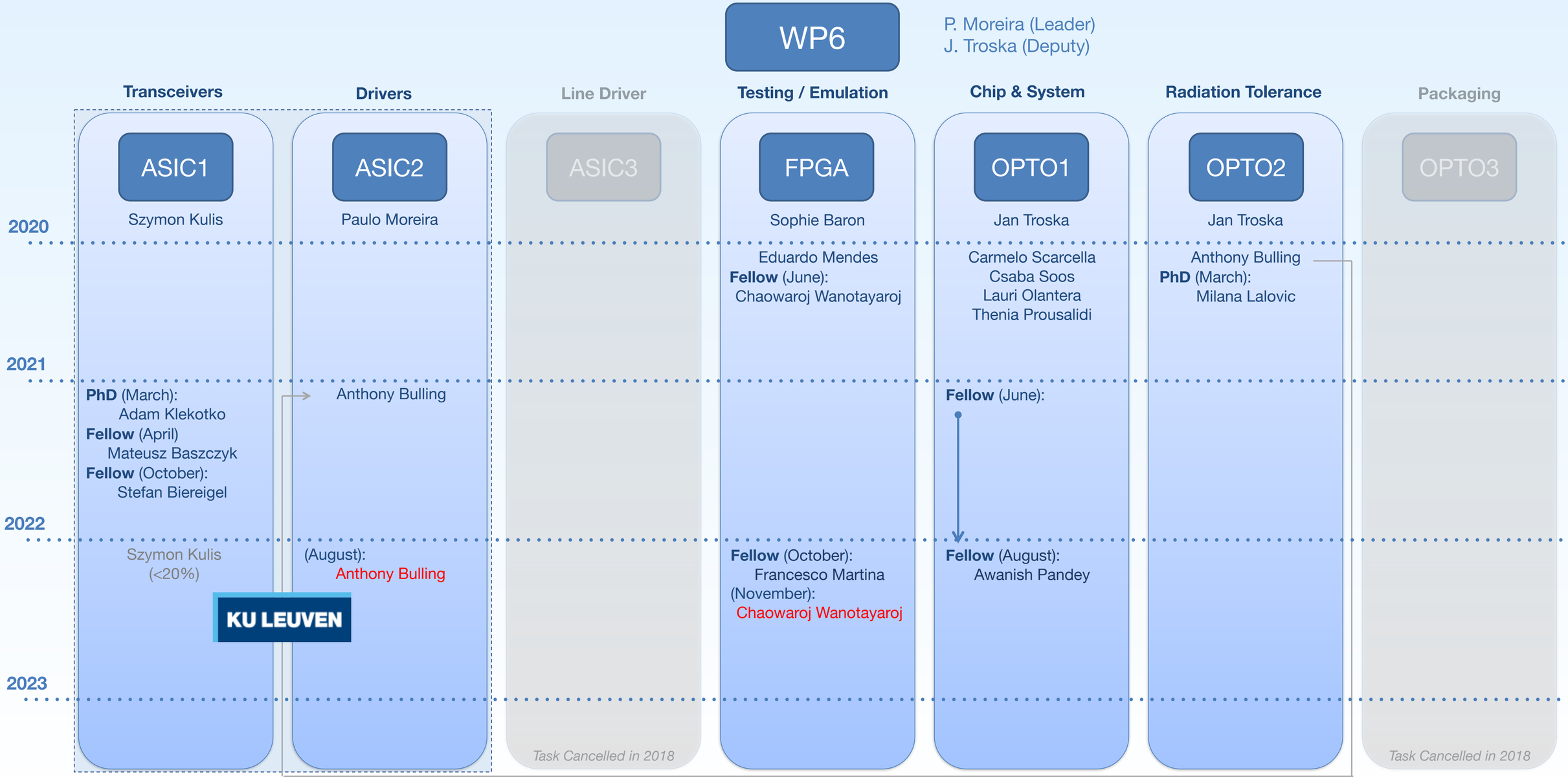
jan.troska@cern.ch

WP6 Project breakdown

- Photonic Integrated Circuits (PICs)
  - RadHard “promise”
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ / 50 Gbps PAM4
  - Fibre: 100 Gbps / 200 Gbps
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?

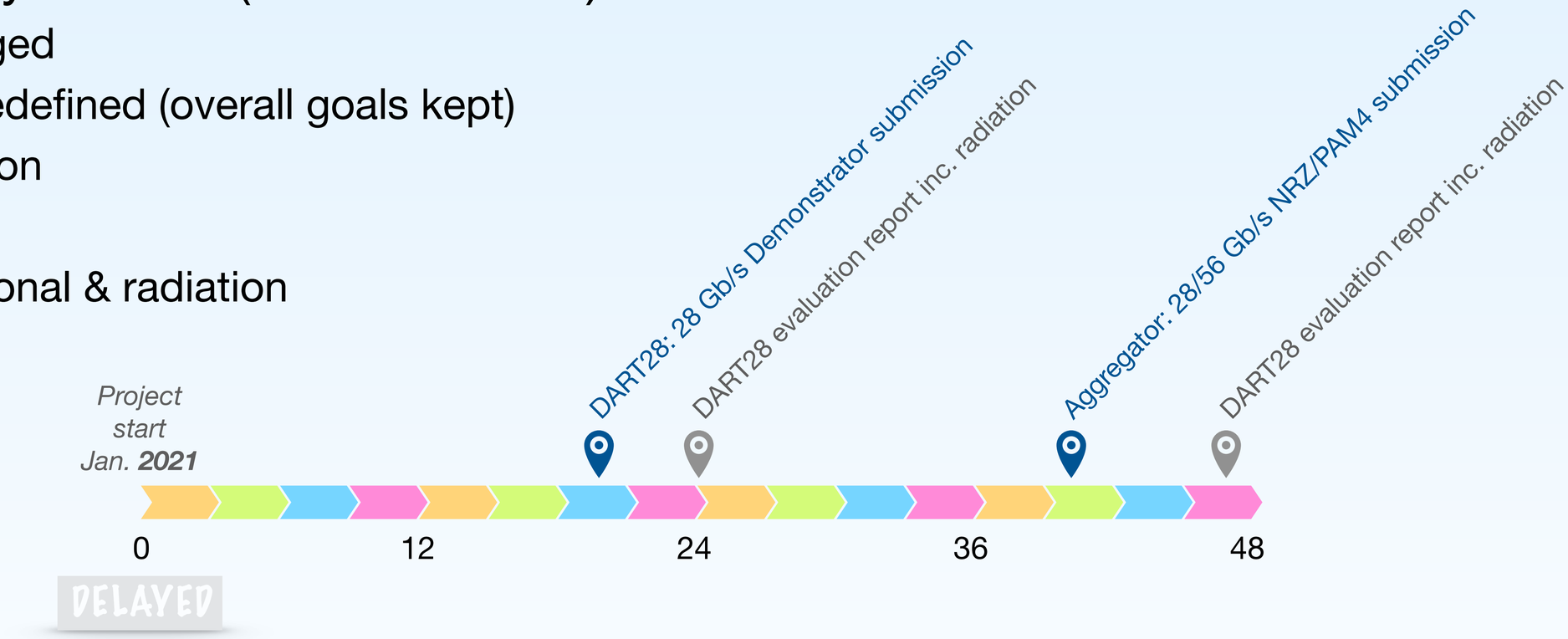


WP6 Team Evolution



ASIC1/2 actual vs planned

- To address the delayed start (2021 vs 2020):
  - ASIC-1/2 activities merged
  - Goals and milestones redefined (overall goals kept)
  - Common chip submission
  - Common test bench
  - Common testing: functional & radiation



Deliverable
Milestone
Actual

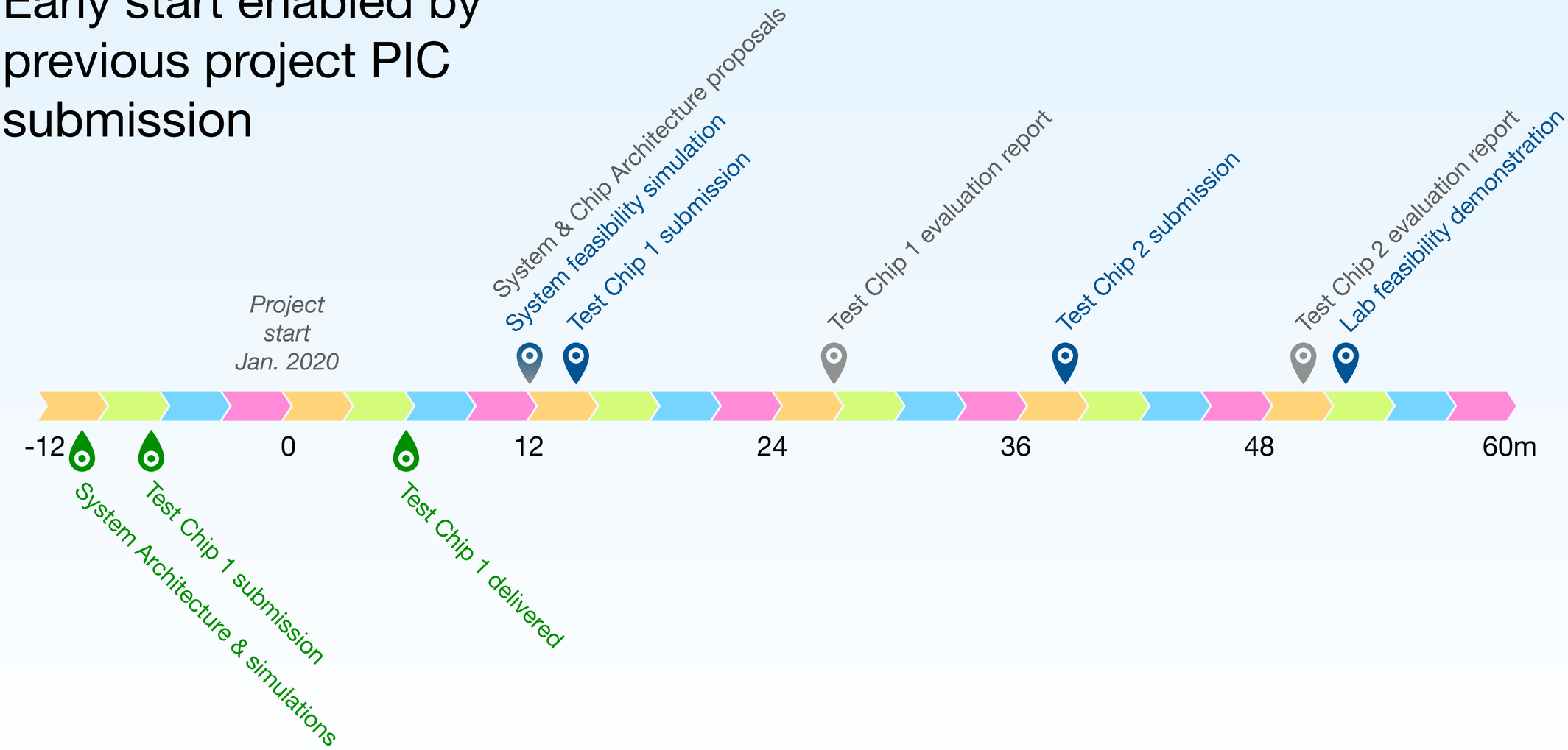
jan.troska@cern.ch

FPGA actual vs planned

Deliverable
Milestone
Actual

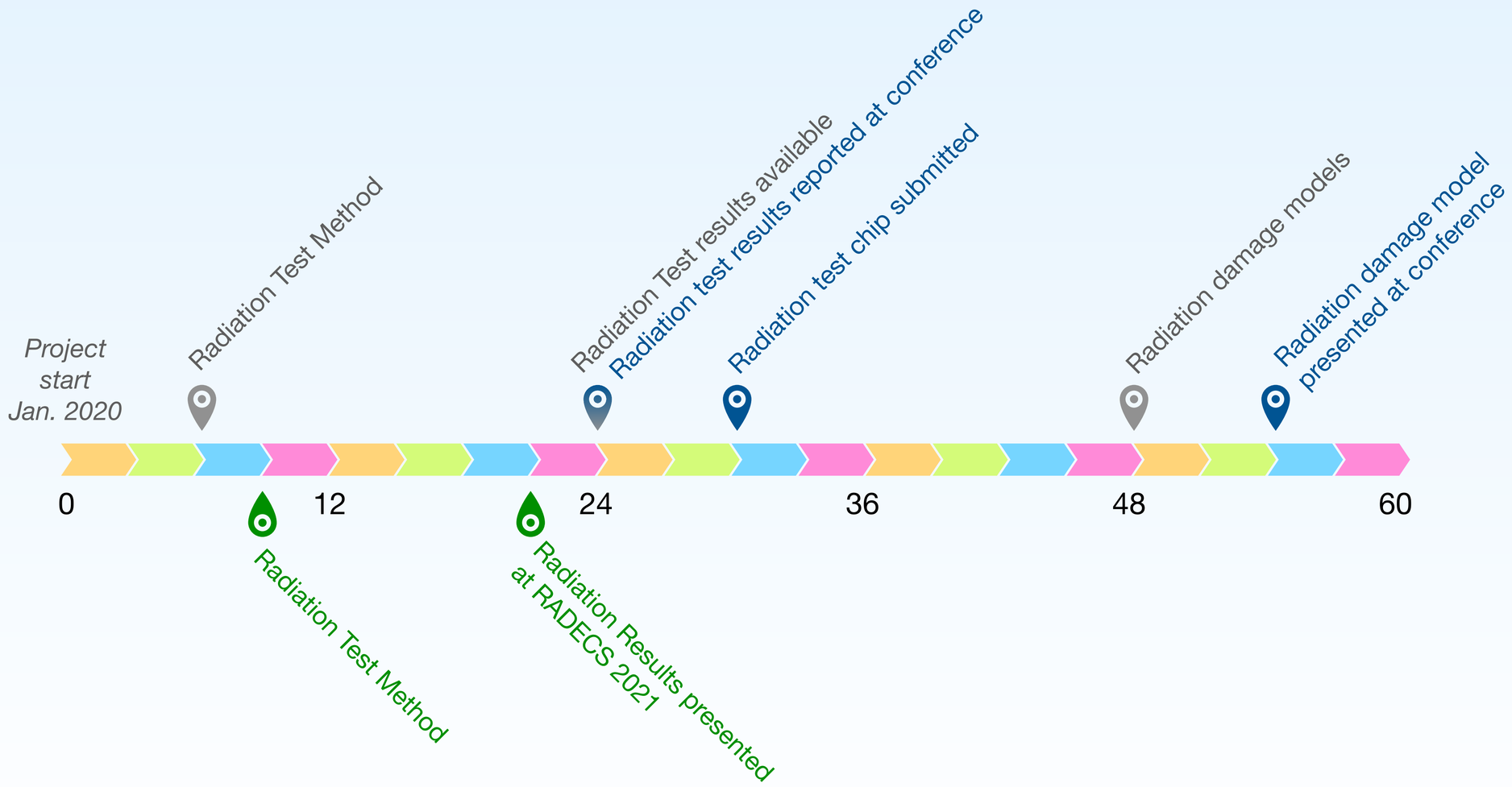
OPTO1 actual vs planned

- Early start enabled by previous project PIC submission



Deliverable
Milestone
Actual

OPTO2 actual vs planned



Deliverable
Milestone
Actual

jan.troska@cern.ch

FPGA task

EP R&D

WP6 High Speed Links

Overview

Methodology

FEC choice and implementation

Data-rates

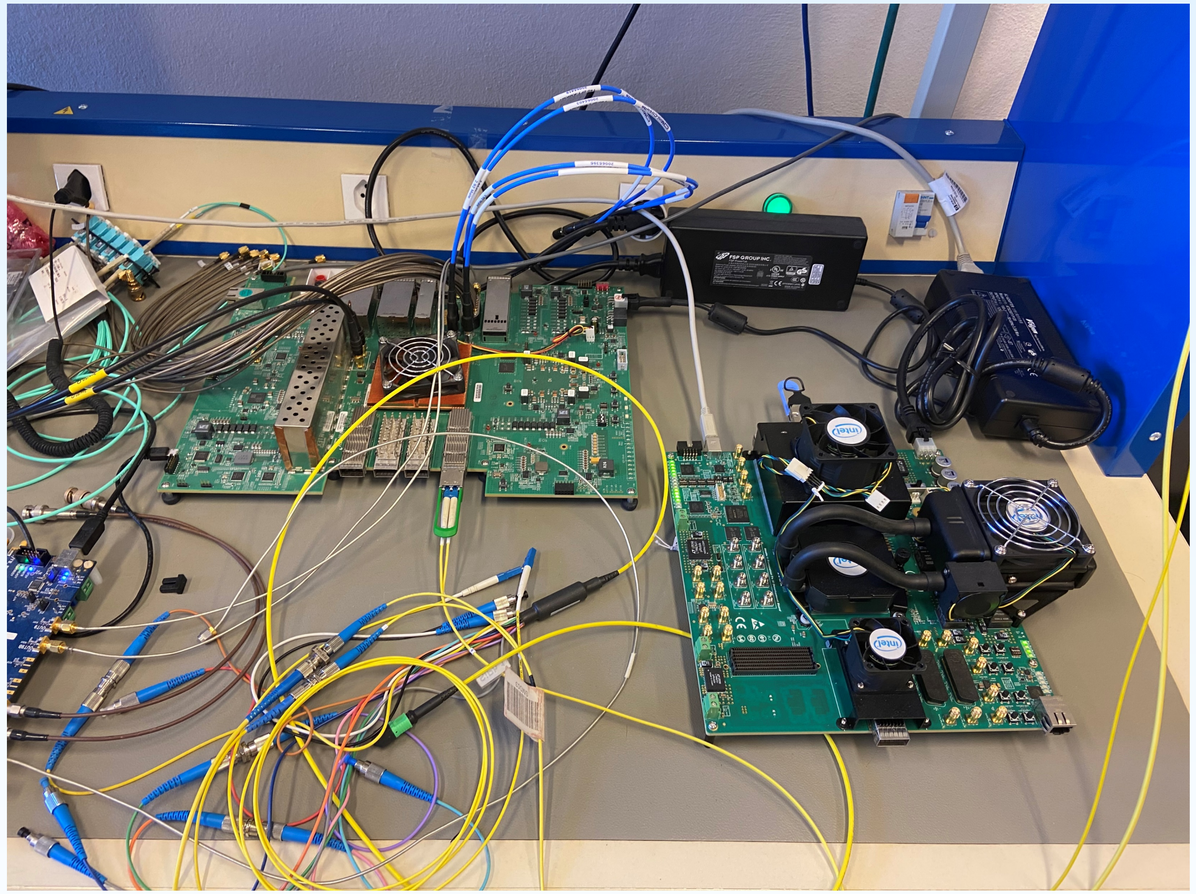
Transceiver module survey

FPGA task overview

- Understanding the High Speed link Market and Technology to answer technical (and existential) questions for the ASIC & Photonics activities:
  - Which Modulation format is most suited to achieving the overall goals of the Project?
    - NRZ, PAM4, …
  - Is Forward Error Correction (FEC) necessary and if so, what kind?
    - Standard vs Custom
  - What target data-rate (per lane, per link)?
    - At high data-rates, Clock and Data Recovery (CDR) circuits present in optical transceiver modules may prevent the use of ‘custom’ (beam synchronous) line rates
  - Which Module types?
    - e.g. QSFP28, QSFP-DD, …
    - Can we meet the optical power budget with custom front-end developments?
  - Which band/wavelengths for CWDM?
    - O-band (around 1310nm) vs C-band (around 1550 nm)
  - How will the Datacom Market evolve? What are the trends?
    - Crystal ball question to try to latch on to more long-lived link standards

FPGA task: Methodology

- Continuous Technology survey
  - FPGAs
  - Commercially available optical transceivers
  - Emerging standards
- Laboratory demonstrations
  - With state-of-the art
    - FPGAs
    - Optical transceivers
    - High end instrumentation
- Continuous feedback to the ASIC and SiPh activities in order to guide technical choices and overall path

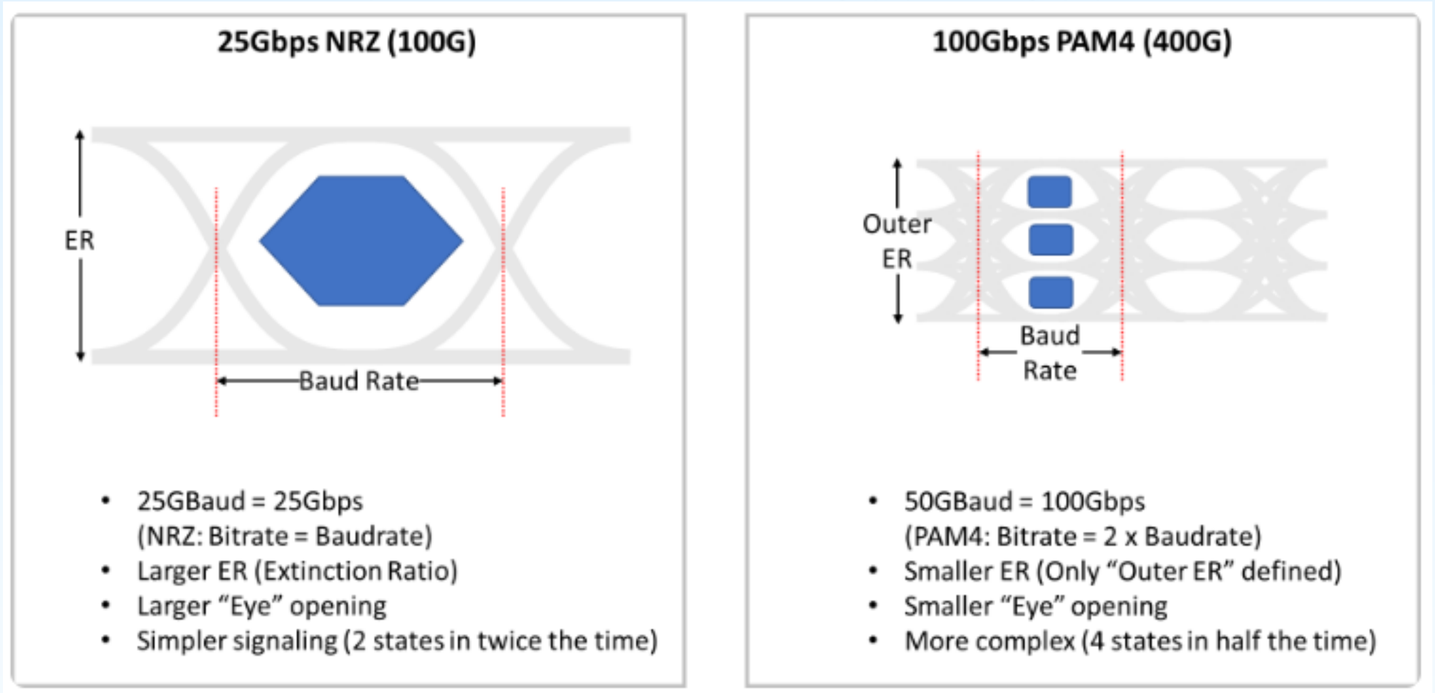


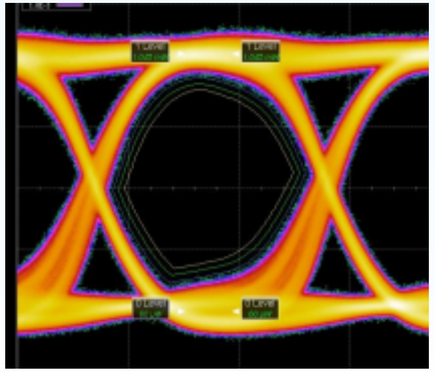
FPGA based demonstrators (left: Xilinx Virtex/AMD Ultrascale+, right: Intel Stratix 10)

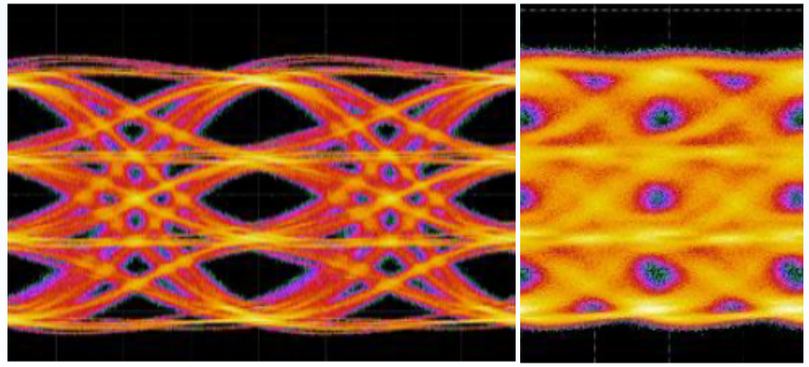
Modulation formats

- Non-Return to Zero (NRZ) vs 4-level Pulse Amplitude Modulation (PAM4)
  - Optical physical layer is SNR-limited at both 28 Gbps NRZ and 56 Gbps PAM4
  - Strong FEC schemes are needed to reach errors rates of below 10^{-9}
    - This is particularly important for PAM4, which comes with an 11-13 dB Signal-to-Noise Ratio (SNR) penalty.

https://www.linkedin.com/pulse/100g-qsfp28-400g-qsfp56-dd-sean-davies/



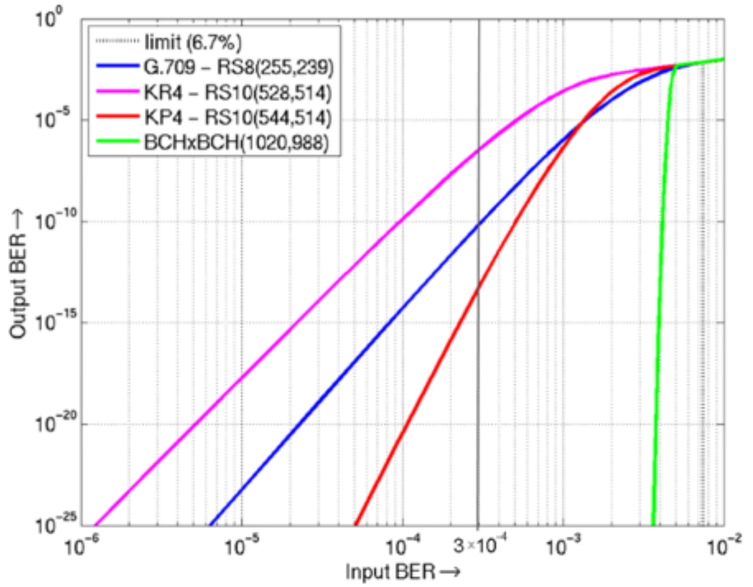


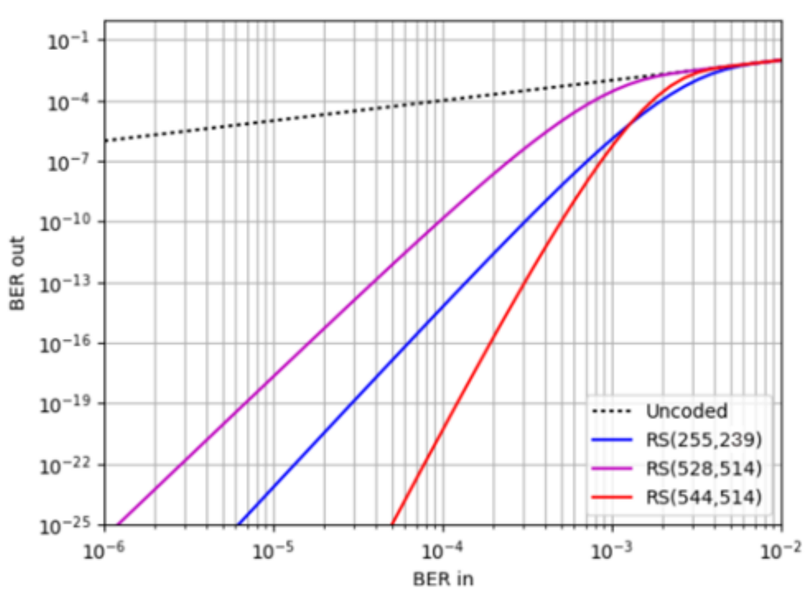


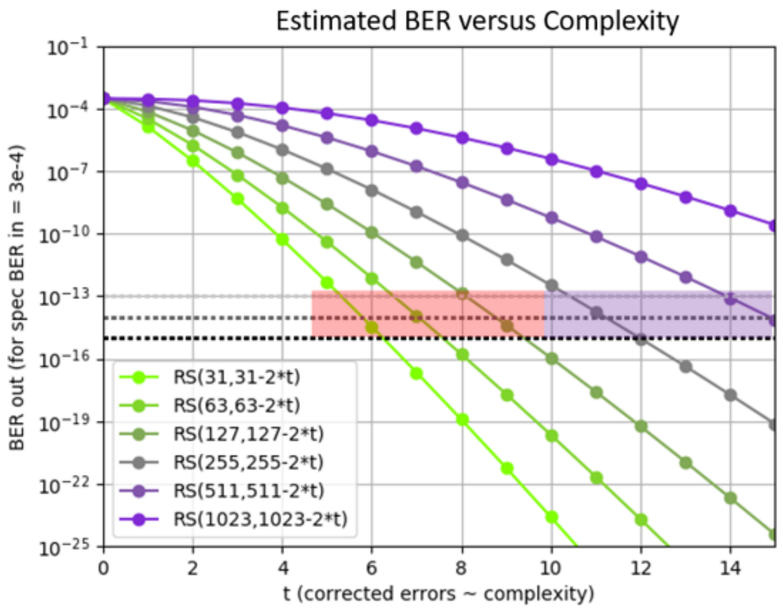
Electrical *Optical*

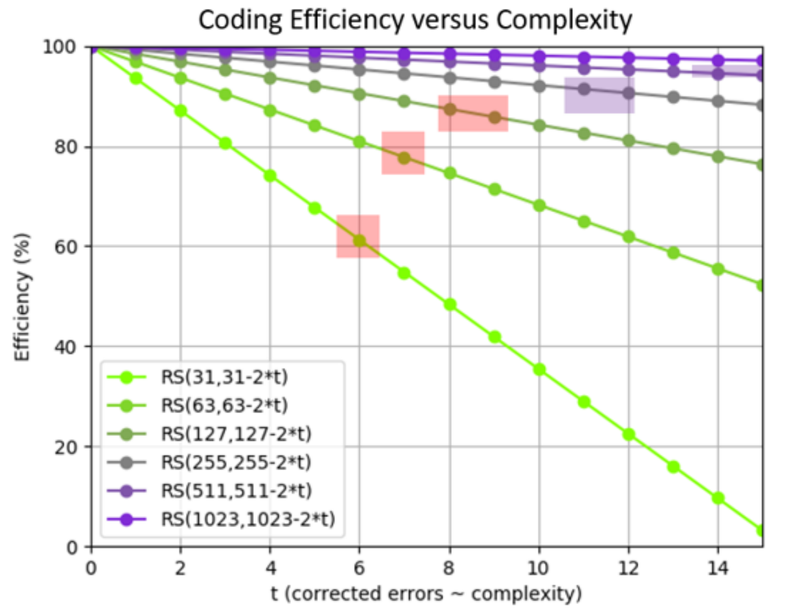
Forward Error Correction modelling

- Reed-Solomon (RS) codes studied for future implementation
- Mathematical modelling of custom FEC candidates for 56 Gbps PAM4
  - compared to the IEEE std. to check validity
- Comparative analysis of the performance of future RS-based FEC schemes to determine the impact of various key parameters
  - symbol number and size
  - correction power/complexity







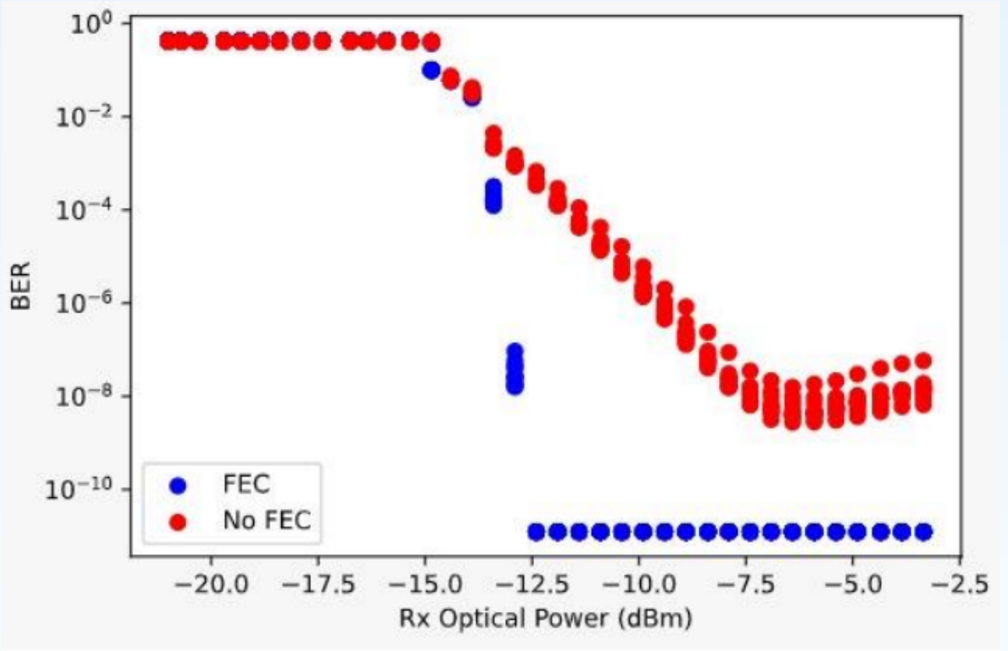


Low complexity Codes = low decoding latency

High complexity Codes = close to PAM-4 popular Codes

FEC implementation

- PAM4 stds. do not impose a FEC scheme
  - IEEE KP4 currently most popular
    - Reed-Solomon RS(544,514), corrects up to 15 10-bit symbols
    - Estimated coding gain of 6.1 dB
    - Hardware-IP for both Intel and Xilinx eases implementation
    - Decoding latency “long”, not considered as a criterion for now
- Both transmission (ASIC) and reception (Back-end) implemented
  - Hard-IP blocks in FPGAs
  - COTS optical transceiver modules
- Full chain was studied in loopback to assess:
  - Coding gain
  - Latency
    - 460 ns including a few meters of fibre.
      - KP4 frame is already responsible for 97 ns latency, even without considering the decoding process.

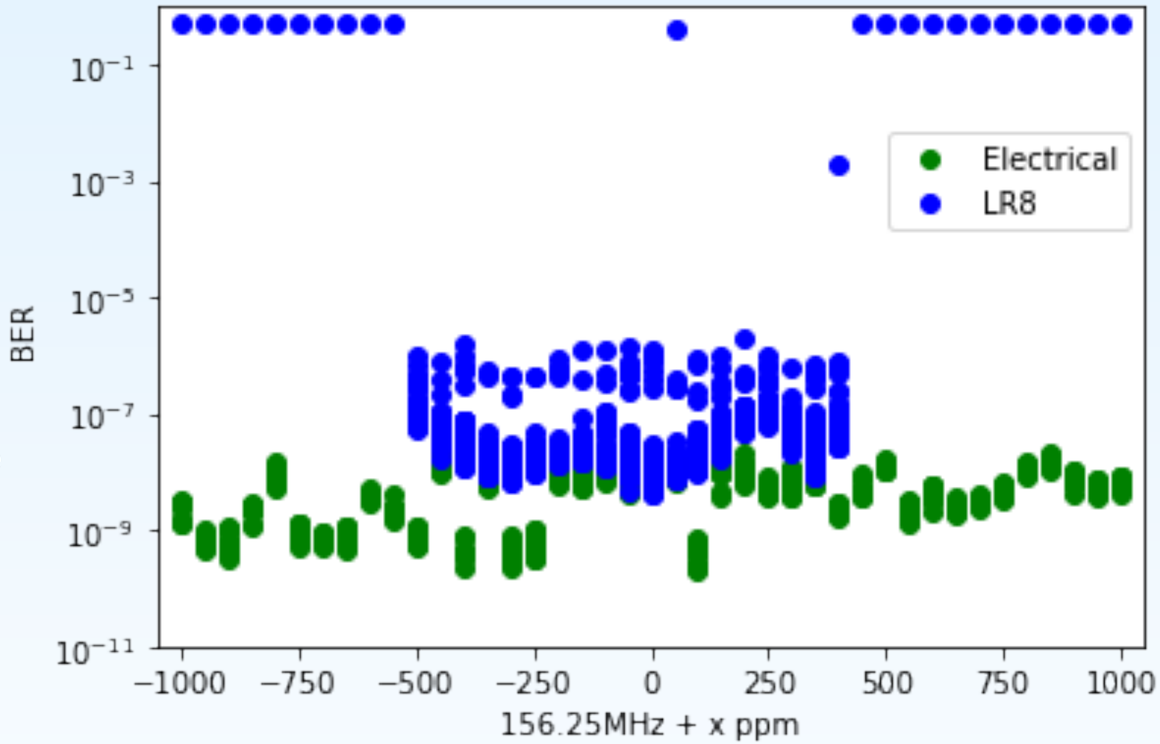


Bit Error Rate of the KP4 PAM-4 link implemented in WP6 proof of concept

jan.troska@cern.ch

Data-rate constraints

- Data transmission synchronous with the LHC collision rate (40.079 MHz) would require operating a PAM4 link at a non-IEEE standard rate (53.125 Gb/s)
- Investigations showed that
  - FPGA transceivers seem to tolerate large rate variations,
  - Most PAM4 transceivers have a very narrow range of data rates (< ±500 ppm) which does not cover any integer multiples of the Bunch Clock frequency (i.e. 1325 or 1326 times 40.079 MHz).
- This would preclude the traditional FE approach in HEP of using synchronous systems operating at a multiple of the bunch clock frequency
  - A Bunch-clock synchronous interface model for a disruptive link type based on asynchronous PAM-4 transmission is being evaluated in VHDL
  - A study of the optical transceiver market to identify modules that allow their Clock and Data Recovery (CDR) circuits to be bypassed



Locking range of Virtex Ultrascale+ GTM transceiver (green) and PAM-4 LR8 module (blue).

Study of the optical transceiver market

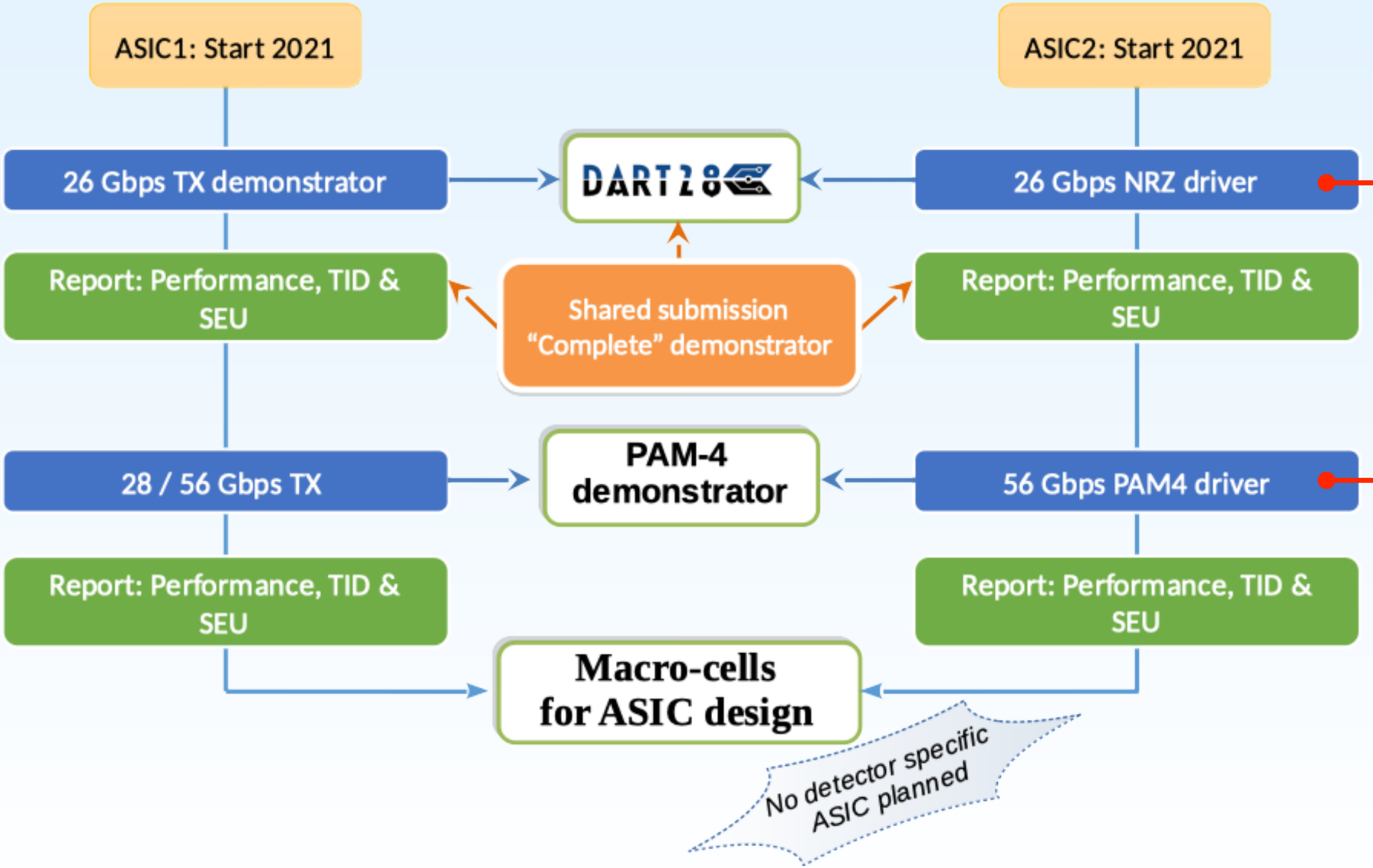
- The market is still rapidly evolving, new ‘standards’ are published every quarter and early adopters (GAFAM) implement own standards
  - Manufacturers have two development paths: single source not-interoperable fast-track; and IEEE standardised slower development
- Overall, this leads to a ‘zoo’ of module types, from which we distilled some trends
  - 56G PAM4 modules: still evolving; inflexible line rates; expensive; FEC required
  - 28G NRZ modules: more stable; flexible line rates possible; less expensive; possibly lighter FEC
  - Tx-side is most expensive and not needed in a typical FE link for HEP: possible customisation?
  - Most transceivers operate in O-band (~1310 nm): re-target SiPh efforts to this wavelength

ASIC design

EP R&D
WP6 High Speed Links

Introduction and ASIC roadmap
DART28 Test Chip
DART28NRZ High Speed Transmitter
ASIC Conclusions

ASIC Roadmap



- Synergy with WP5
  - 28 nm technology
- SiPh co-integration (wire-bond)

- PAM4 signalling
  - doubling the data-rate
- SiPh co-integration (flip-chip)

DART28NRZ Test Chip

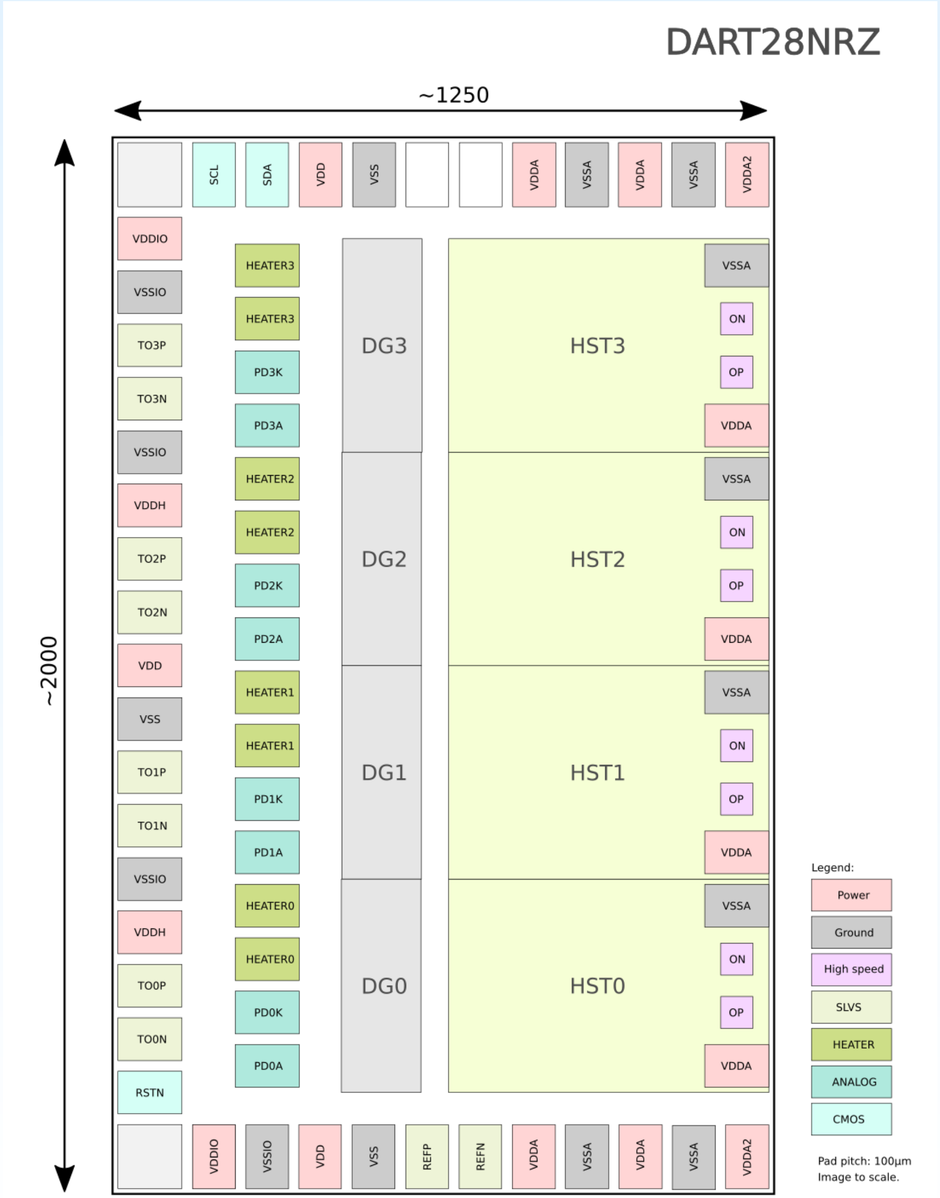
DART28 (**D**emonstrator **A**SIC for **R**adiation-Tolerant **T**ransmitter in **28**nm)

Goals:

- Demonstration of a NRZ transmitter
  - Using embedded data generators
- Radiation hardness
- SiPh PICs co-integration
- Flexible test structure

Chip architecture:

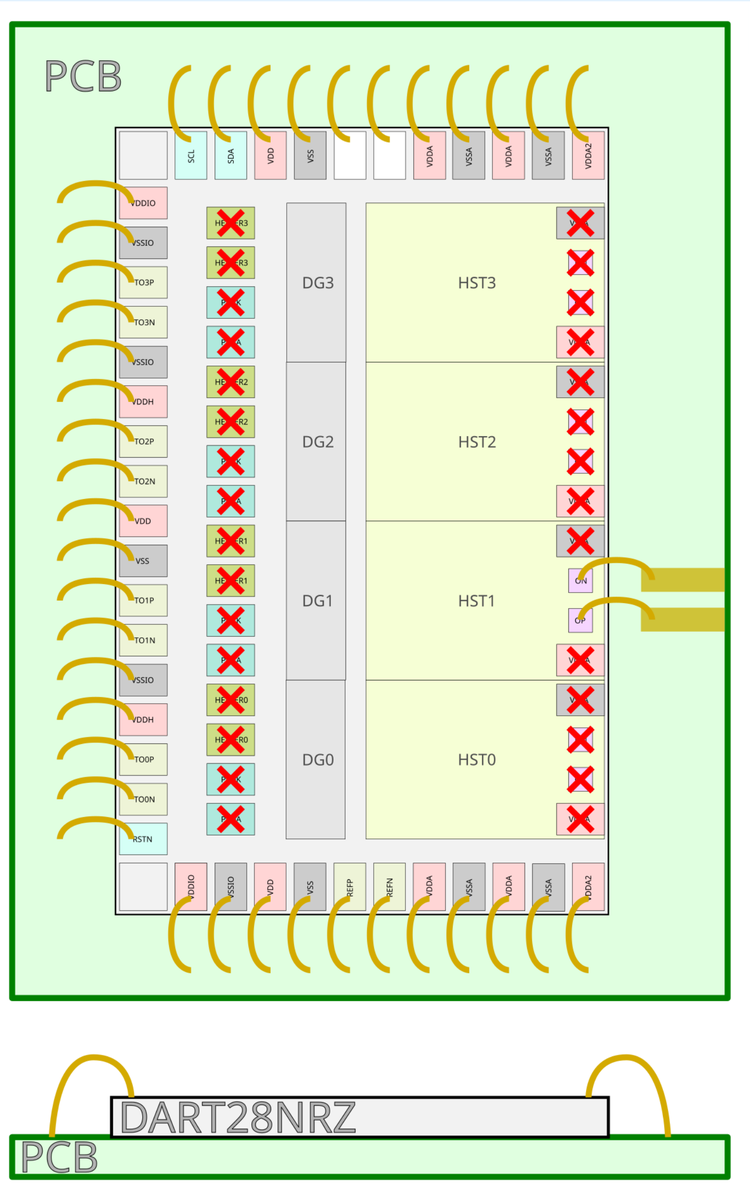
- Four high speed transmitters (HST) blocks:
  - Two 100 Ω line drivers
  - Two ring modulator drivers
- Data generators (DG)
- IO pads:
  - High speed signals
  - Control signals



DART28NRZ Test Chip

Electrical high speed transmission using a 100 Ω transmission line:

- Functional testing
- Performance characterization across voltage/ temperature
- Tests in radiation environment:
  - TID (X-ray)
  - SEU (Heavy Ion / Laser)



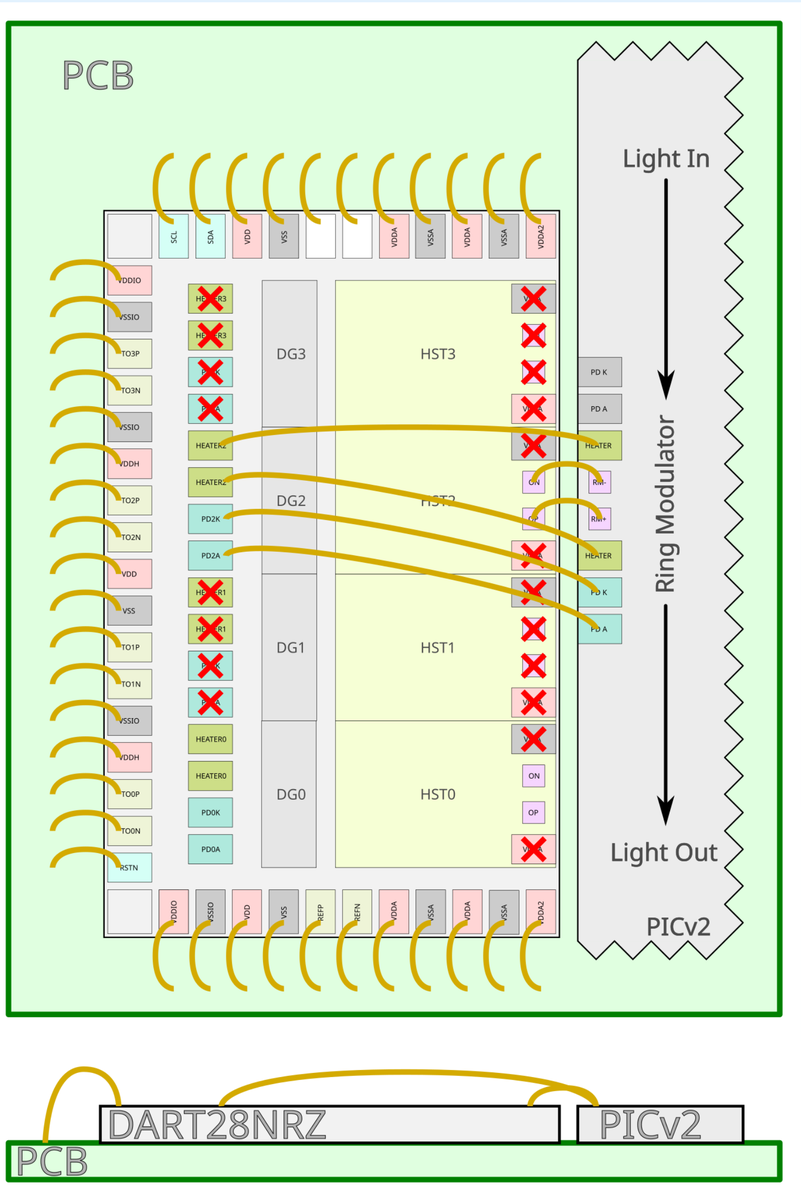
DART28NRZ Test Chip

Electrical high speed transmission using a 100 Ω transmission line:

- Functional testing
- Performance characterization across voltage/temperature
- Tests in radiation environment:
  - TID (X-ray)
  - SEU (Heavy Ion / Laser)

Optical high speed transmitter – single channel:

- Demonstrate SiPh integration, end-to-end optical link



mateusz.baszczyk@cern.ch

DART28NRZ Test Chip

Electrical high speed transmission using a 100 Ω transmission line:

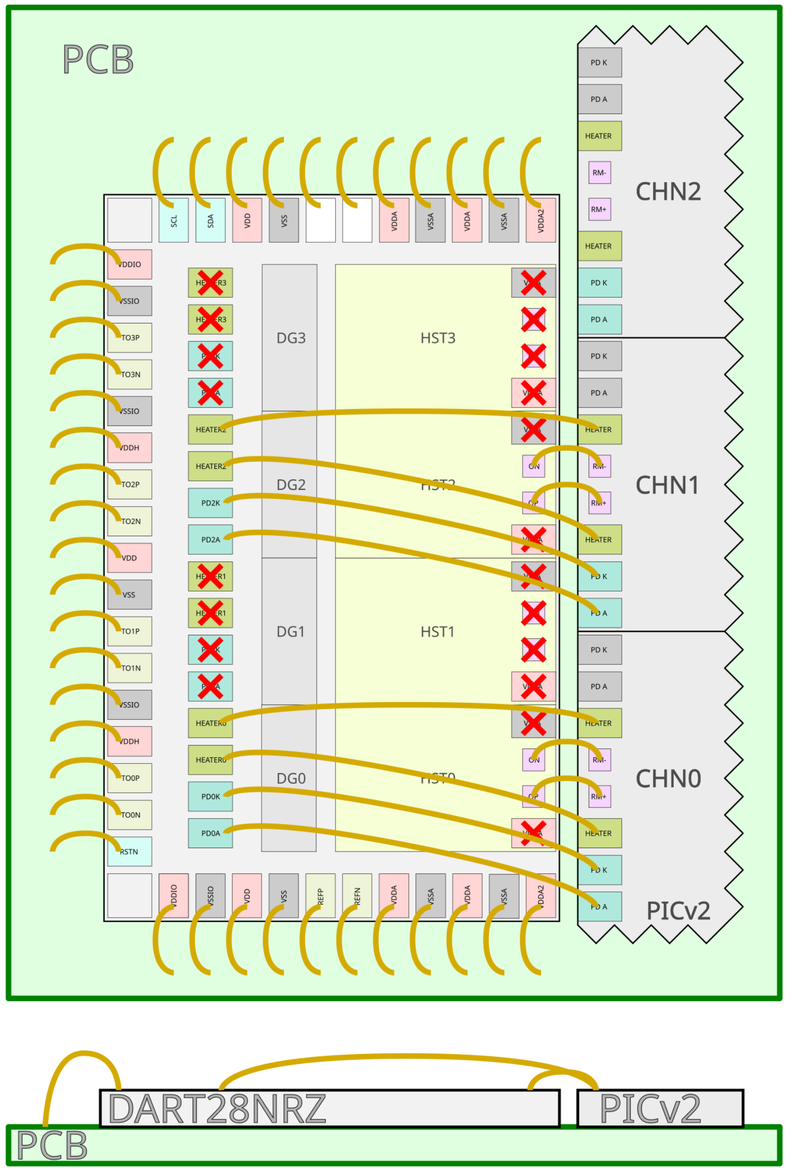
- Functional testing
- Performance characterization across voltage/temperature
- Tests in radiation environment:
  - TID (X-ray)
  - SEU (Heavy Ion / Laser)

Optical high speed transmitter – single channel:

- Demonstrate SiPh integration, end-to-end optical link

Optical high speed transmitter – dual channel Wavelength-division multiplexing (WDM):

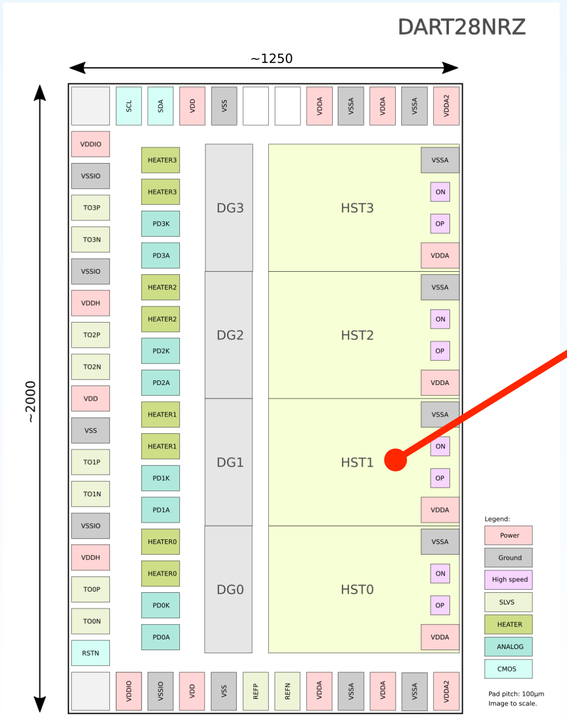
- Demonstrate two NRZ links on one fiber using existing PICv2

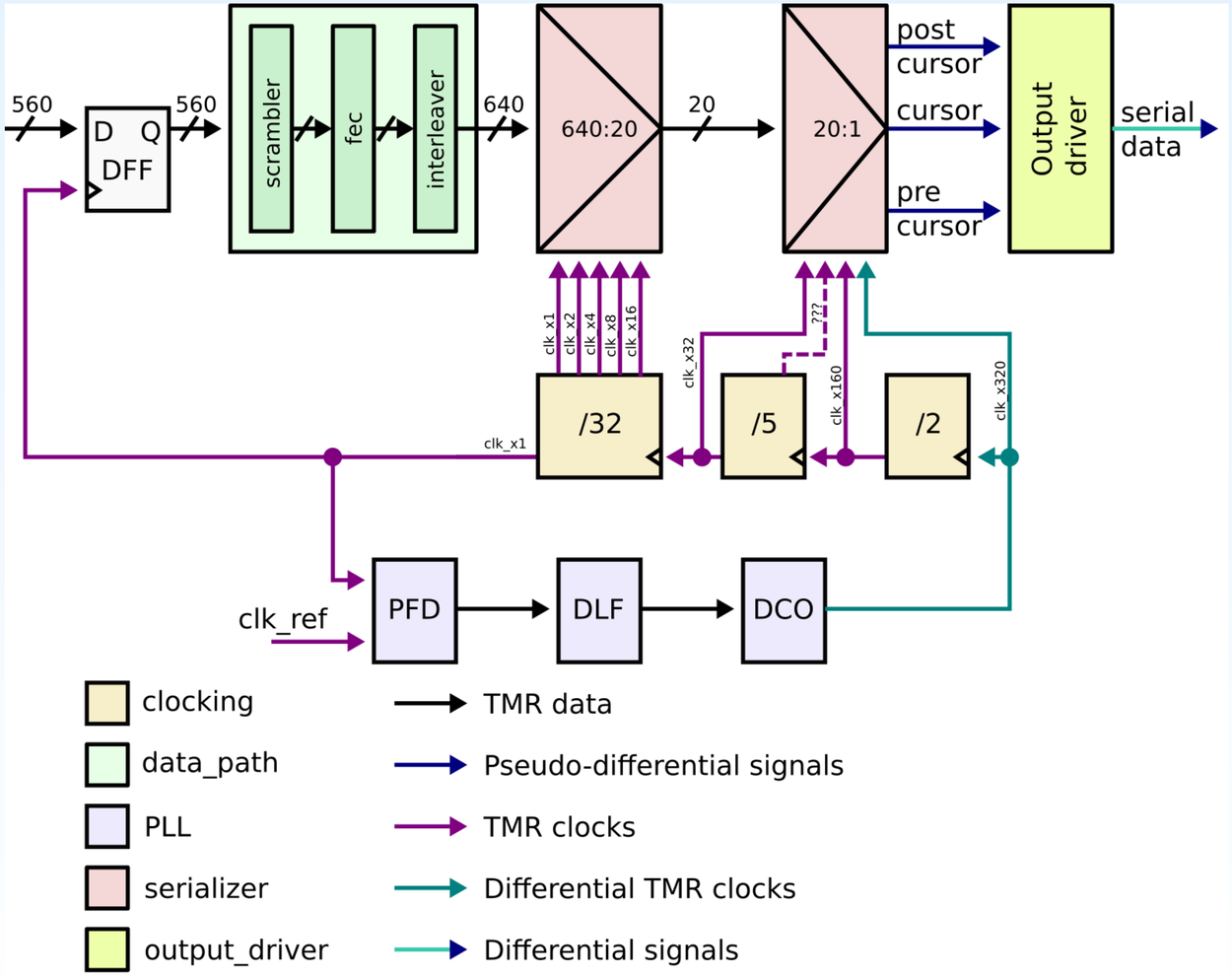


DART28NRZ High Speed Transmitter

Structure of the high speed transmitter path:

- Data path
- High-frequency PLL
- Clock generation
- High-speed Serializer
- Output driver



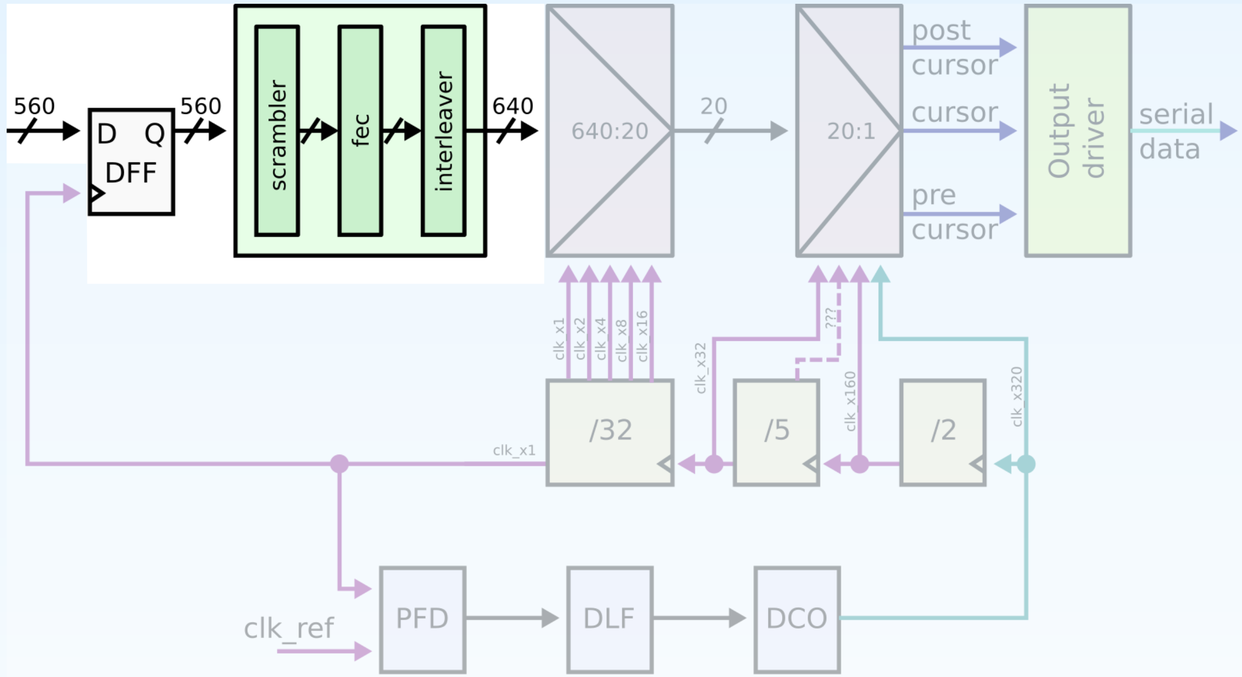


DART28NRZ/high_speed_transmitter

High Speed Transmitter – data path

Data path structure:

- Scrambler for DC balancing of data
- Forward error correction (FEC): Reed Solomon (31, 29) code
- Interleaver to improve burst error resiliency
- Accepts 560 user data bits per frame
- Produces 640 output data bits per frame
- Payload bit rate: 22.44 Gbps



Integrated Design-for-Test features:

- PRBS / fixed pattern generation
- Error injection
- Flag injection (for latency measurements)

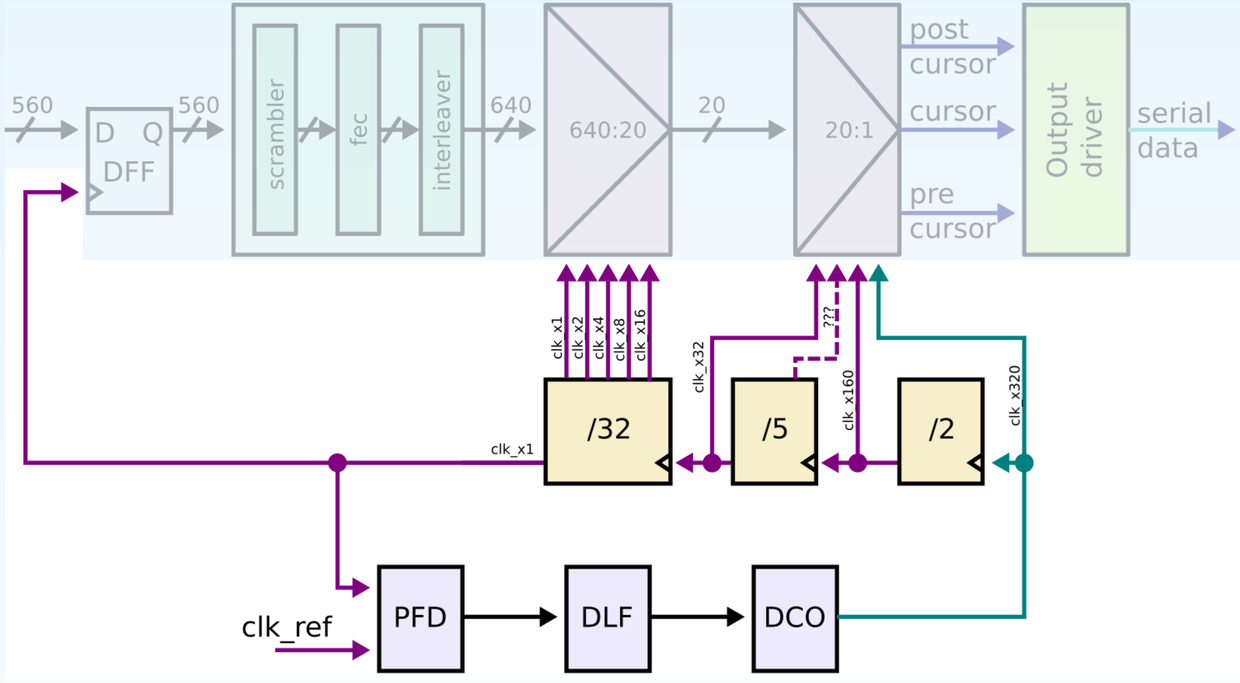
mateusz.baszczyk@cern.ch

HST – PLL + clock generation system

PLL provides high-speed and low jitter clock and it is accompanied by a clock generation system.

Design considerations:

- A half-rate serializer requires generation of 12.8 GHz clock
- NRZ transmitter uses highly synchronous clocking architecture:
  - f_{LHC} x 640 ≈ 25.650 Gbps (1 UI ≈ 40 ps)
- Stringent jitter requirement: below 1 ps rms
- LC oscillator for low-jitter local clock generation
  - All-Digital PLL architecture (minimizing required analog circuitry)
- TMR dividers shared between PLL and serializer



Design challenges: Clock duty-cycle distortion

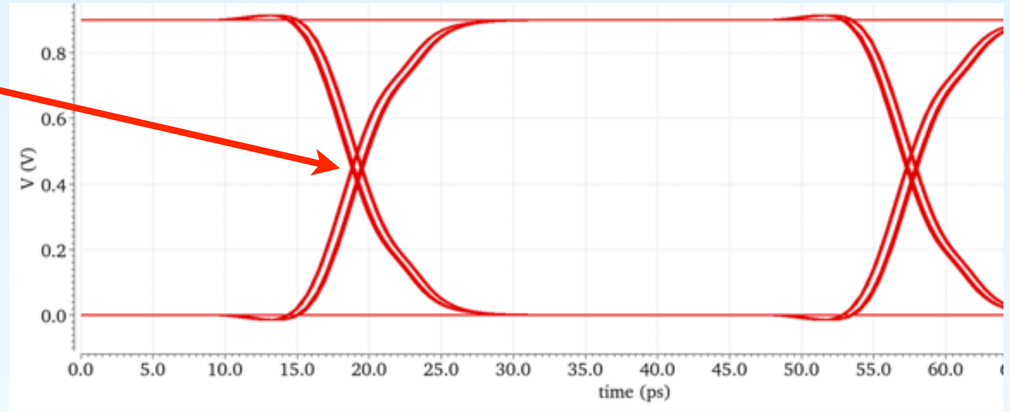
Clock duty cycle distortion (DCD) converts into Even-Odd Data Jitter (in a ½ rate serializer architecture):

- Specification for NRZ: 0.035 UI (~1.36 ps)
- Challenging to meet the specs over Process, Voltage, Temperature (PVT) variations and TID

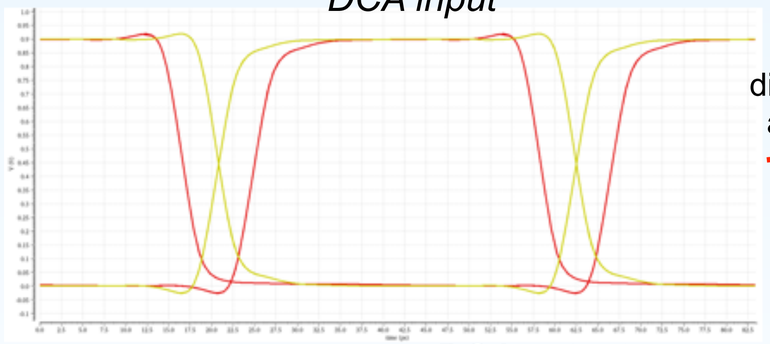
Adopted solution:
Digital Duty Cycle Adjustment (DCA):

- Drive strength adjustable inverter stages
- On-chip measurement and control
- Tuning range ±6% with 200fs resolution

Serializer eye diagram with even-odd jitter

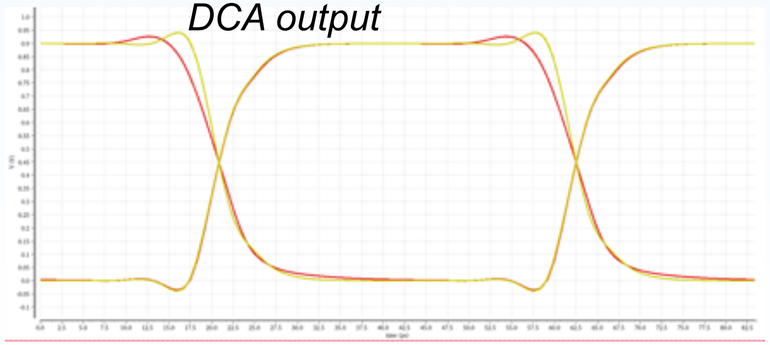


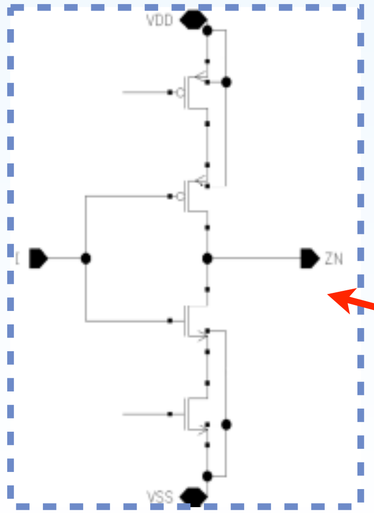
DCA input

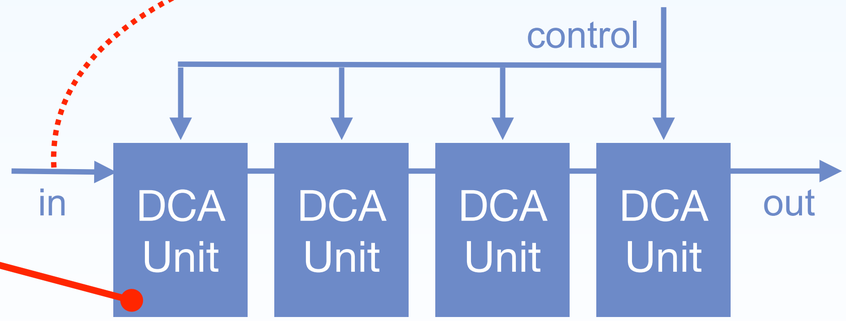


Two signals with different duty cycle are tuned to have the same performance

DCA output





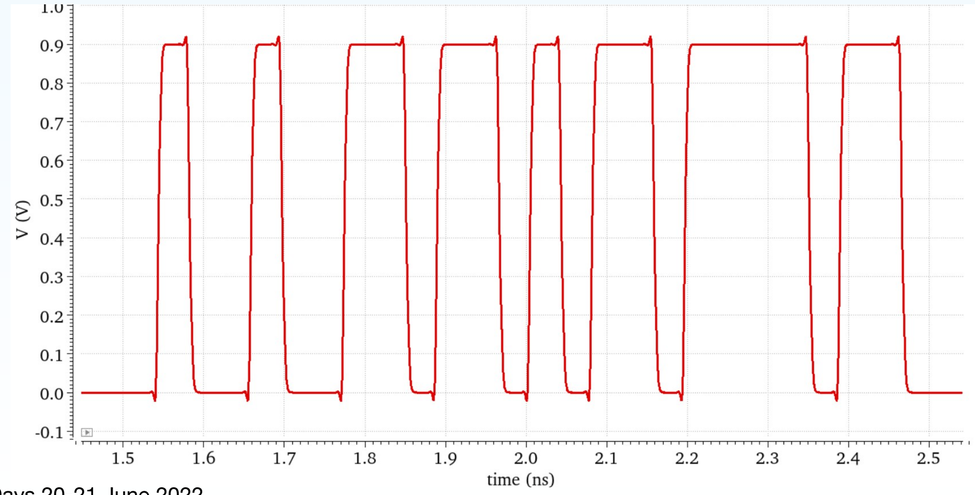


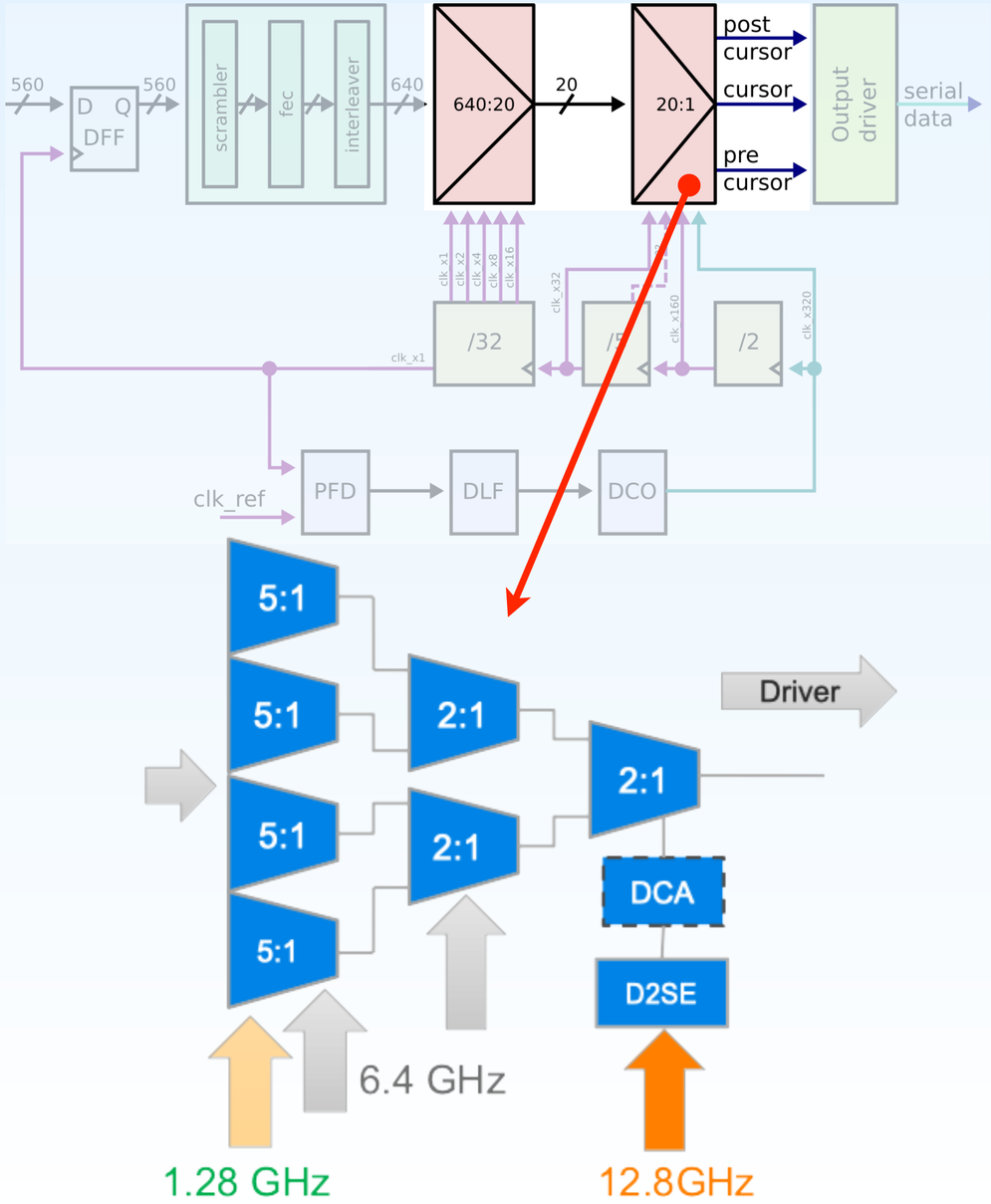
HST – Serialiser

The serializer converts parallel data into high speed serial data stream.

It consists of:

- Low-speed serializer (640:20), 40 MHz – 1.28 GHz
  - Digital design flow methodology used
- High-speed serializer (20:1), 1.28 GHz – 12.8 GHz
  - High data rate
  - Full-custom design flow used
    - Careful design of clock and data distribution, balanced layout, etc
  - Stringent specifications for duty cycle distortion and even-odd jitter performance (<1.36 ps)



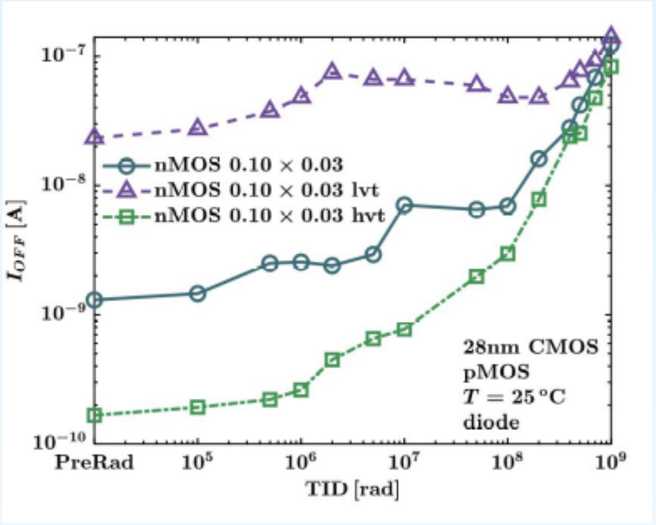


mateusz.baszczyk@cern.ch

Design challenges: Sub-threshold leakage

Transistor is never in an off state which implies a leakage current I_{off}

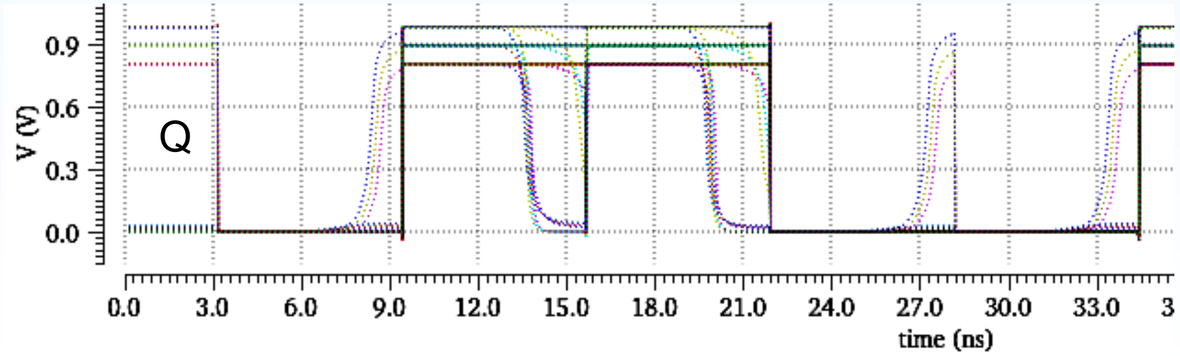
- PVT variation:
  - I_{off} can change over 3 orders of magnitude
- Radiation:
  - I_{off} increases with TID also up to 3 orders of magnitude



Credit: G. Borghello (EP-ESE-ME) WP5

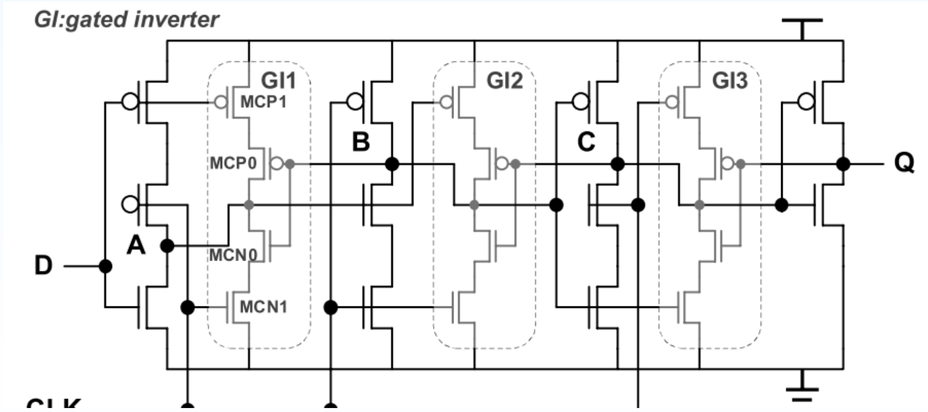
An example of the leakage at the system level:

- A dynamic true single-phase clocked (TSPC) flip-flop:
  - Faster than conventional FF
  - Used in high speed part of HST
  - Sensitive to leakage - Q outputs should be a square signal



Adopted solution:

- Inclusion of gated inverter feedback



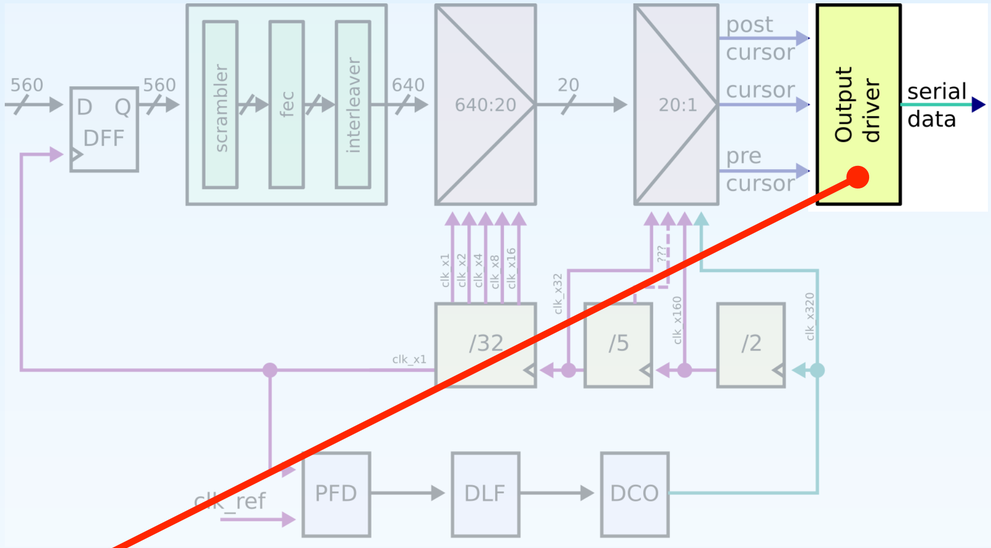
Ref: Lee et al: “A true single-phase clocked flip-flop with leakage current compensation” (2012)

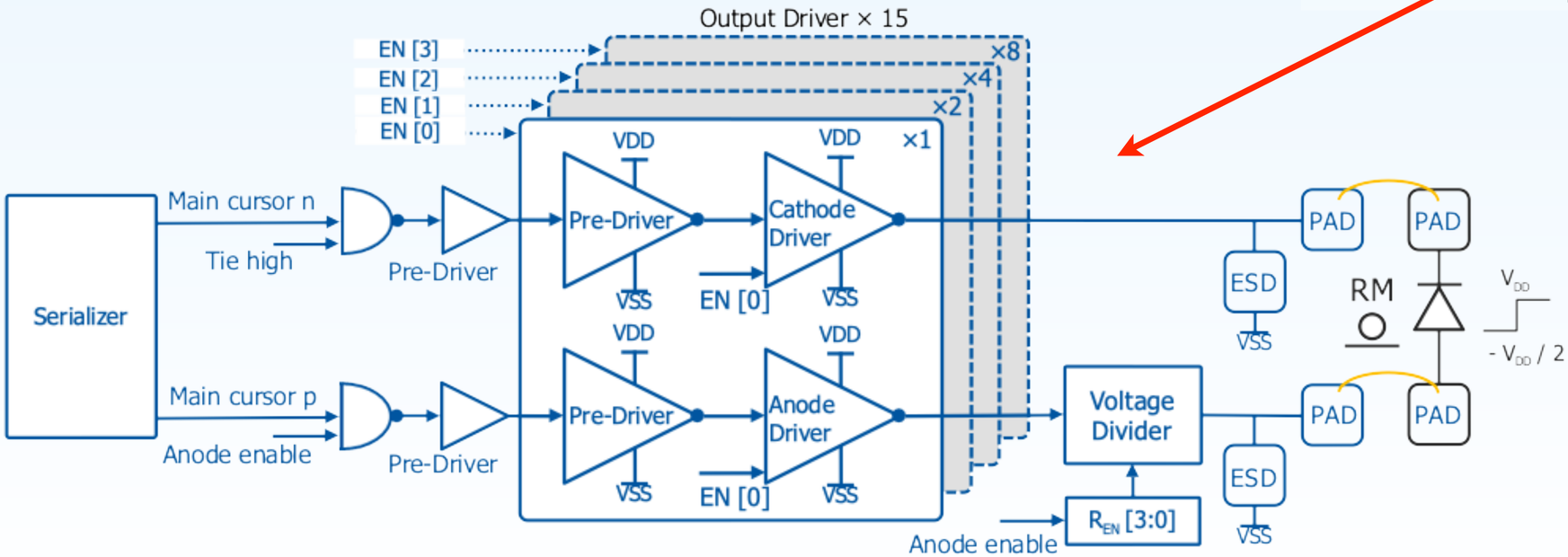
HST – Ring Modulator Driver

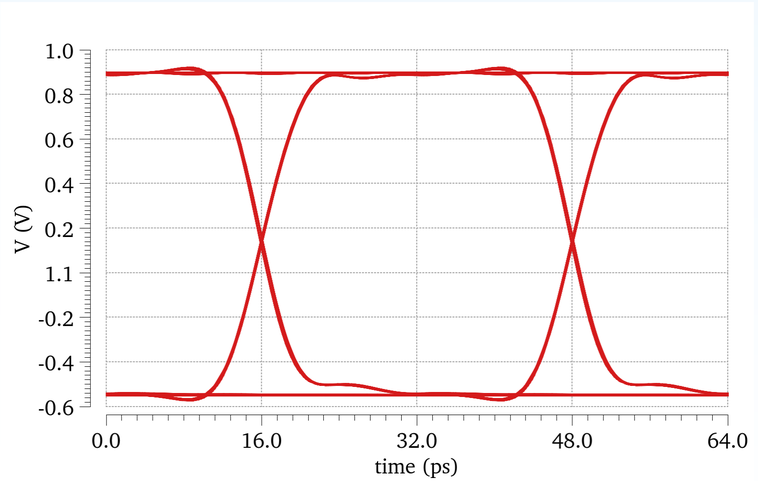
It is designed to drive a ring modulator on SiPh IC.

Architecture:

- Pseudo-Differential Inverter Driver
- Symmetric drivers for Anode + Cathode
- Segmented for current control (PVT)
- Programmable voltage divider on Anode to limit forward-biasing of the ring modulator

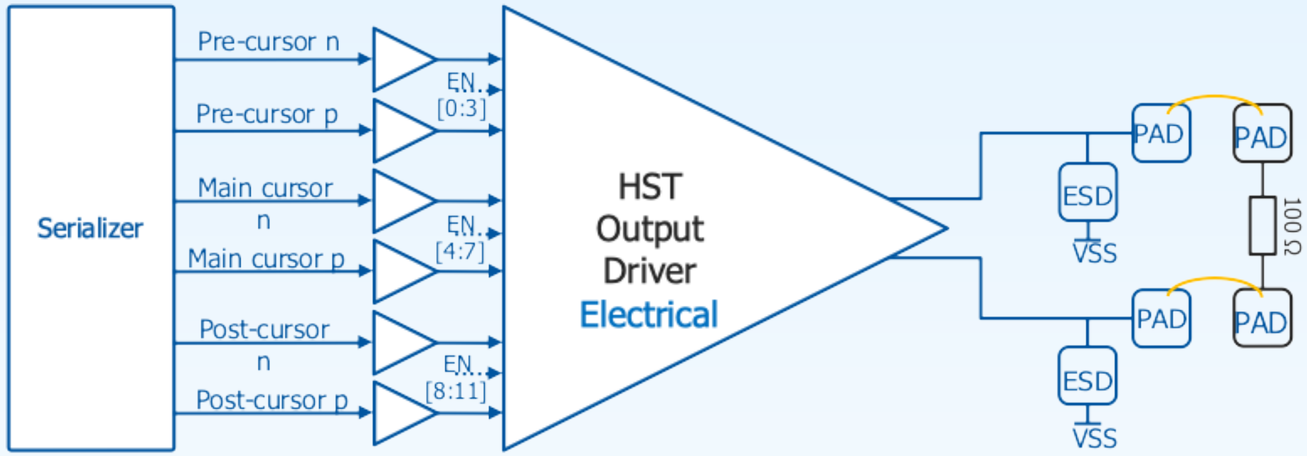




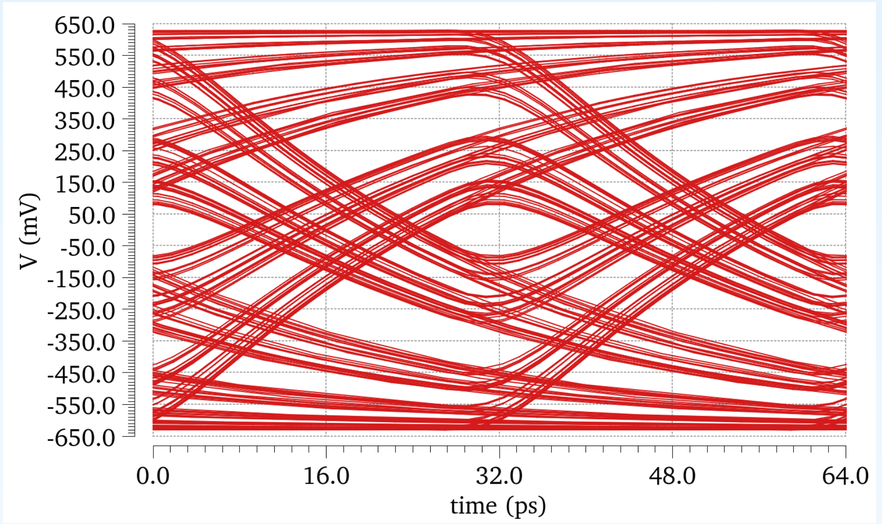


Design Challenges: output driver

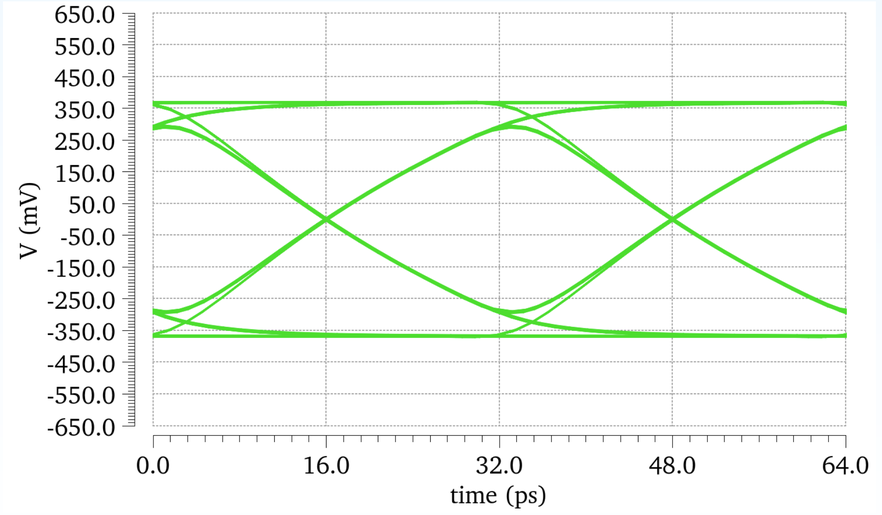
100 Ω line driver with a preemphasis circuit: increasing the output bandwidth while minimizing the intersymbol interference (ISI) in bandwidth-limited channels



Eye diagram without pre-emphasis @32Gbps

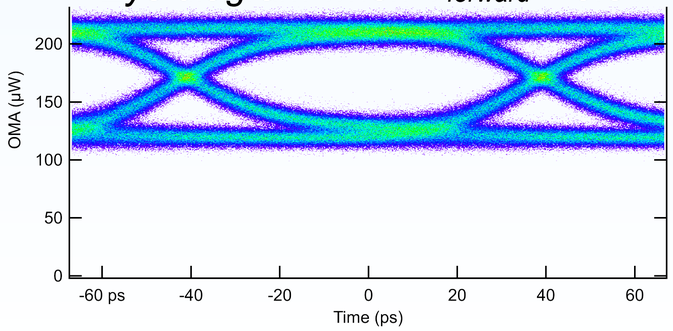


Eye diagram with pre-emphasis @32Gbps

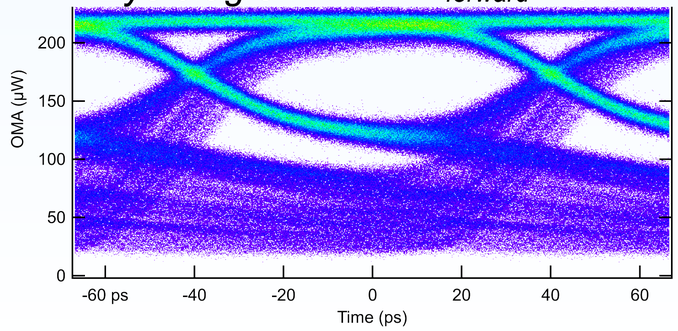


Ring modulator driver: maximizing the driving amplitude, while limiting forward-bias of the ring modulator:

Eye diagram when $V_{forward}$ = 0.5V

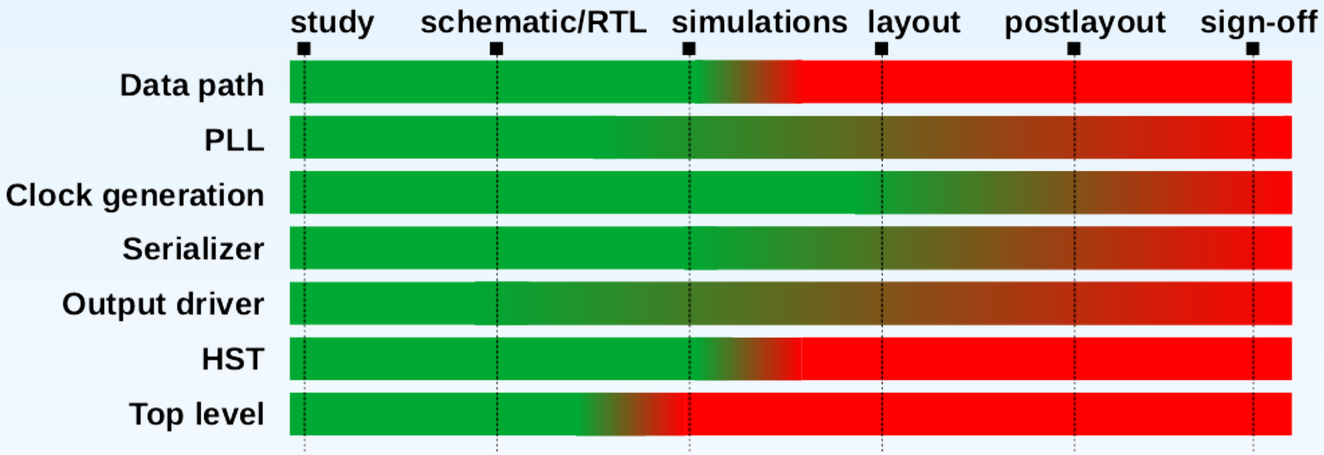


Eye diagram when $V_{forward}$ = 0.9V



Status of DART28NRZ Test Chip

- Submission target: end of 2022 (depends on mini@sic schedule)
- Design status:



Very good progress. Large experience gained:

- Requirements (data rates)
- Performance of the technology:
  - Many thousands of design rules
  - Heavy verification: Large PVT variations, Electro-Migration (EM), Resistive Voltage drop (IR)
  - Low supply voltage (challenge for the opto-electronics circuits driver)
- Design process / PDK (both analog and digital flow)

Opto: Silicon Photonics

EP R&D

WP6 High Speed Links

Overview

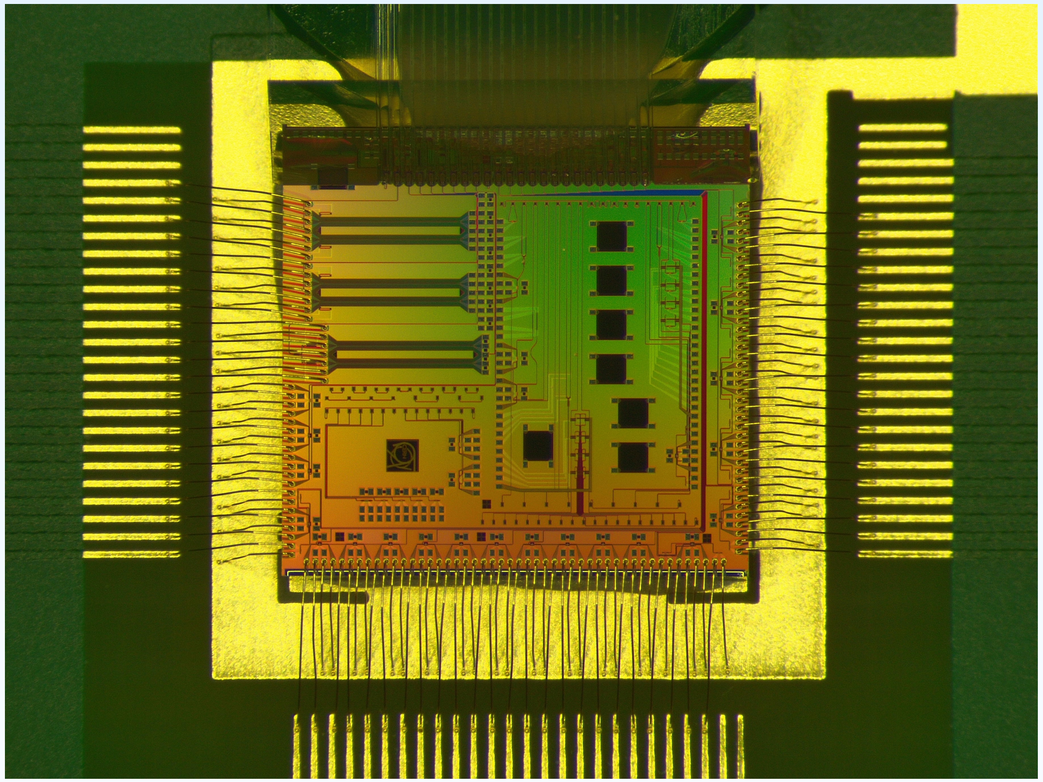
Temperature control

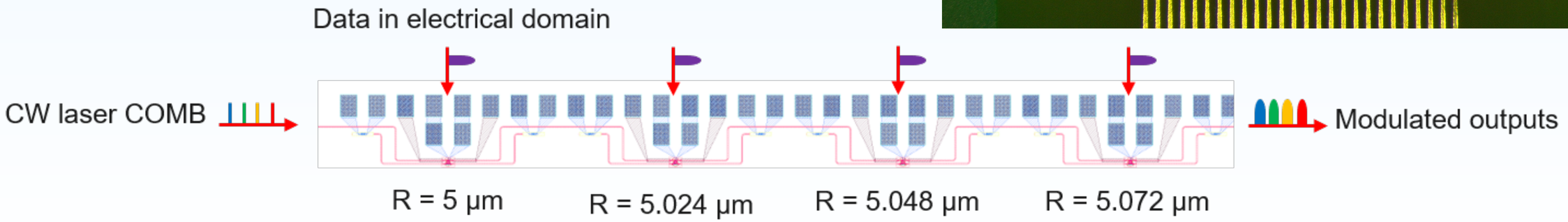
System demonstrators

Radiation effects

Silicon Photonics Overview

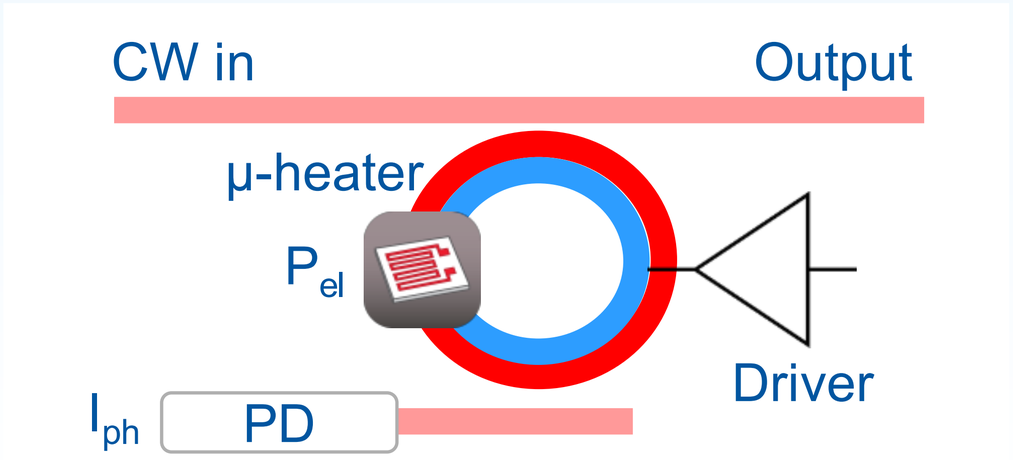
- Exploiting full potential of most recent Photonic Integrated Circuit (PIC)
  - Large number of different modulator designs
    - Ring Modulators, Mach-Zehnder Modulators
    - Many with built-in micro-heaters for circuit control
  - Different photodiode designs
  - System demonstrator for 4-wavelength system
  - Various test structures:
    - Polarisation diversity
    - Doping levels
    - Waveguide loss

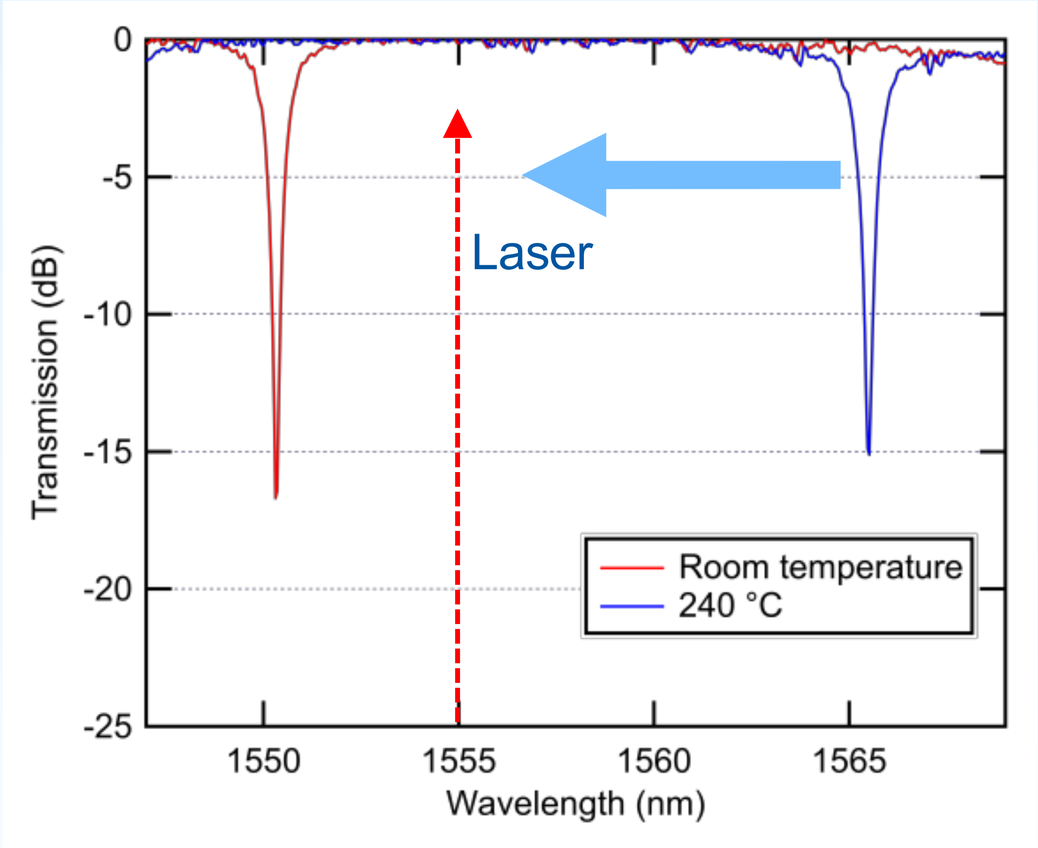




Wavelength control with Micro-heaters

- Ring modulators are highly selective wavelength filters
  - Centre wavelength depends on environmental and fabrication parameters
  - Need mechanism to control individual rings to the wavelength we would like to modulate
  - Resistive heating elements patterned directly on top of ring, providing very localised control of the silicon temperature and thus the refractive index
    - Monitored via a built-in photodiode

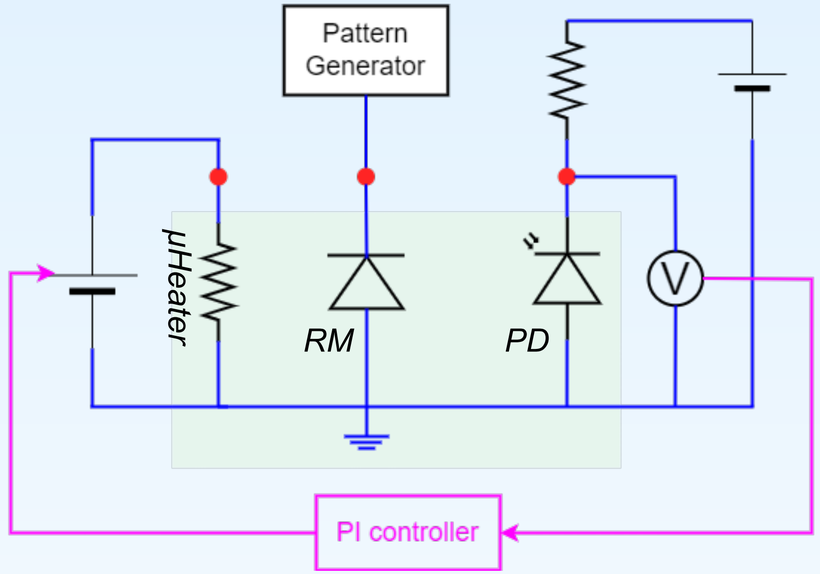


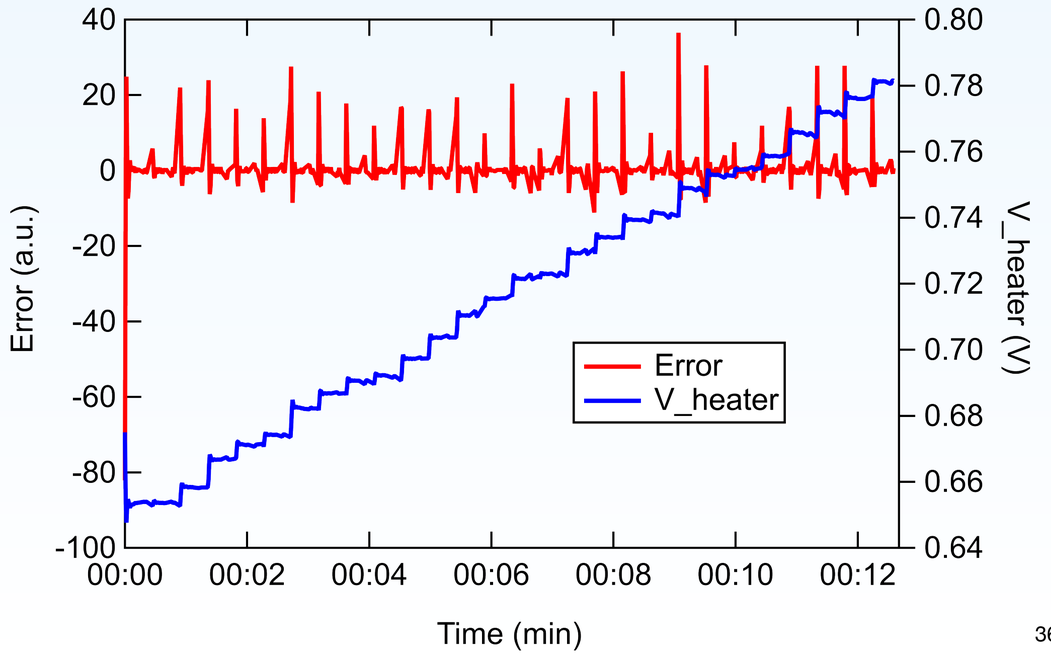


large range of tuneability available

Control system for wavelength stabilisation

- Goal is to create a system that can automatically lock a given ring to the input light of a given wavelength
  - Eventually this controller should be integrated into the ring modulator driver ASIC (c.f. DART28)
- First need to determine the parameters of the controller
  - Implemented a system based on lab instruments
    - Measurement of Photodiode Current
    - Steering of Heater current
- Have demonstrated reasonable stability
  - Tested by changing the input wavelength, which is equivalent to changing device temperature but more easily controlled

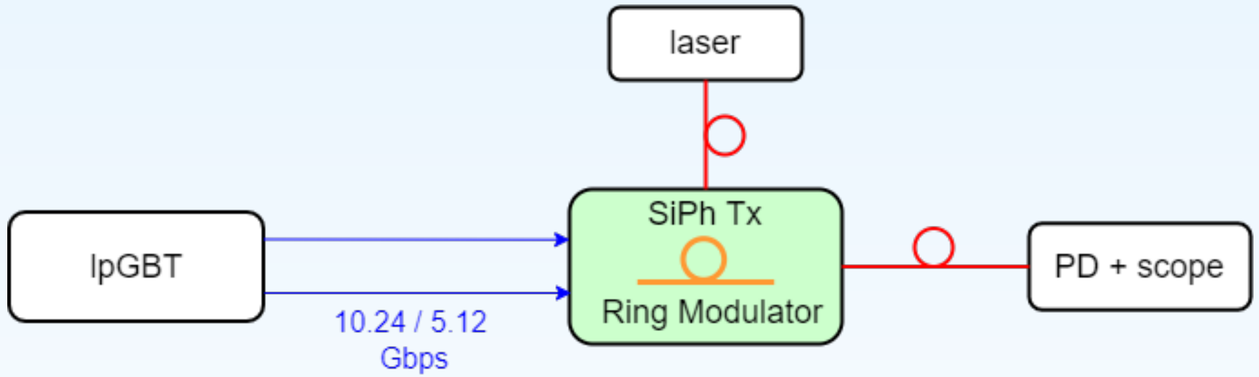


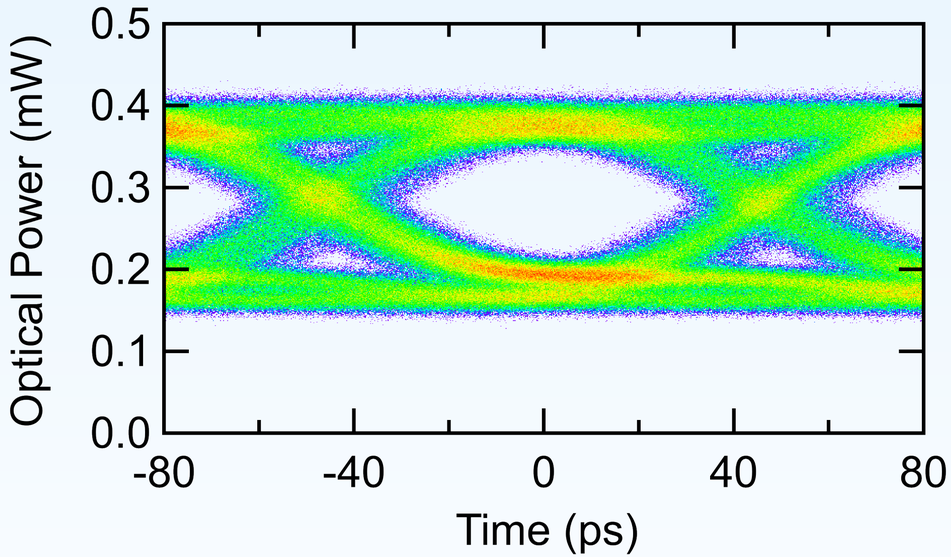


jan.troska@cern.ch

Performance Demo: lpGBT as driver

- First system demonstration carried out using lpGBT as driver while dedicated ring modulator driver is being designed
  - CML output driver of lpGBT sufficient for driving at 10.24 Gb/s

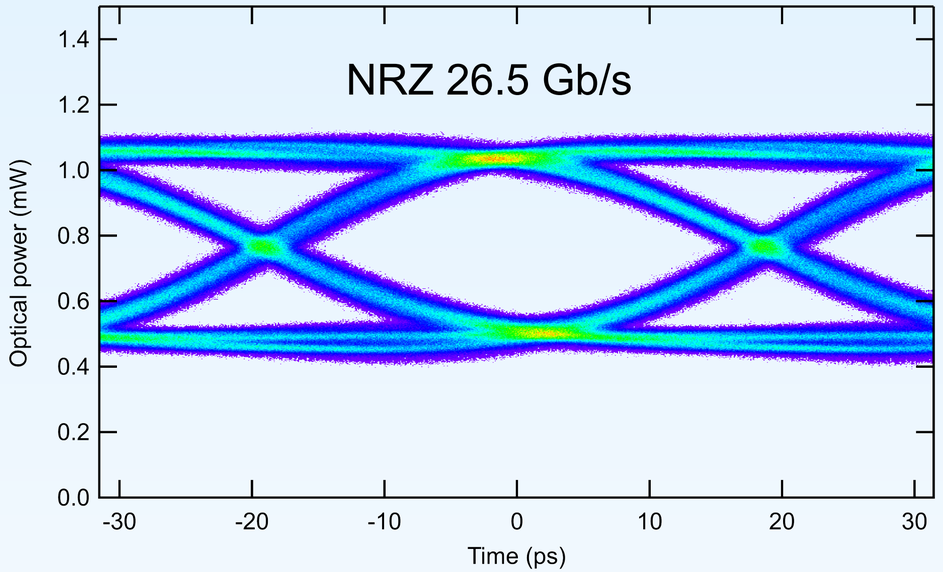


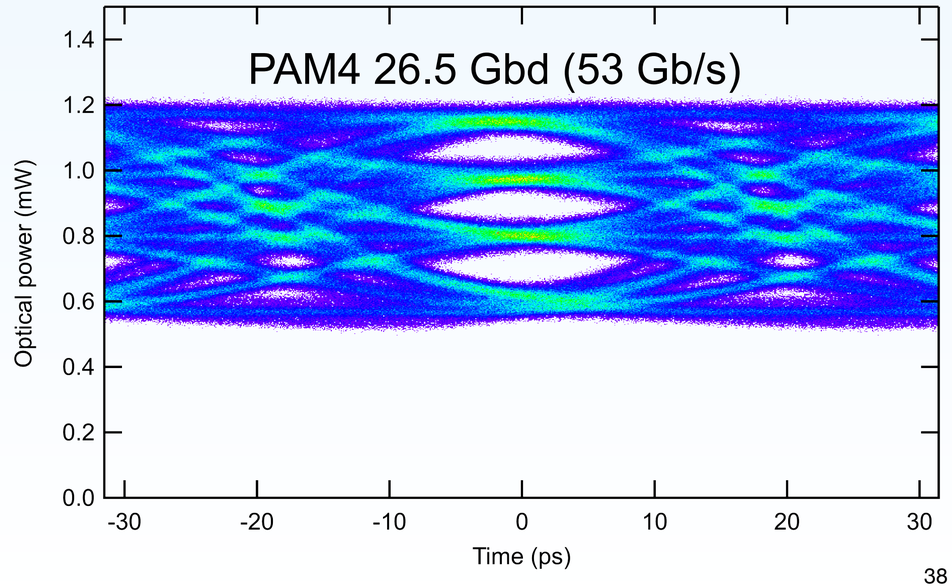


- Timing/Control path from Back-end to Front-end also demonstrated using existing ASIC (GBTIA) coupled to integrated photodiode
  - Reported at TWEPP by Thenia Prousalidi

Performance Demo: 25/50G

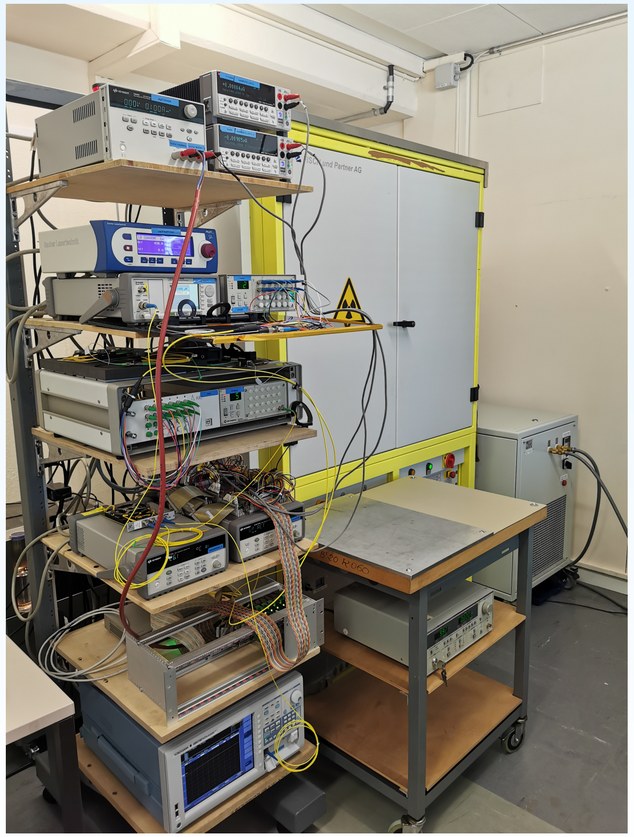
- Higher-speed system demonstration possible with commercial modulator drivers and newly acquired test instrumentation
  - Validates performance of the ring modulator designs that achieve good radiation hardness
  - Allows the understanding of the relative performance of different modulator types
    - e.g. O-band (~1310 nm) vs C-band (~1550 nm)
- Successful test required the design of a carrier PCB with high speed trace routing
  - Experience gained will later be valuable also for ASIC testing
- PAM4 is clearly challenging for optoelectronics in terms of SNR
  - Trade-off between optical SNR and electrical driver speed



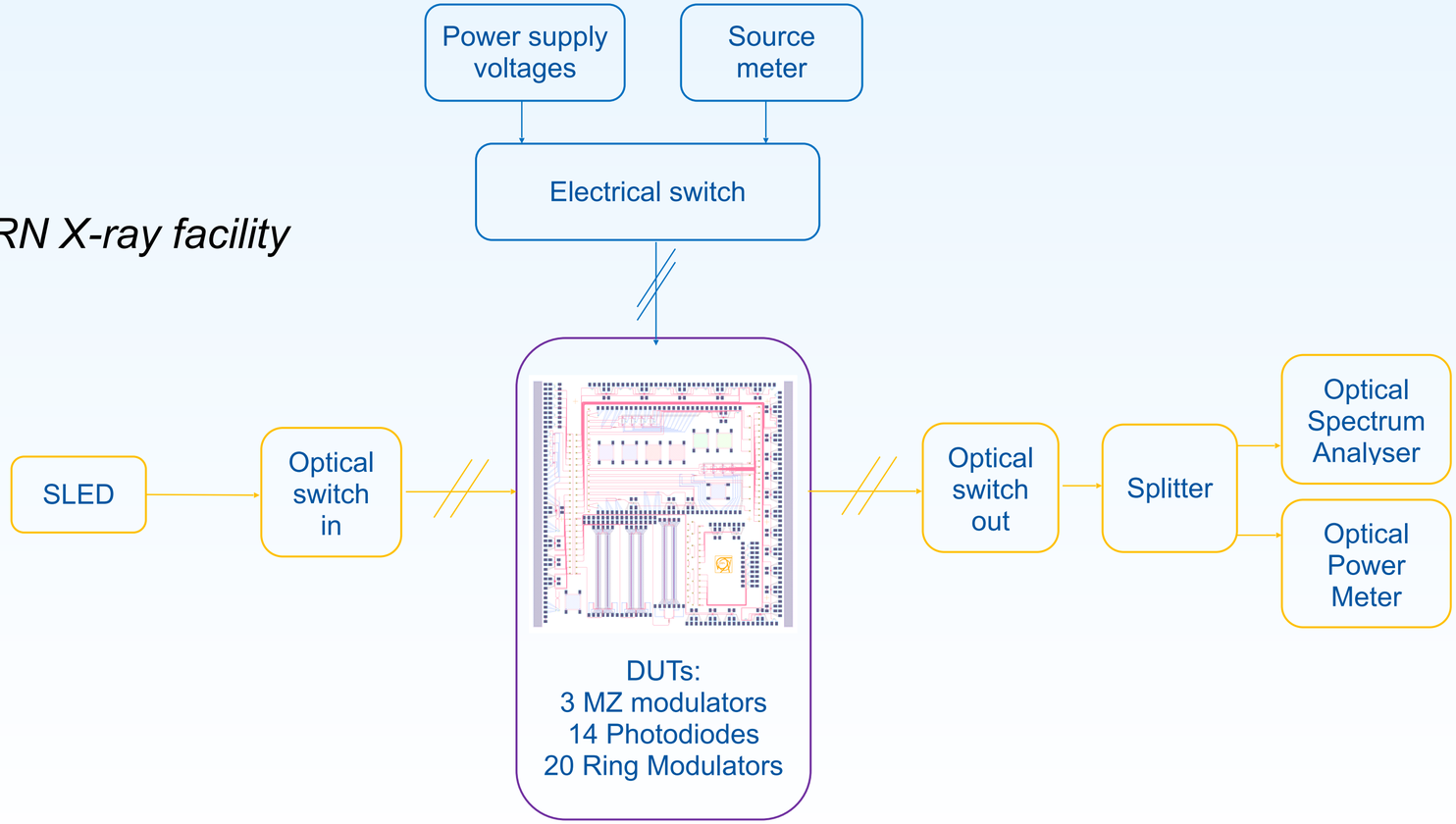


Radiation Testing

- Since we do not yet understand all subtleties of radiation effects of Silicon Photonics devices, carry out extensive testing of effects
  - X-ray at CERN for Total Dose, Neutrons at UCL (B) for Total Fluence



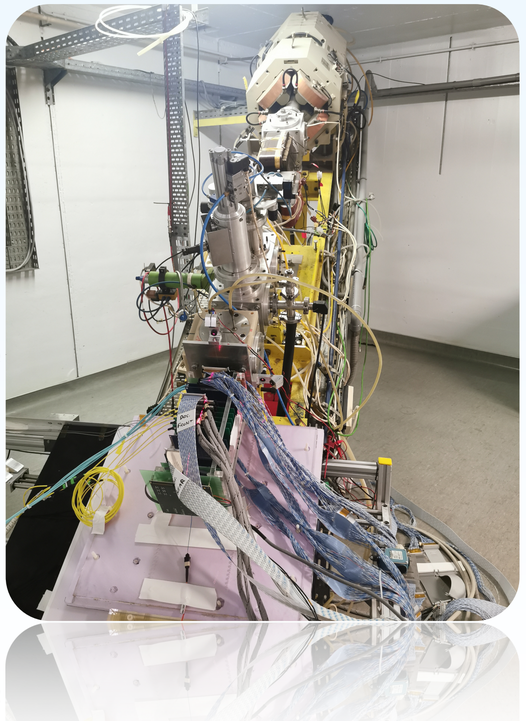
CERN X-ray facility

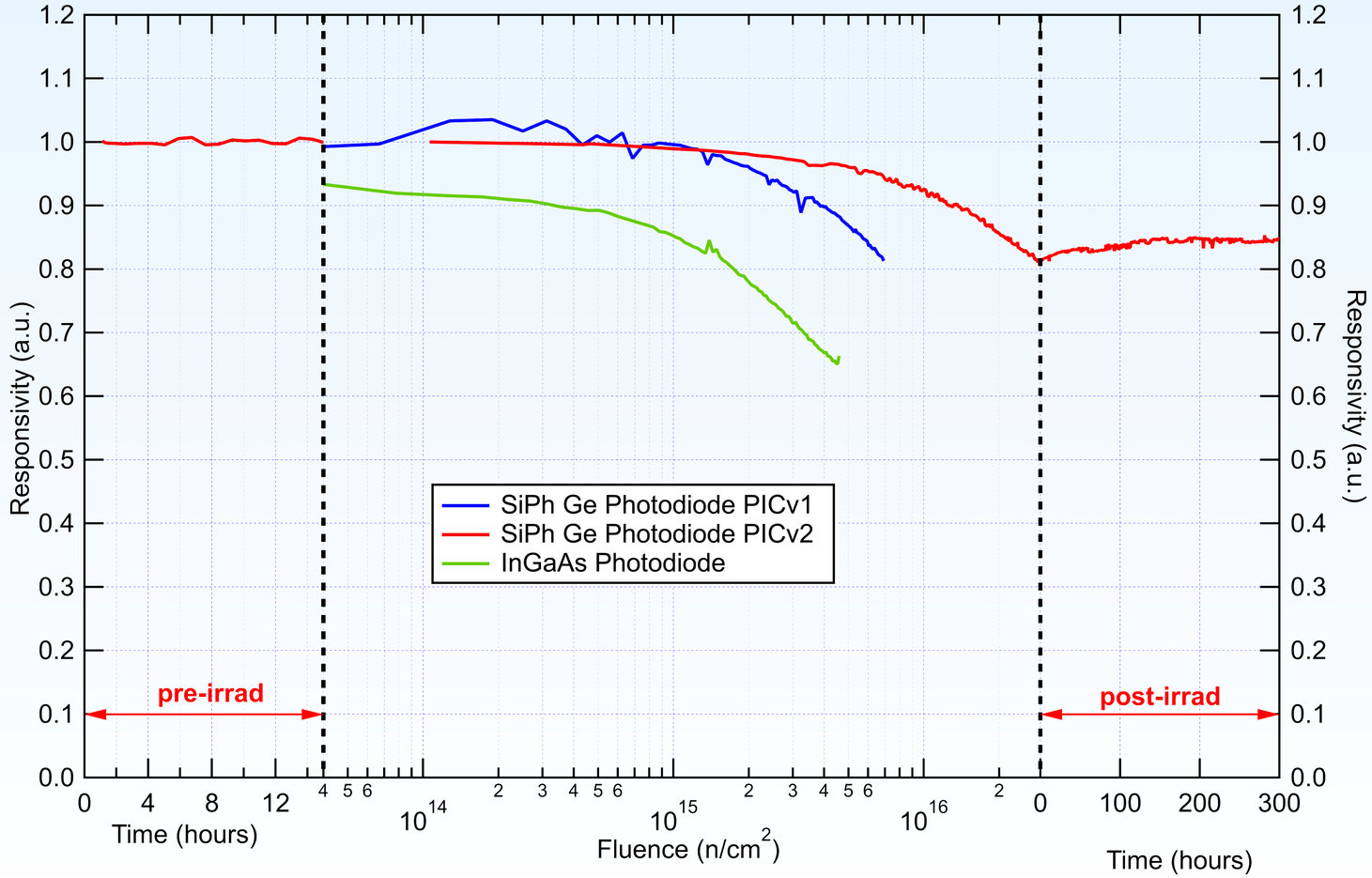


Total Fluence effect on integrated PDs

- Photodiodes are generally more sensitive to displacement damage effects, being bulk devices
  - Excellent performance
    - Better than existing discrete PDs (InGaAs)
    - Most recent process changes have been beneficial in terms of radiation tolerance

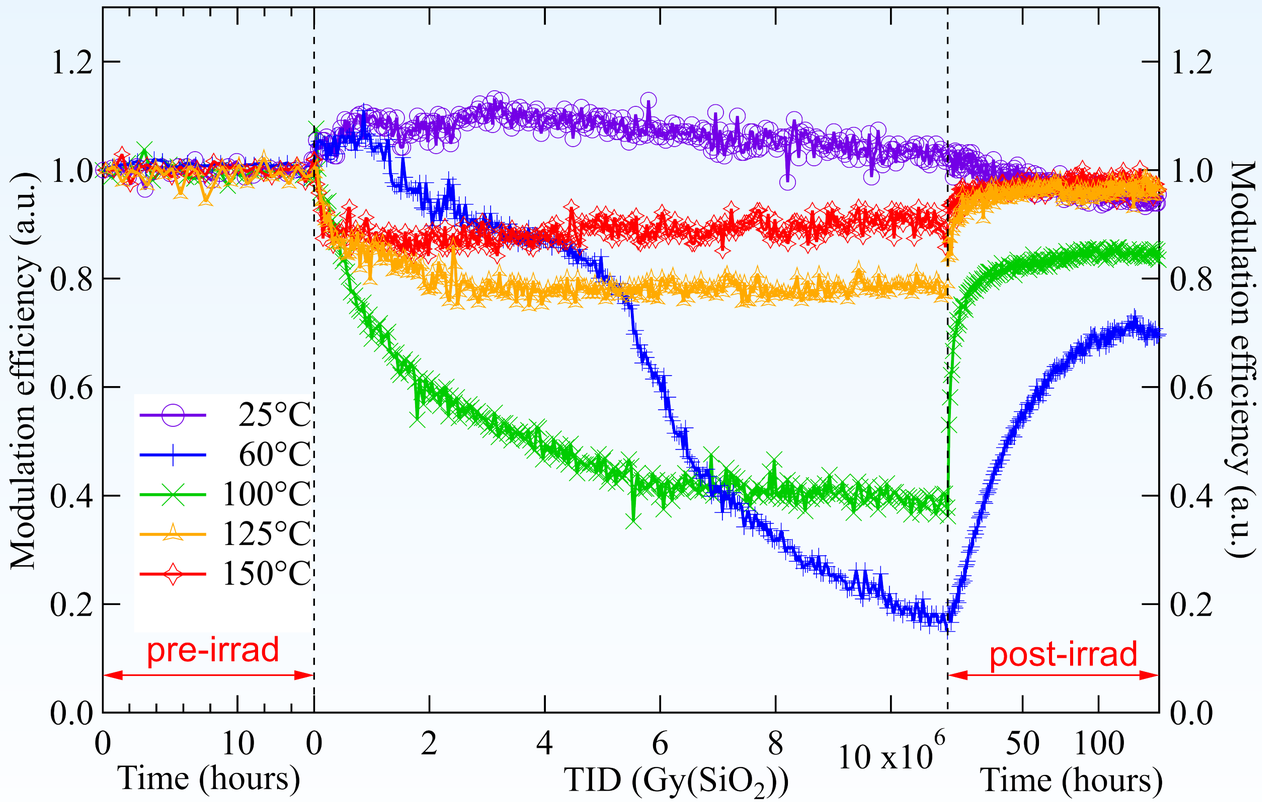
UCL Cyclotron neutron beamline with setup in place





Effect of Temperature on Dose Effects

- Ring Modulators most sensitive to Total Dose
- Micro-heaters built-in to PIC v2 allow localised temperature control during irradiation
  - First demonstration of this temperature effect in Silicon Photonics devices
    - reported at RADECS 2021
- Will be subject of further irradiation studies in order to understand the non-linear nature of the effect
  - Ultimately parameterise the effect and build into radiation damage model



Final Summary

- WP6 has produced much interesting R&D towards the implementation of future optical data transmission systems in line with the ECFA roadmap
  - Radiation tolerance
  - Higher line rate
  - COTS standards vs HEP
  - Async links
  - Low Mass, Low Power, Low Cost
- First link demonstrators have been operated
  - FPGA-based for line rate and FEC studies
  - Instrumentation-based for Silicon Photonics components
    - Including first thermal control of ring modulators, an important step to a robust system
- Work on providing building blocks for future application specific implementations is thus well advanced
  - Not a project goal to provide turn-key components for final applications

Outlook

- Key to actually deploying this type of technology with maximum impact will be in co-integration and/or co-packaging
  - This is the path to ultimate low-power and low-mass
    - Every chip-to-chip interconnect burns (unnecessary) power in the interconnect capacitance
  - This implies
    - ASIC building blocks to be integrated in specific FE ASICs
    - Tight co-packaging of photonics with electronics
- WP6 strongly suggests to re-instate the Packaging Task that was removed as part of the initial project re-baselining

- Starting already to field questions regarding what might be possible from future detector upgrade projects
  - e.g. LHCb, CMS