EP R&D WP5
Status & Plans

CERN EP R&D Days 2022

21 June 2022

Kostas Kloukinas
on behalf of the WP5 Team

WP5 Motivations

WP 5
EP R&D

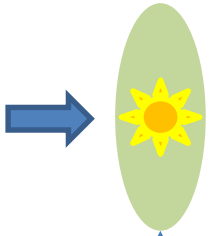
Identify IC technologies and Powering Solutions for on-detector ASICs and make them available in the HEP community

2020-2021

Technology Selection Criteria

- Radiation Tolerance
- Accessibility
- Long-term availability
- Availability of IP blocks
- Technical support
- Cost

2021-2022



Technology Selection
"TSMC 28nm CMOS"

Common Design Platform

Mixed-Signal Design Kit,
Reference Workflows, Rad-Tol techniques

Basic macro-blocks

Rad-Tol IO pads, ESD structures, SRAMs

Analog IP blocks (WP5.2a)

Rad-Tol Vbg., ADC, DAC, PLL, DLL,..

SOC Platform

System-On-Chip design Enablers

Powering solutions (WP5.2b)

DC/DC, LDOs

Collaborative Framework

3-way NDAs, Commercial contract,
framework for collaborative design work

Resources 2021-22

- WP5.1
  - Kostas Kloukinas *(Staff)*
  - Davide Ceresa *(Staff)*
  - *Giulio Borghello (Staff)*
  - Risto Pejasinovic *(Fellow)**
  - Francisco Piernas Diaz *(Tech. Student)**
  - Jashandeep Dhaliwal *(Trainee)**
  - Morten Andersen *(Danish Trainee)* >> July 2022*
  - Anvesh Nookala *(AT Doct. Student) >> Oct. 2022*
- WP5.2a
  - Rafael Ballabriga *(Staff)*
  - *Jan Kaplon (Staff)*
  - Franco Bandi *(Fellow)**
  - Markus Piller (*Doct. Student*)*
  - Khalil Khalife *(Trainee)**
  - Simone Emiliani *(Trainee)**
  - Tobias Hoffman *(Fellow)**
- WP5.2b
  - Stefano Michelis *(Staff)*
  - *Giacomo Ripamonti (Fellow)*
  - Pablo Antoszczuk *(Fellow)**
  - Mattia Balutto *(Tech. Student)**
- CERN ASIC Support
  - *Alessandro Caratelli (Staff)*
  - *Marco Andorno (Fellow)**

** funded by WP5*

Workplan

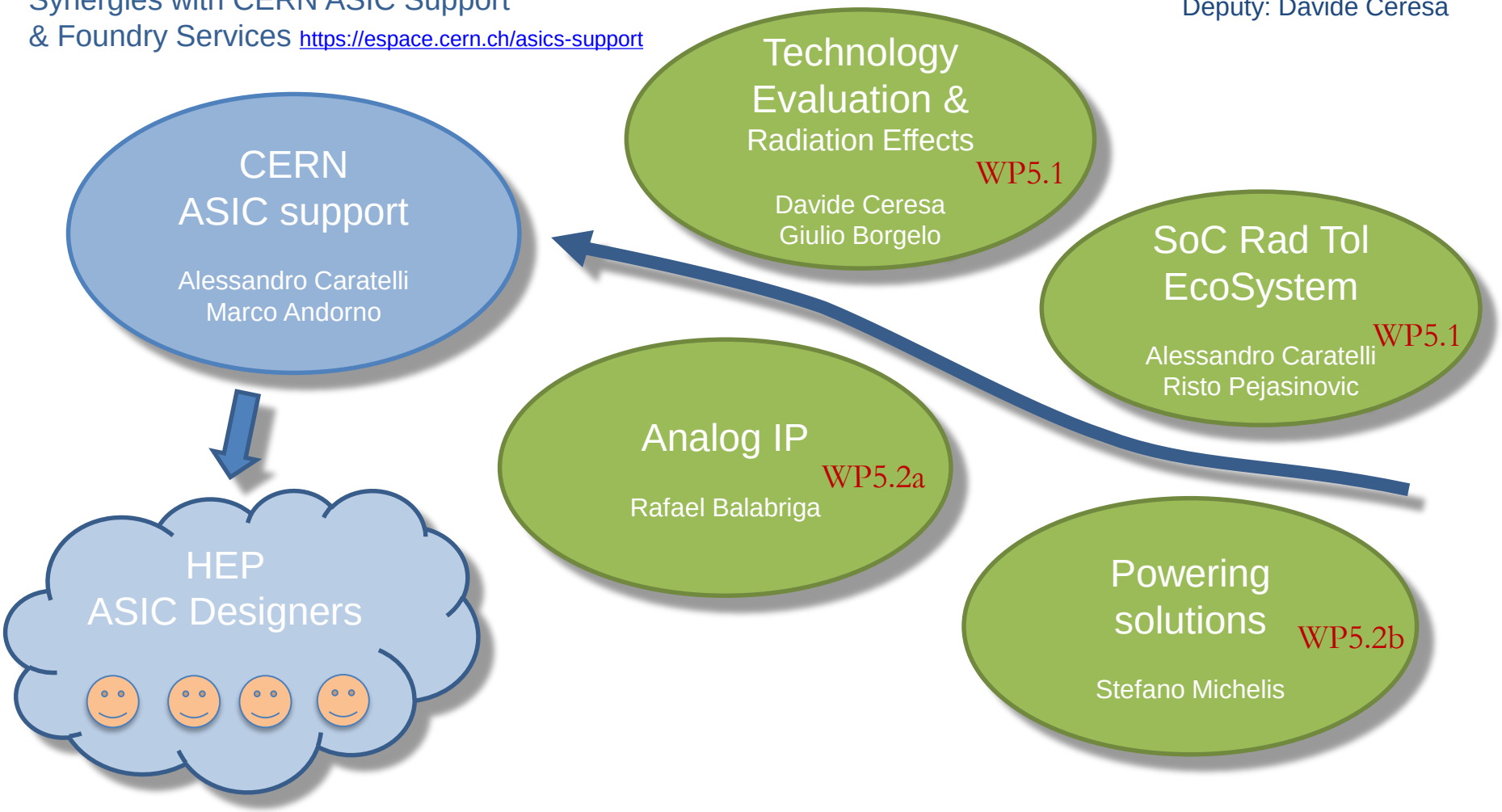
- Radiation hardness evaluation of 28nm chips prototyped in 2021
  presentation by Davide Ceresa
- Explore possibilities to access and evaluate nanoscale IC technologies
- Development of IP blocks (CERN and collaborating institutes)
  presentation by Franco N. Bandi
- R&D on Rad-Tol SoC topologies and design methodologies
- Powering solutions activities: originally planned developments and R&D for a 28nm on-chip DC/DC converter
  presentation by Stefano Michelis
- Disseminate results to the HEP community

WP5 Activities

WP 5
EP R&D

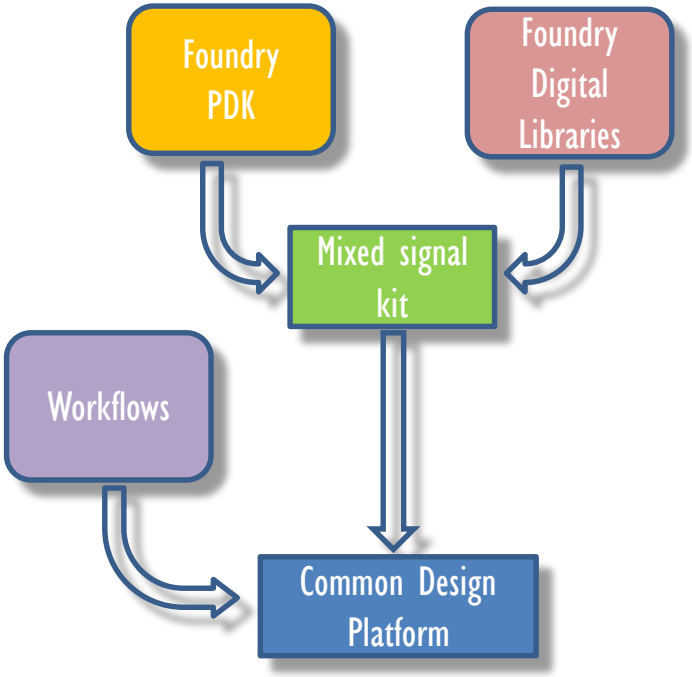
Leader: Kostas Kloukinas
Deputy: Davide Ceresa

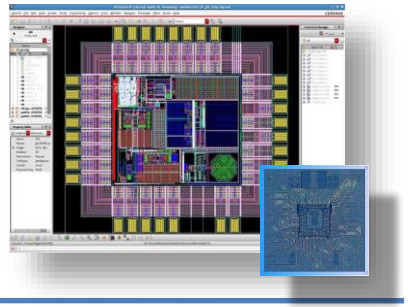
Synergies with CERN ASIC Support
& Foundry Services https://espace.cern.ch/asics-support



Common Design Platform

- 28nm Common Design Platform:
  - Support collaborative work of distributed design teams
  - Minimize efforts to integrate a “design environment”
  - Avoid incompatibilities
- Incorporates:
  - **Mixed-Signal Design kit**
  - **Scripted Design Flows** that are standardized and validated using selected EDA software tools
  - **Maintenance**
  - **Technical Support**
  - **Training**
    - 28nm 5-days course under development
- Developed by
  - **CERN ASIC Support Team** in collaboration with Cadence VCAD Design Services
    - https://asicsupport.web.cern.ch



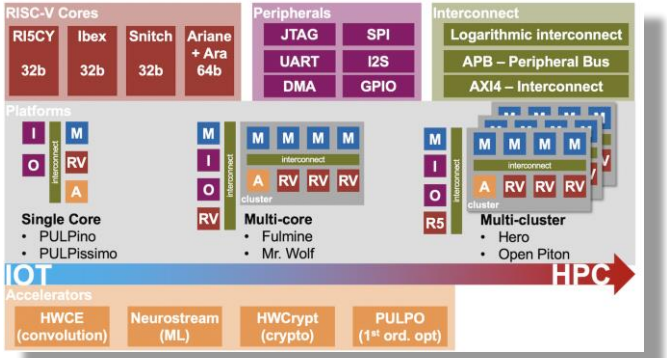


SoC design Platform

- Motivation
  - Introduce a more abstract design methodology to tame design complexity
  - Enable on-detector data processing
  - Reconfigurable & flexible on-detector electronics

- Proposed solution
  - Complement the Common Design Platform with SoC Design Platform
  - Define standardized interconnects for IP blocks
    - Develop IP blocks that adhere to a standard
    - Facilitate Hierarchical digital Implementation and Verification
    - IP blocks accompanied by Verification IP code
  - Programmable, flexible logic (core processor, eFPGA)
  - Employ Radiation Tolerant design techniques

SoC partners



- ETH-Zurich
  - Parallel Ultra Low Power (PULP) Platform
  - Open-source RISC-V architecture
  - PULP team ….https://pulp-platform.org/team.html
  - Regular meetings and technical support

- KU Leuven University (Belgium)
  - High-Performance fault-tolerant RISC-V microprocessors for harsh environments
  - Fault tolerance systolic array Deep Neural Network (DNN) accelerator
  - Established bi-weekly meetings

KU LEUVEN

Team leader: Prof. Jeffrey Prinzie (jeffrey.prinzie@kuleuven.be)
Principal researchers: Karel Appels, Mohamed Mounir, and Naïn Jonckers

Collaborative Framework

- Commercial frame contract
  - CERN has a frame contract that allows small-scale prototyping (MPWs)
  - It will be extended to cover full-maskset engineering and production works
  - The frame contract is accessible by HEP Institutes and Universities, via CERN

- NDAs
  - Special 3-way NDA that permit collaborative work
    - Permit the exchange of designs and technical data among collaborators
    - CERN has signed the 3-way NDA *(CERN-Europractice/IMEC-TSMC)*
    - Signatory process for Institutes and Universities has started

The "28nm Forum"

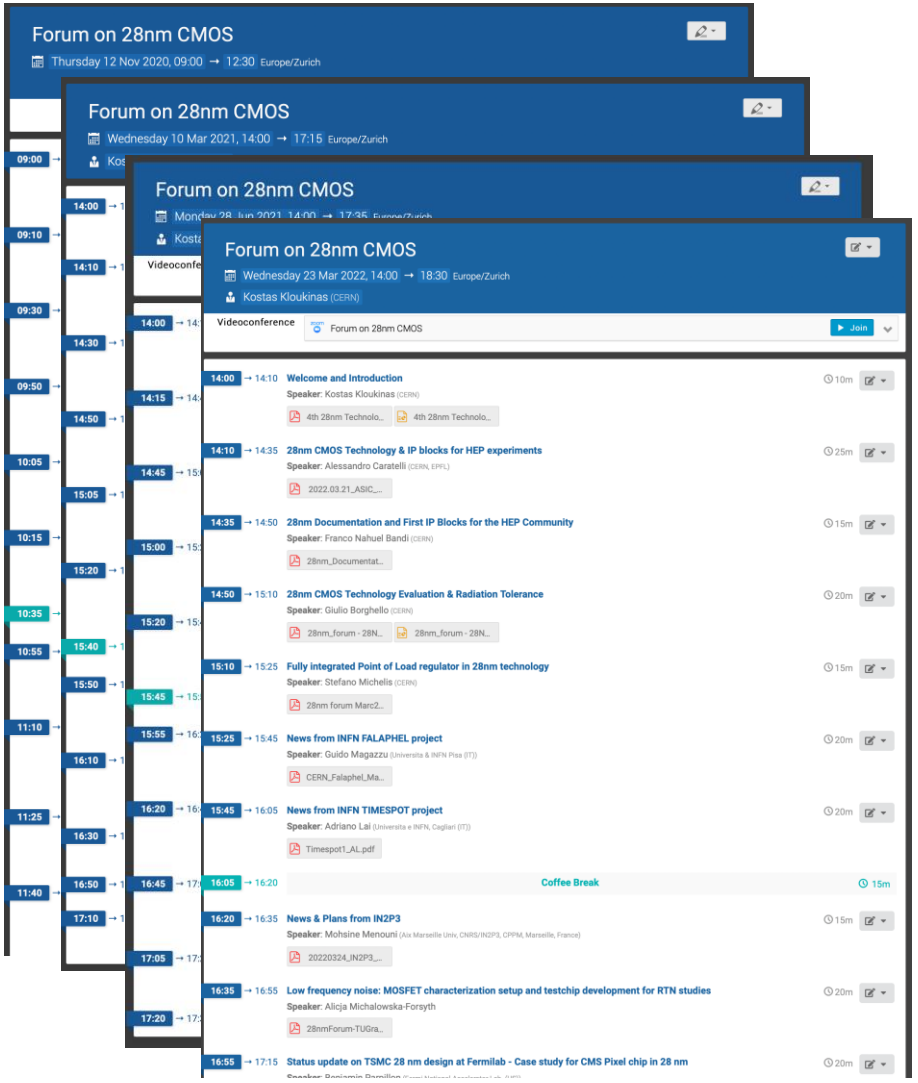
- Purpose of the 28nm Forum
  - CERN to communicate the EP R&D WP5 activities
  - Institutes to present their R&D activities and plans
  - Identify synergies
  - Establish collaborations

28nm Technology Forum Sessions

1st session (Nov. 12, 2020) https://indico.cern.ch/event/970389/
2nd session (Mar. 10, 2021) https://indico.cern.ch/event/1009040/
3rd session (July 28, 2021) https://indico.cern.ch/event/1042567/
4th session (Mar 23, 2022) https://indico.cern.ch/event/1132318/
5th session proposed for **Q3 2022**

established periodicity: 3 times per Year

- Restricted access; requires registration
- Self-inscribed CERN e-group: **28nm-Forum@cern.ch**



Coherence with ECFA roadmap

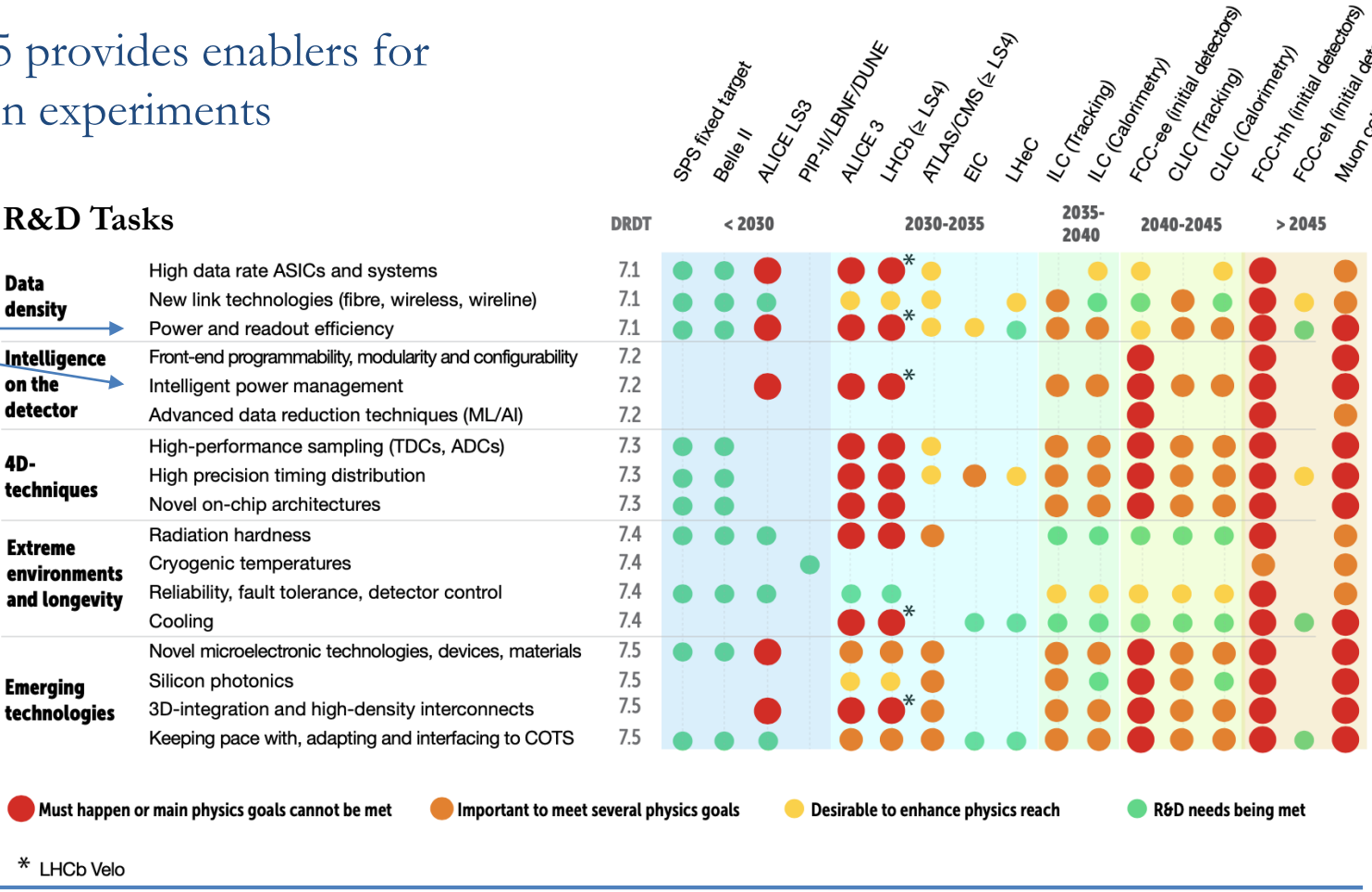
WP 5 EP R&D

2021 ECFA DETECTOR RESEARCH AND DEVELOPMENT ROADMAP
Chapter 7 Electronics and Data Processing

EP R&D WP5 provides enablers for next generation experiments

WP5.2

WP5.1

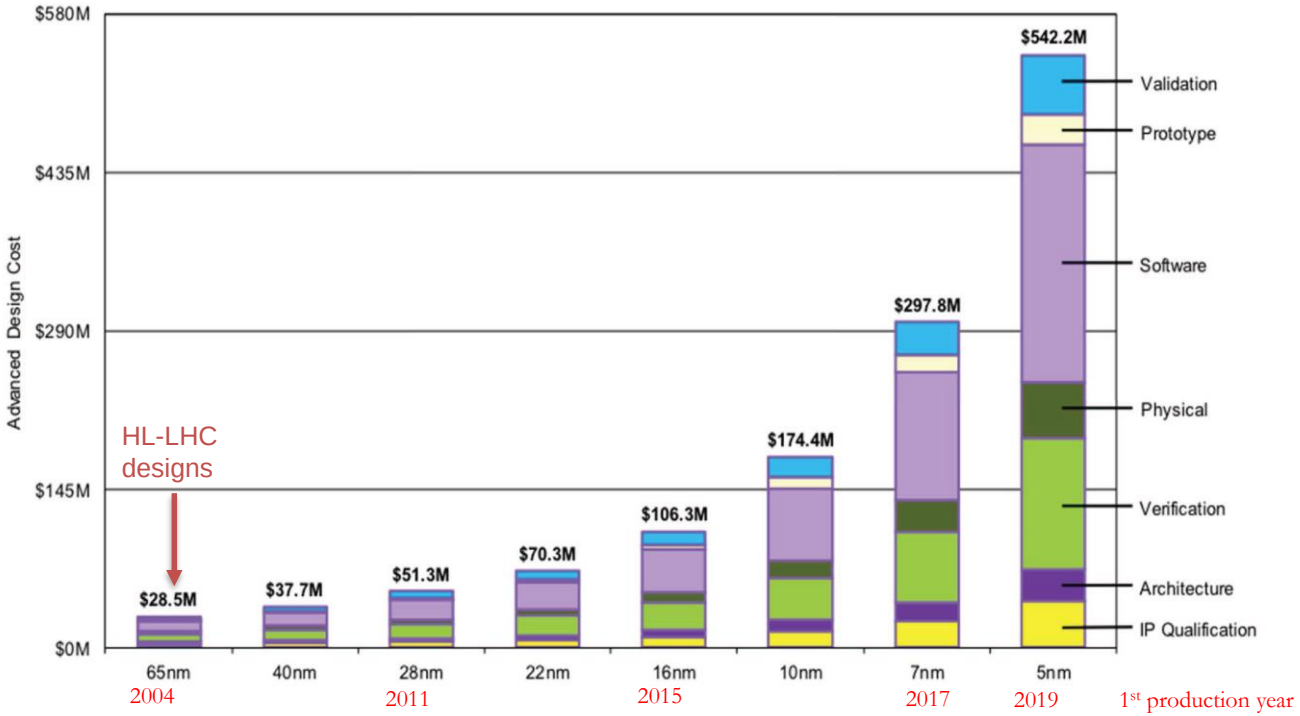


Coherence with ECFA roadmap

- Technology Choice
  - The selection and adoption of the 28nm CMOS technology as a “mainstream” process will ”fuel” the developments of *”near-future”* experiments
  - *“Further-future”* collider experiments would require more advanced technologies offering the necessary combination of performance, power efficiency and radiation hardness
    - R&D on future state-of-the-art IC technologies would be necessary
- ASICs evolution and front-end “intelligence”
  - Data reduction/processing adaptable to changing experimental conditions
  - Programmability and configurability to facilitate retargeting ASICs to different applications
  - Present R&D on core-based SoC design topologies and methodologies will be applicable in “near-future” experiments as well as pave the way for the electronics of “further-future” colliders
- Power distribution
  - Stagged voltage conversion, multiple supply voltages, intelligent power management
- Infrastructure needs and Organizational issues
  - Common Design Platforms
    - A common support service provides maintenance, support, training
  - Collaborative Framework


Thank You

ASIC development costs



Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS*

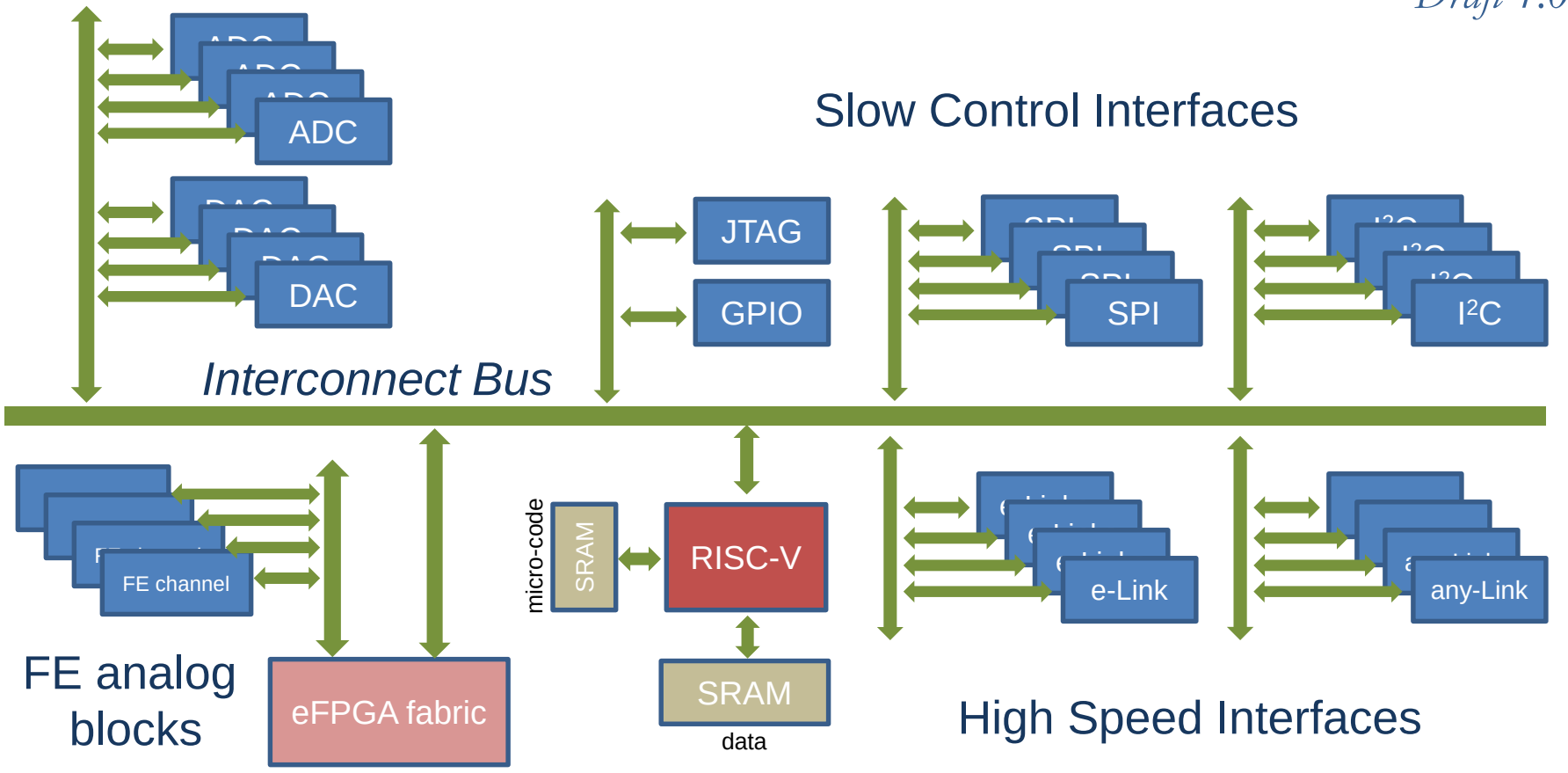
- Escalating design development costs
- Techno-economic constraints associated with the use of Ultra Deep Submicron technologies

SoC Radiation Tolerant Ecosystem

WP 5 R&D

Conceptual Scheme

Draft 1.0



WP5 Activities

WP 5
EP R&D

Leader: Kostas Kloukinas
Deputy: Davide Ceresa

- Activity 5.1: CMOS Technologies
  - Technology evaluation
  - Radiation Effect studies
  - Common Design Platform
  - Collaborative Framework
- Activity 5.2: Design & IPs
  - 5.2a: Analog IP blocks
    - Hard IP block development
  - 5.2b: Powering Solutions
    - High Efficiency DC/DC converters and power management