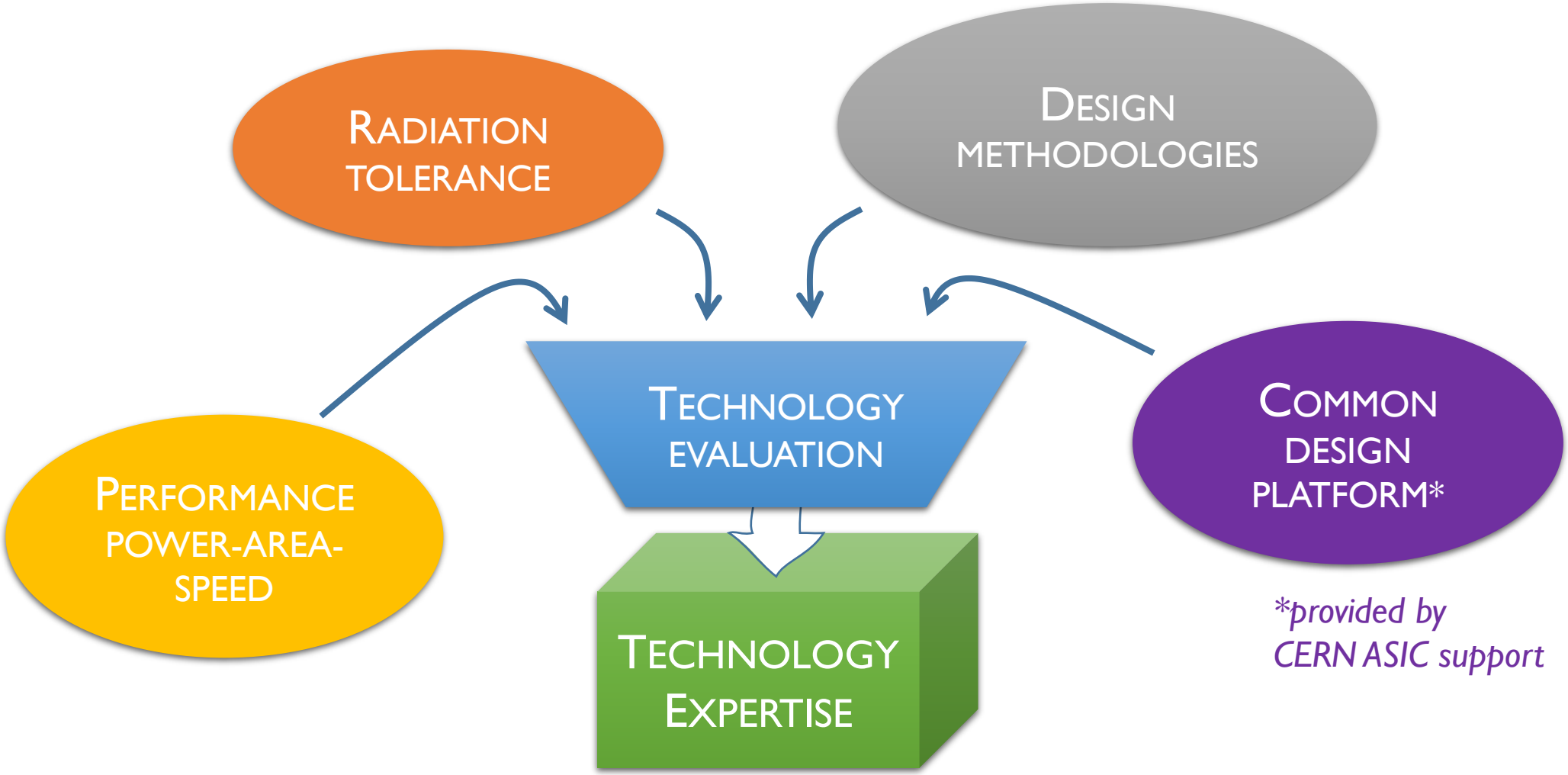
EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

WP 5
TECHNOLOGY EVALUATION

D. CERESA on behalf of EP R&D Work Package 5

WP5 Technology Evaluation: What is it?



WP5 Technology Evaluation: the Team(s)

CHIP DESIGN AND TESTING

GIULIO BORGHELLO (STAFF)

DAVIDE CERESA (STAFF)

FRANCISCO PIERNAS DIAZ (TECH)

RISTO PEJASINOVIC (FELL)

GIANMARIO BERGAMIN (EXT. EP-ESE-ME)

ADITHYA PULLI (EXT. EP-ESE-ME)

JOINED EFFORT WITH WP5.2a TEAMS

NEW DESIGN SOLUTIONS

ALESSANDRO CARATELLI (STAFF)

DAVIDE CERESA (STAFF)

KOSTAS KLOUKINAS (STAFF)

MARCO ADORNO (FELL)

JASHANDEEP DHALIWAL (TRAINEE)

RISTO PEJASINOVIC (FELL)

WP5 Technology Evaluation: timeline

2020

Technology choice

- Technologies evaluated at transistor level on provided samples
- Main focus on performance and radiation tolerance
- 28 nm CMOS technology selected as main node for upcoming development

2021

Test chip design

- Transistor level chip designed in the selected technology
- 3x digital-on-top chips designed for technology building blocks evaluation
- Design methodologies and common design platform developed

2022

Testing & evaluation

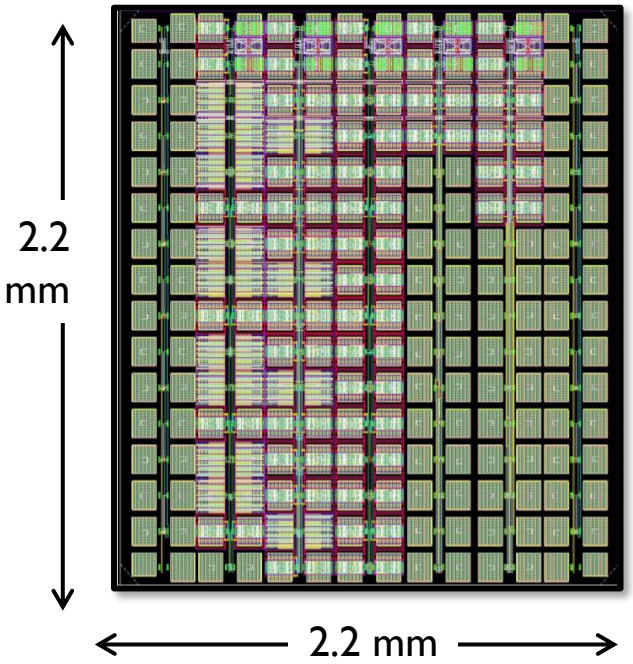
- Functional testing of test chips
- Radiation testing (TID and SEE) of test chip
- Prepare technology guidelines for 28 nm radiation tolerant design

Total Ionizing Dose – TID - chip

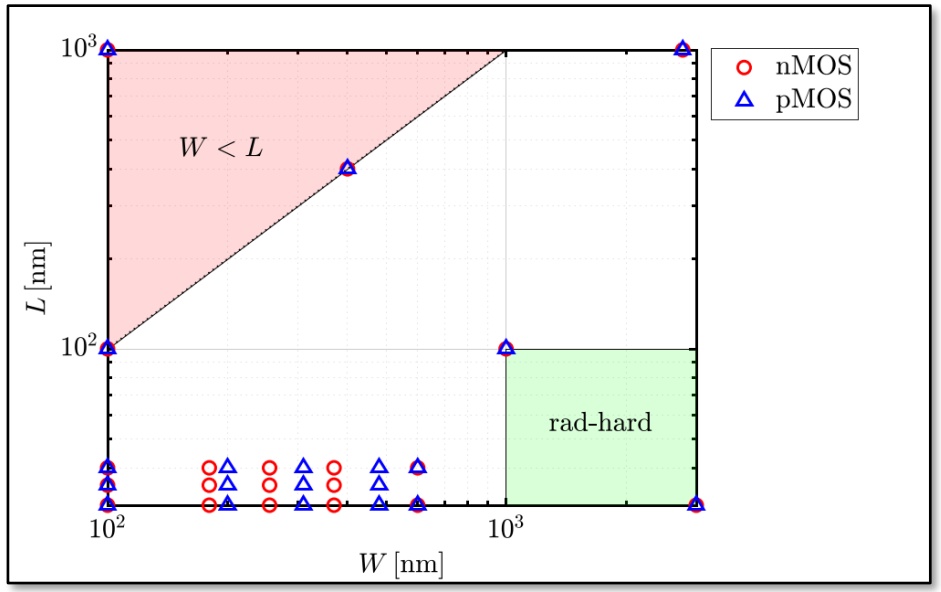
A chip to study radiation effect on single transistors in the HPC+ technology flavour

- 7x probing arrays compatible for the EP-ESE-ME X-ray machine setup
- Different transistor flavors and variability arrays
- Design submitted on a MINI@SIC run in June 2021

TID chip layout



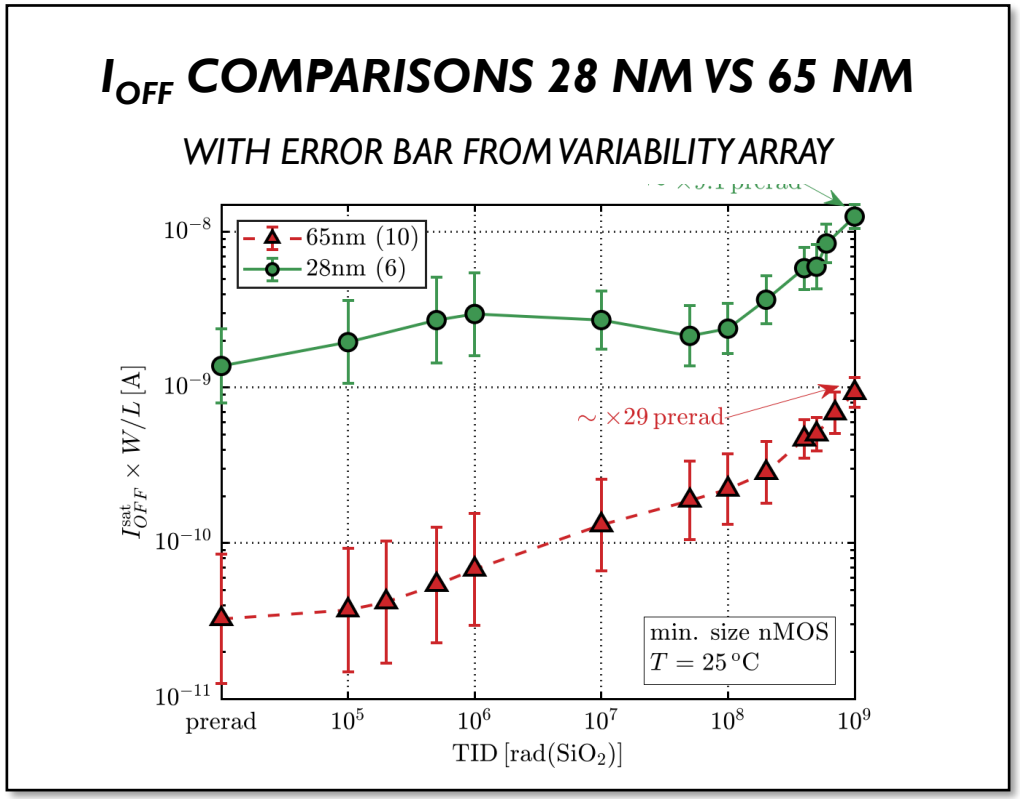
Transistor sizing array

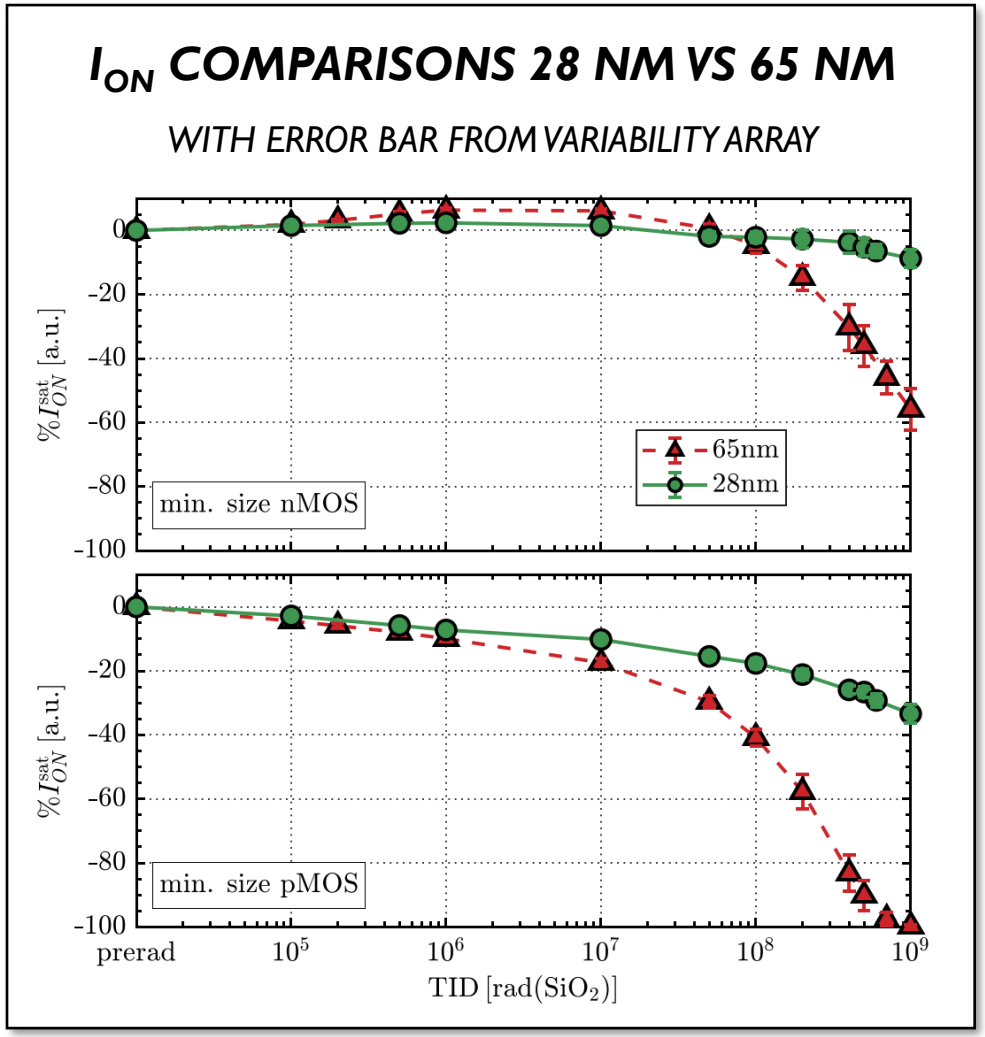


TID CHIP RESULTS

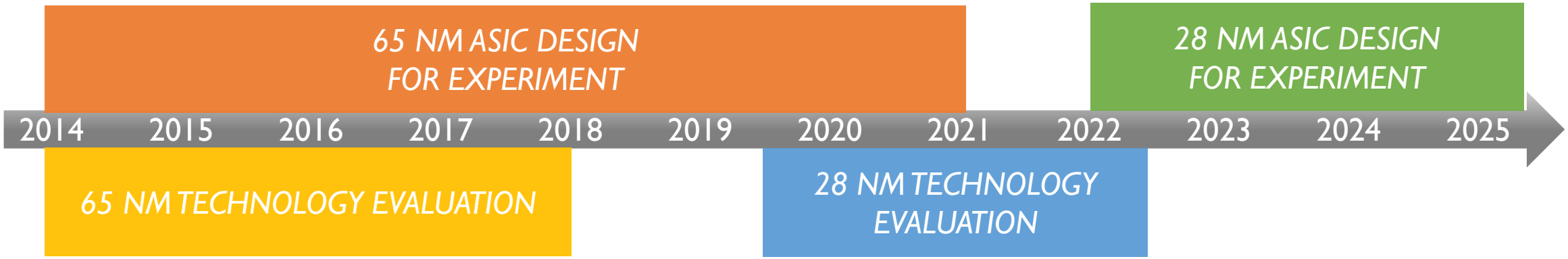
28 NM TECH. OUTPERFORM 65 NM AT HIGH TID (1 GRAD):

- < -40% CONDUCTIVE CURRENT LOSS
- ONLY x10 LEAKAGE CURRENT RESPECT 65 NM





WP5 Technology Evaluation: Design & IP block level



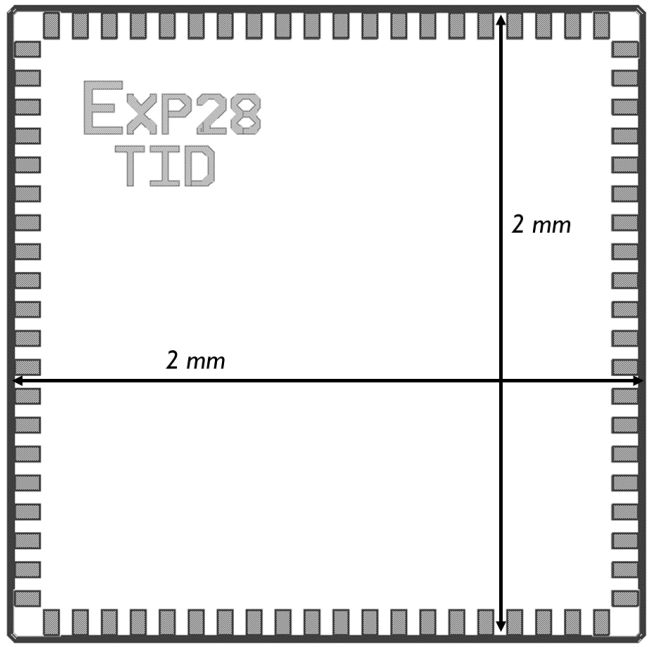
Charachterize the 28 NM technology, experience the design flow and build an IP block library before the design of large and complex ASICs begins

Exp28 chips suite

EXP28 CHIP SUITE: 3X DIGITAL-ON-TOP DESIGN

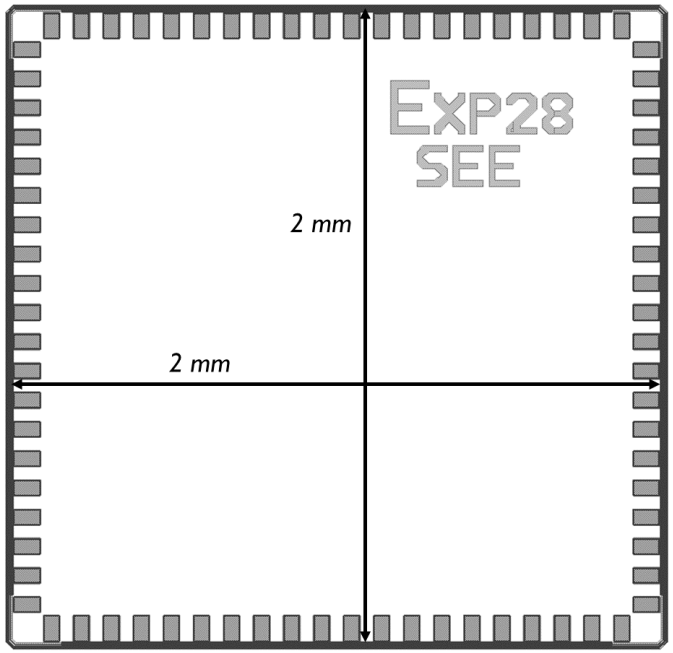
TOTAL IONIZING DOSE (TID) STUDIES:

- Ring Oscillator for standard cells
- Built-In-Self-Test for SRAM memories



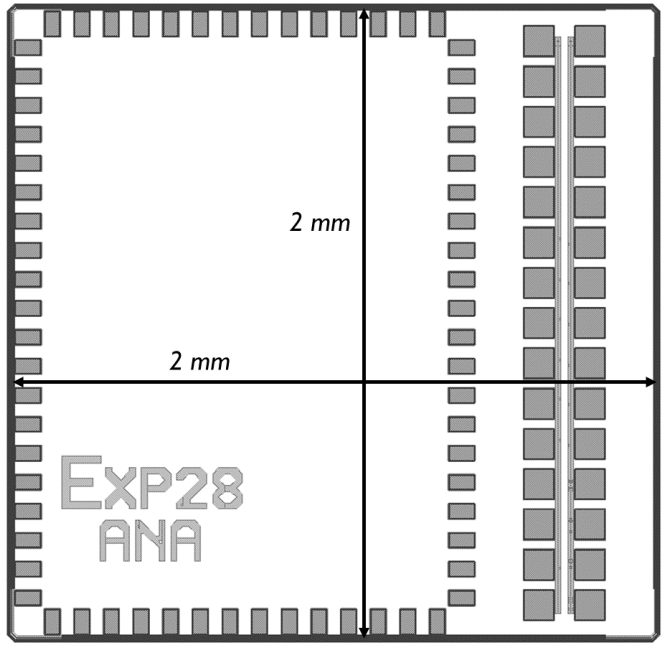
SINGLE EVENT EFFECT (SEE) STUDIES:

- Vernier Delay line for Single Event Transient (SET)
- Flip-Flop matrixes for Single Event Upset (SEU)
- Functional SRAM test for SEE on memories

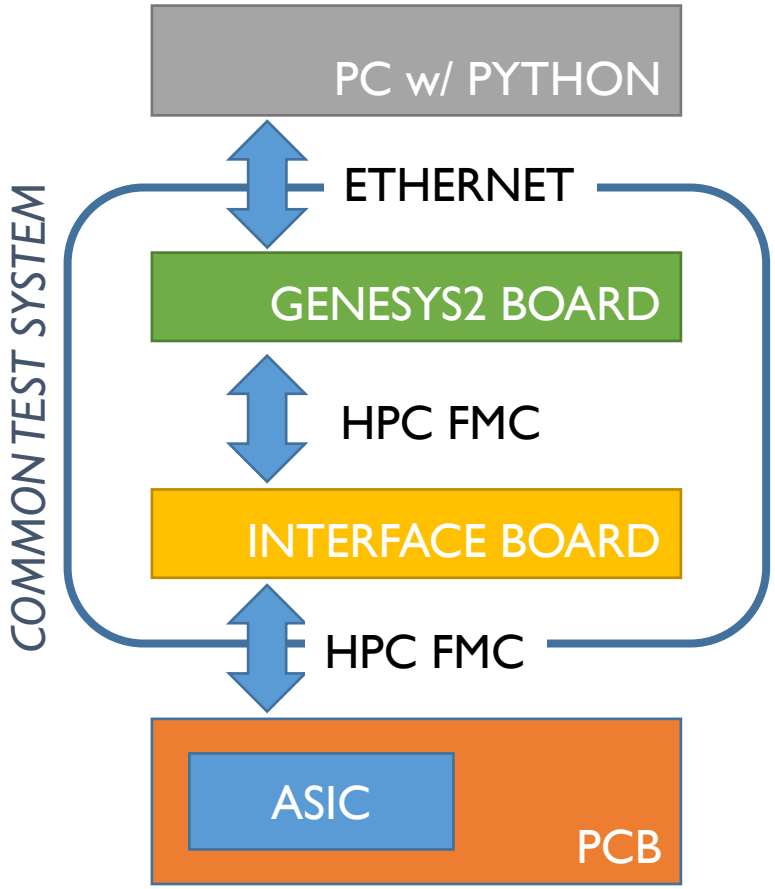


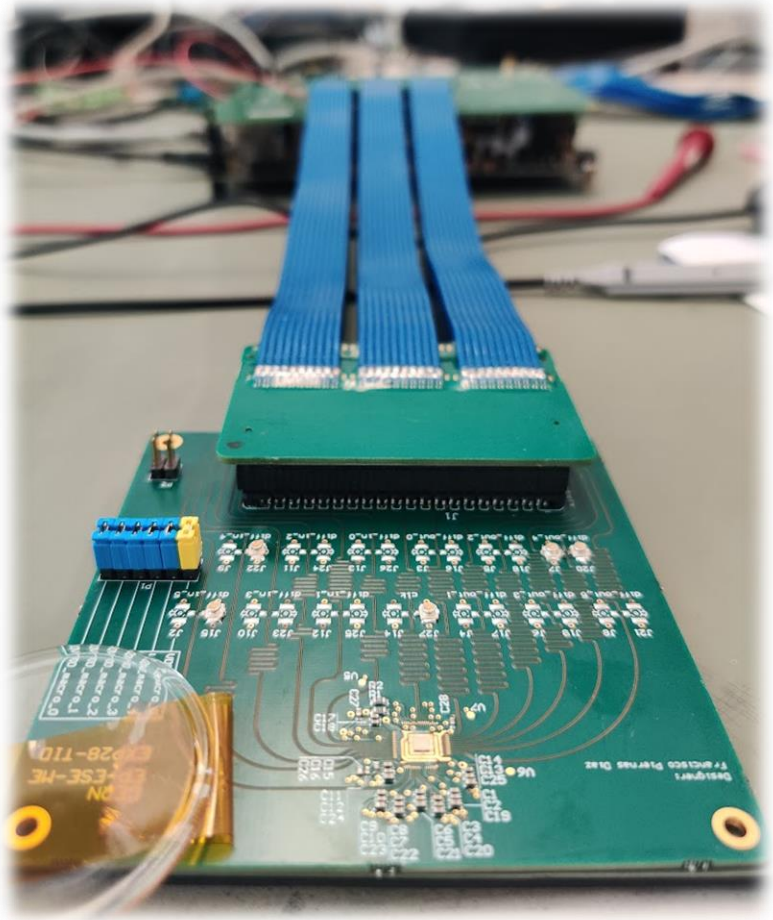
IP BLOCKS CHARACHTERIZATION

- Bandgap and Temperature sensor
- Digital-to- Analog Converted (DAC)
- Probe array for HV devices and resistors



EXP28: A COMMON TEST SYSTEM



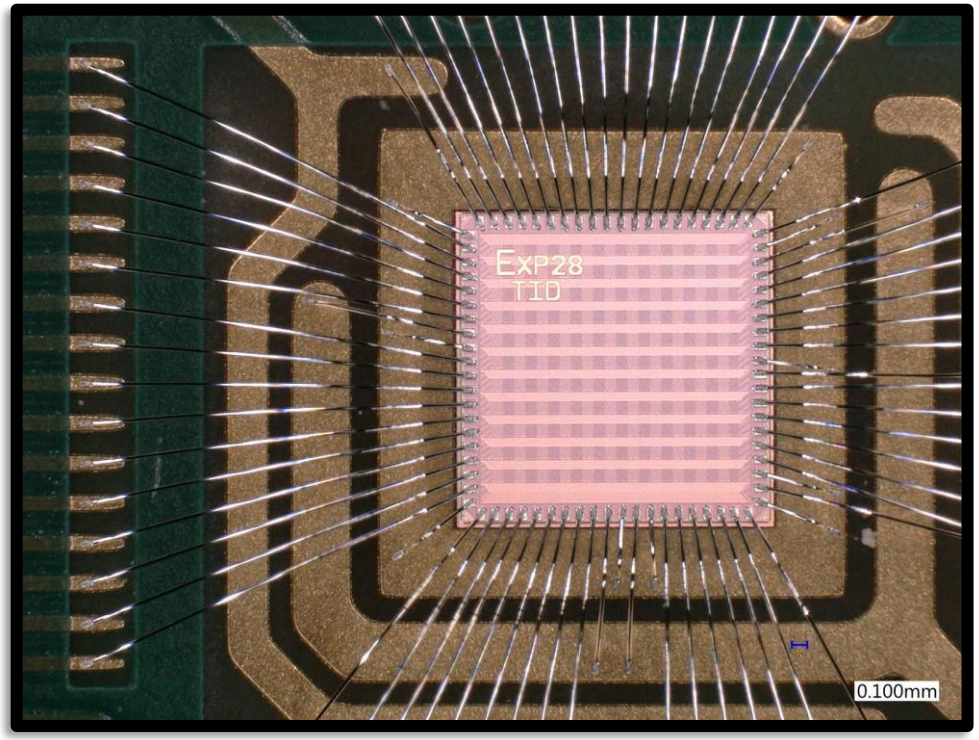


Credits:

Interface board design by R. Pejasinovic
Firmware development by R. Pejasinovic
Carrier board design by F. Piernas Diaz
Wire-bonding by CERN bonding lab

EXP28 TEST CHIP FAMILY:

SUBMITTED ON 5TH OF JANUARY 2022
RECEIVED IN MAY 2022



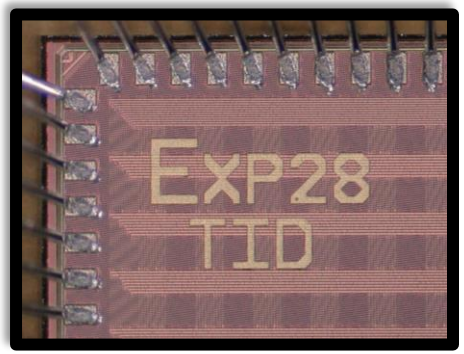
Credits:
Wire-bonding by CERN bonding lab

POWER-UP AND CONFIGURATION TESTS PASSED ON ALL CHIPS

PLAN FOR TESTING :

- FUNCTIONAL TESTING – MAY - JULY '22
- TID TESTING – JULY - SEPTEMBER `22
- SEE TESTING – SEPTEMBER - DECEMBER `22
  - RADNEXT APPLICATION ACCEPTED FOR HEAVY ION TESTING
  - FURTHER TEST UNDER DISCUSSION WITH R2E PROJECT

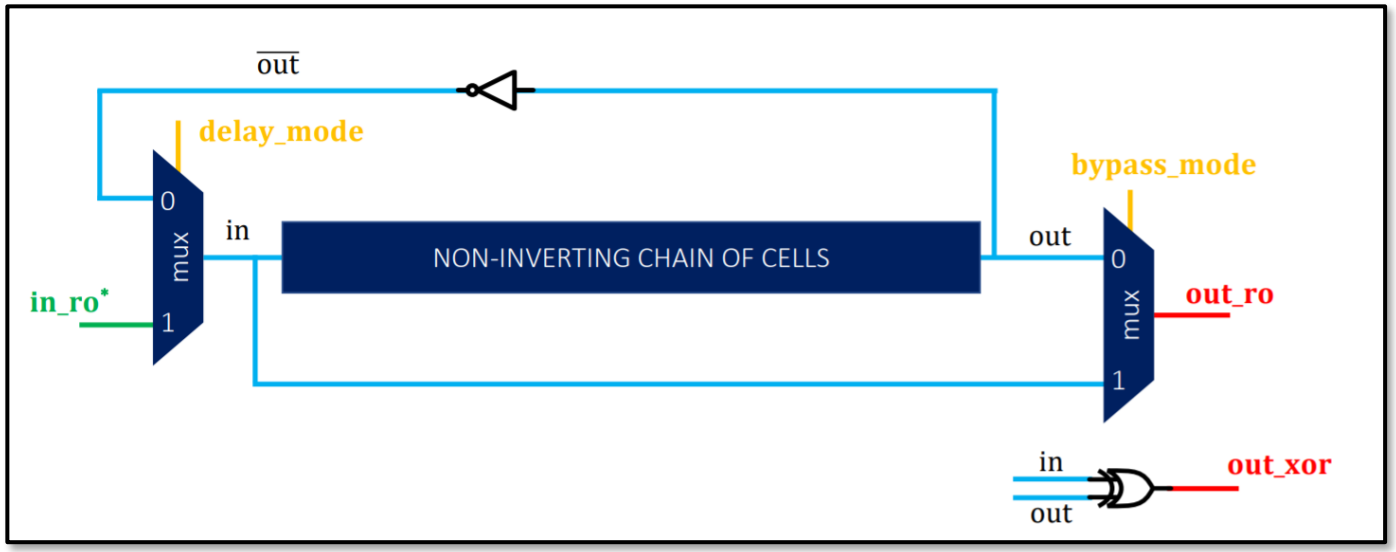
RING OSCILLATOR: TEST STRUCTURE



TOTAL IONIZING DOSE STUDY ON STANDARD CELL LIBRARIES:

I_{ON} VS TID MEASURED AS VARIATION OF FREQUENCY IN A RING-OSCILLATOR.

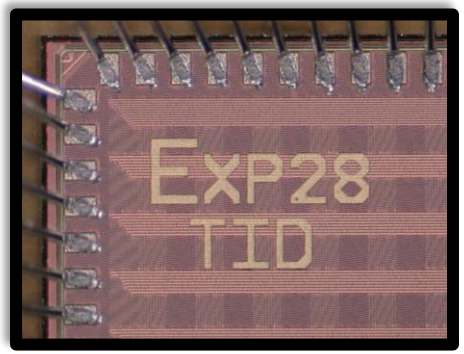
UN-BALANCING BETWEEN RISE AND FALLING TIME MEASURED WITH A DELAY CHAIN



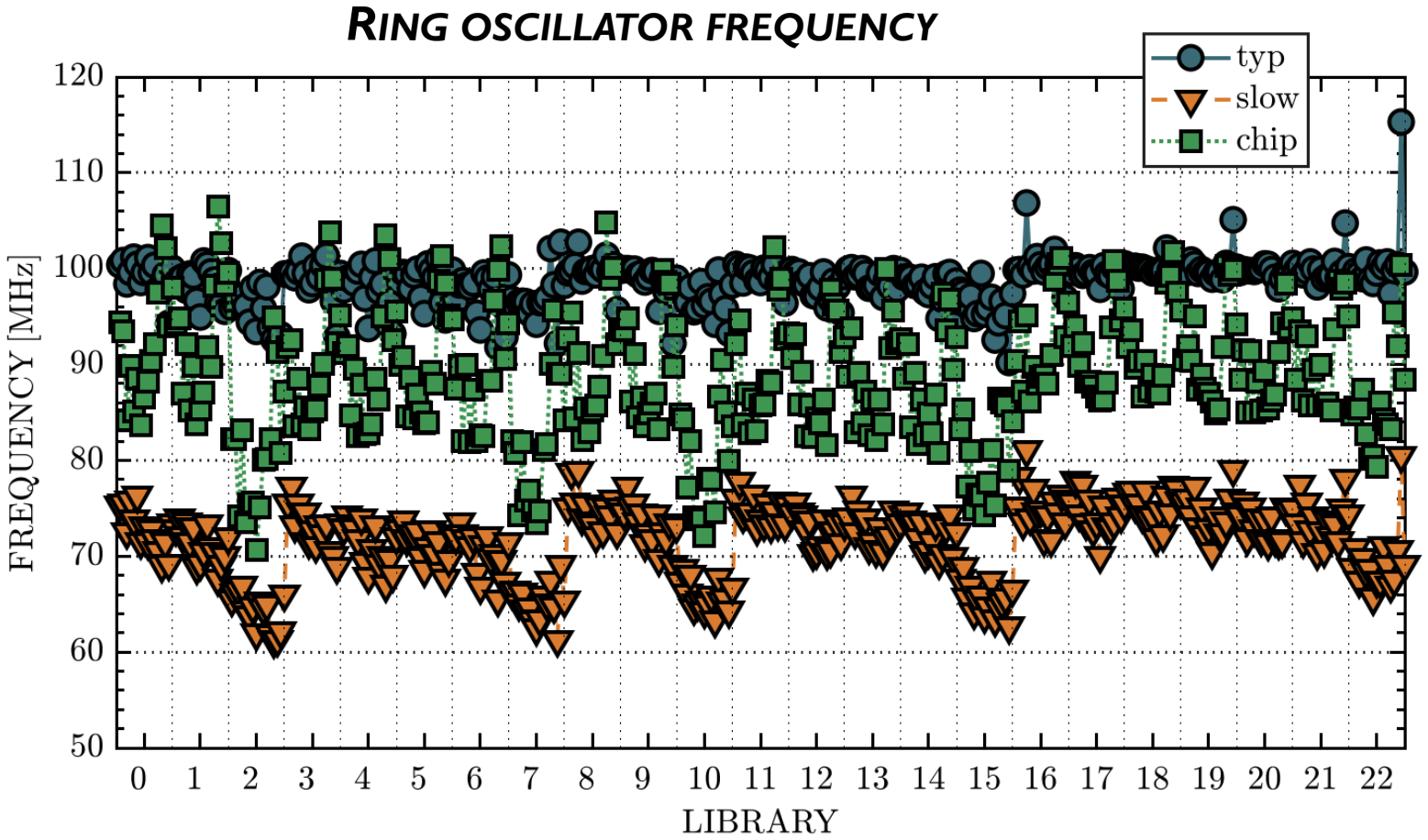
TESTING FEATURES:

- *INTERNAL COUNTERS ACCESSIBLE VIA I2C*
- *POWER GATING FOR SINGLE CELL CURRENT MEAS.*
- *EXTERNAL PSEUDO DIFFERENTIAL MEASUREMENT*

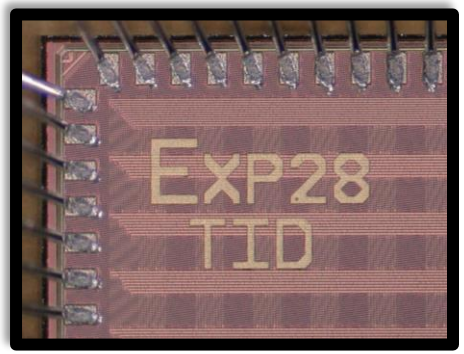
RING OSCILLATOR: PRE-RAD RESULTS



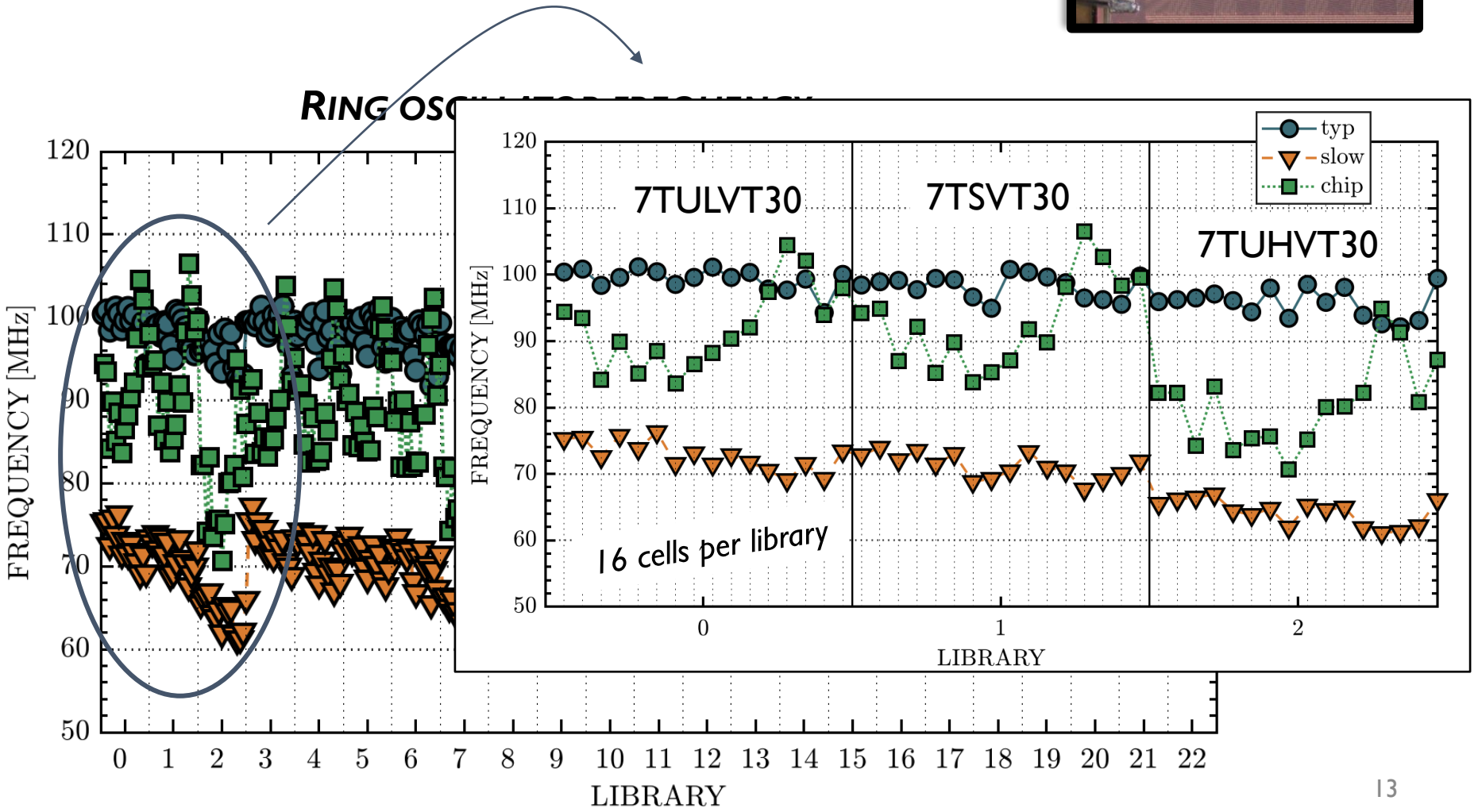
0	7TULVT30
1	7TSVT30
2	7TUHVT30
3	7TULVT35
4	7TSVT35
5	7TLVT40
6	7TSVT40
7	7TUHVT40
8	9TULVT30
9	9TSVT30
10	9TUHVT30
11	9TULVT35
12	9TSVT35
13	9TLVT40
14	9TSVT40
15	9TUHVT40
16	12TULVT30
17	12TSVT30
18	12TULVT35
19	12TSVT35
20	12TLVT40
21	12TSVT40
22	12TUHVT40



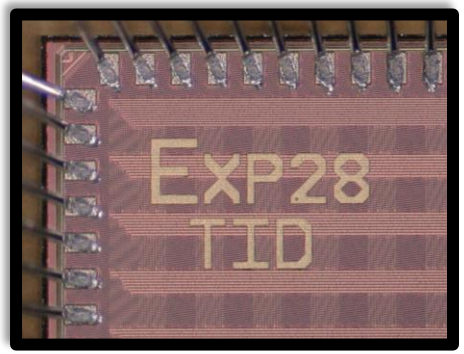
RING OSCILLATOR: PRE-RAD RESULTS



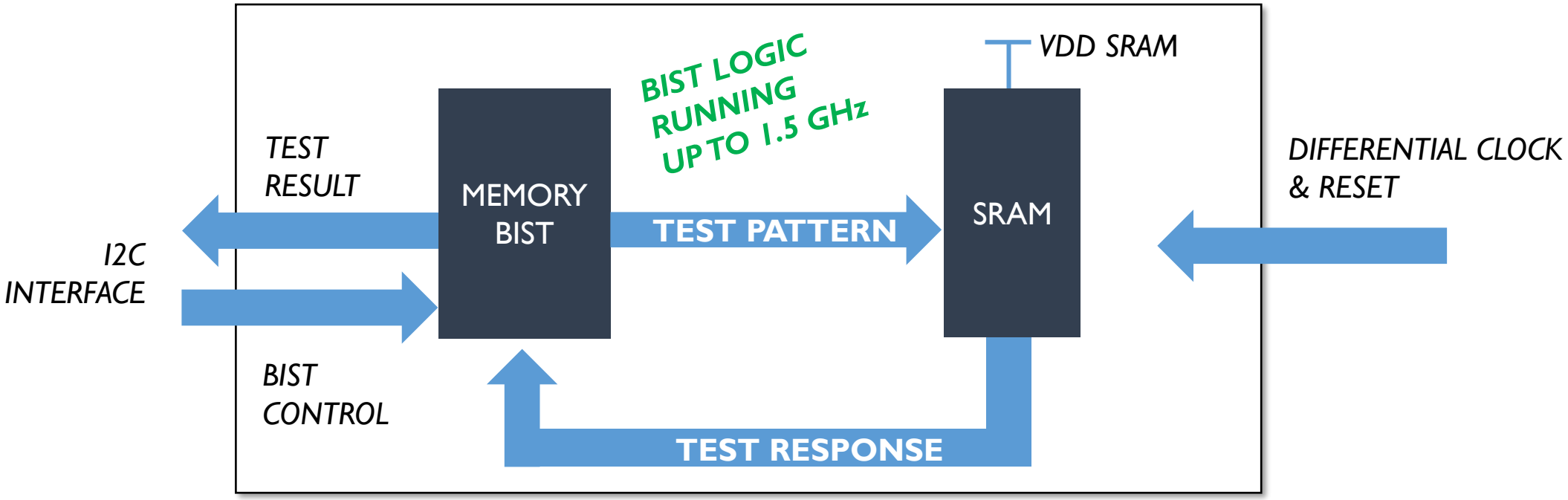
0	7TULVT30
1	7TSVT30
2	7TUHVT30
3	7TULVT35
4	7TSVT35
5	7TLVT40
6	7TSVT40
7	7TUHVT40
8	9TULVT30
9	9TSVT30
10	9TUHVT30
11	9TULVT35
12	9TSVT35
13	9TLVT40
14	9TSVT40
15	9TUHVT40
16	12TULVT30
17	12TSVT30
18	12TULVT35
19	12TSVT35
20	12TLVT40
21	12TSVT40
22	12TUHVT40



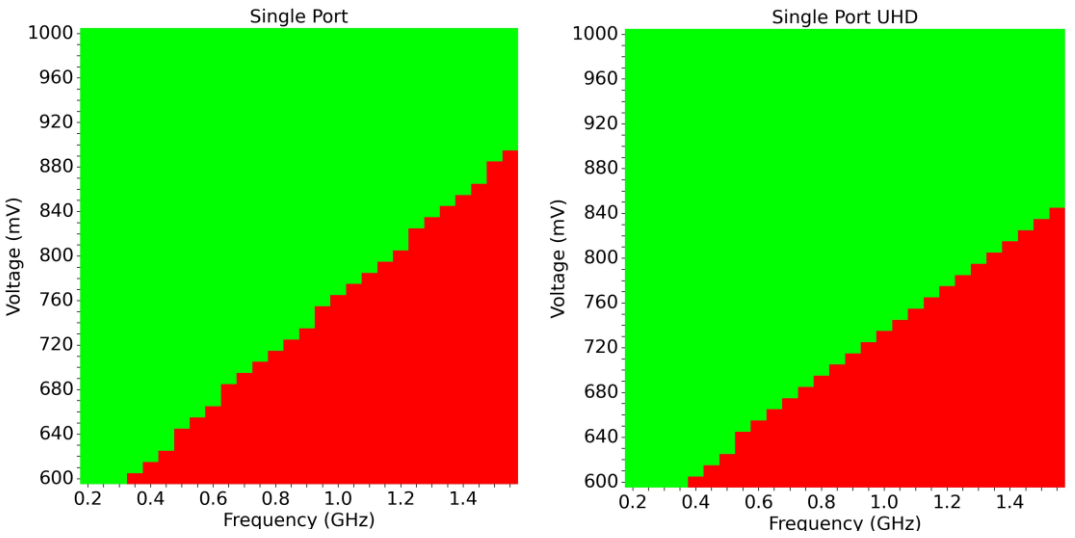
SRAM BUILT-IN-SELF-TEST: TEST STRUCTURE



- BIST REQUIRED TO COPE WITH HIGH SPEED MEMORY (ACCESS TIME ~ FEW NS)
- FOUNDRY MEMORY INCLUDES SUB-MINIMUM TRANSISTOR SIZE
- DIFFERENT TYPE OF MEMORY TESTED (SINGLE/DUAL PORT, STANDARD/ULTRA-HIGH DENSITY)



PRE-RAD RESULTS



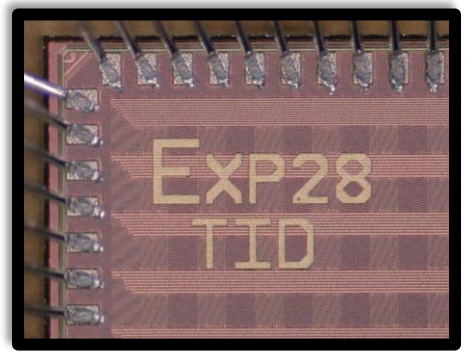
VOLTAGE-FREQUENCY SCHMOO PLOT

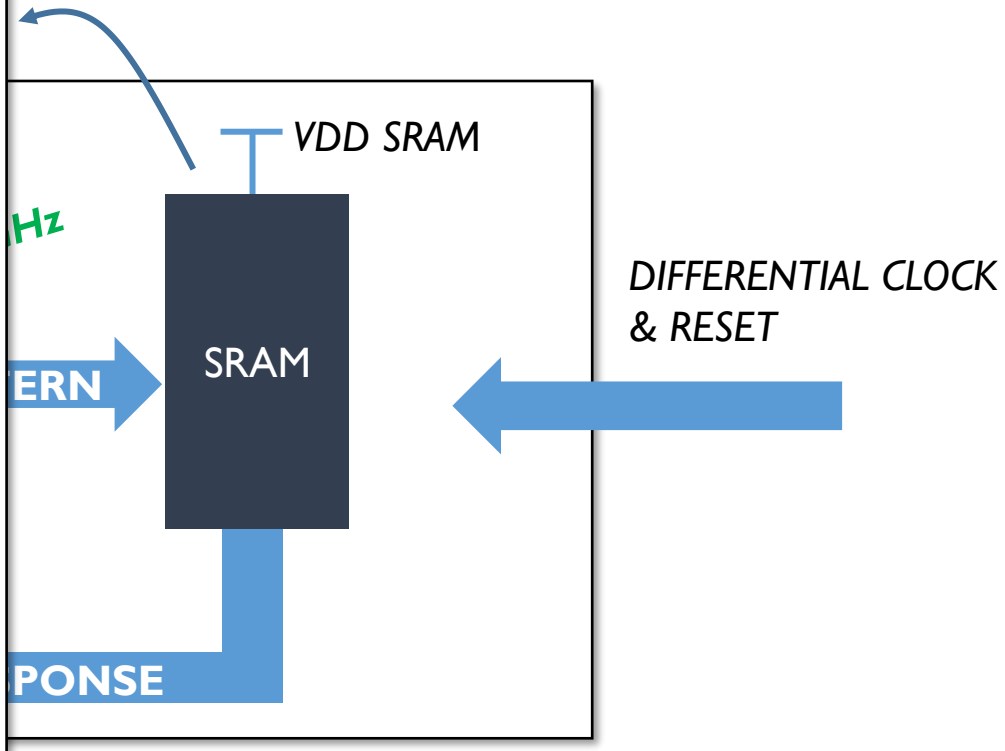
UCTURE

RY (ACCESS TIME ~ FEW NS)

NSISTOR SIZE

L PORT, STANDARD/ULTRA-HIGH DENSITY)





What's next?

Technology evaluation and development keep going

Depends on testing results and technology availability:

- SRAM custom development
- Evaluation of new technology as 22 nm FTX-SOI, FinFET,…

Explore new design solution

Transition from on-chip configurability to programmability:

- System-on-chip design solution
- New field of research for EP-ESE-ME
- Apply to several applications

Radiation tolerant System-On-Chip ecosystem for HEP application

Two complementary field of research:

Control & Monitoring

RISC-V based

- Standardized solition
- Open source
- Fully radiation tolerant
- ECO system for the community
  - RT SOC IP blocks
  - RT SOC interconnect

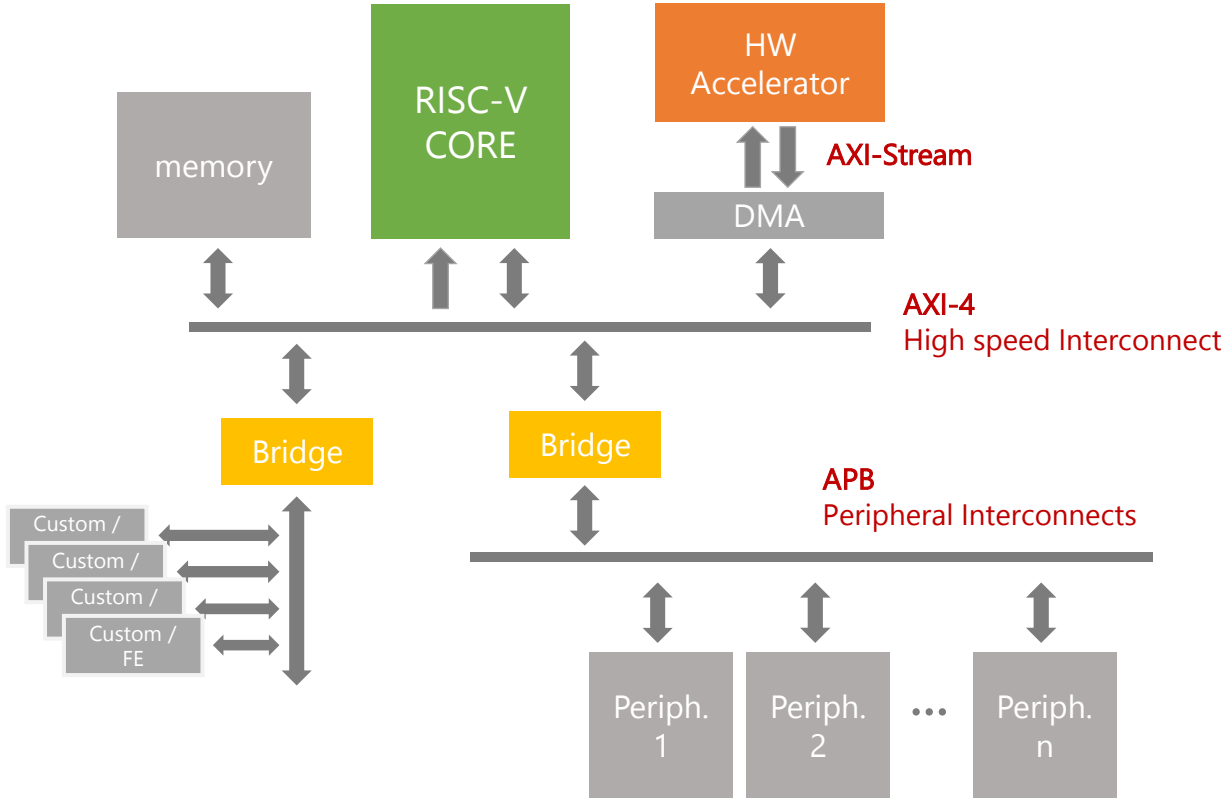
Data Processing

ASIP based

- Application specific instruction set processor
- Tool based – ASIP designer by Synopsis
- Custom ISA
- Custom microarchitecture

RISC-V BASED SOC ECOSYSTEM

- SURVEY OF DIFFERENT ARCHITECTURES
- EXPLORED SOLUTIONS:
  - ETH PULP-PLATFORM
  - CHISEL BASED ROCKET-CHIP
  - PICORV32
- **EMPLOY RADIATION HARDENING DESIGN TECHNIQUES**
- DEMONSTRATOR ASIC IS IN DEVELOPMENT

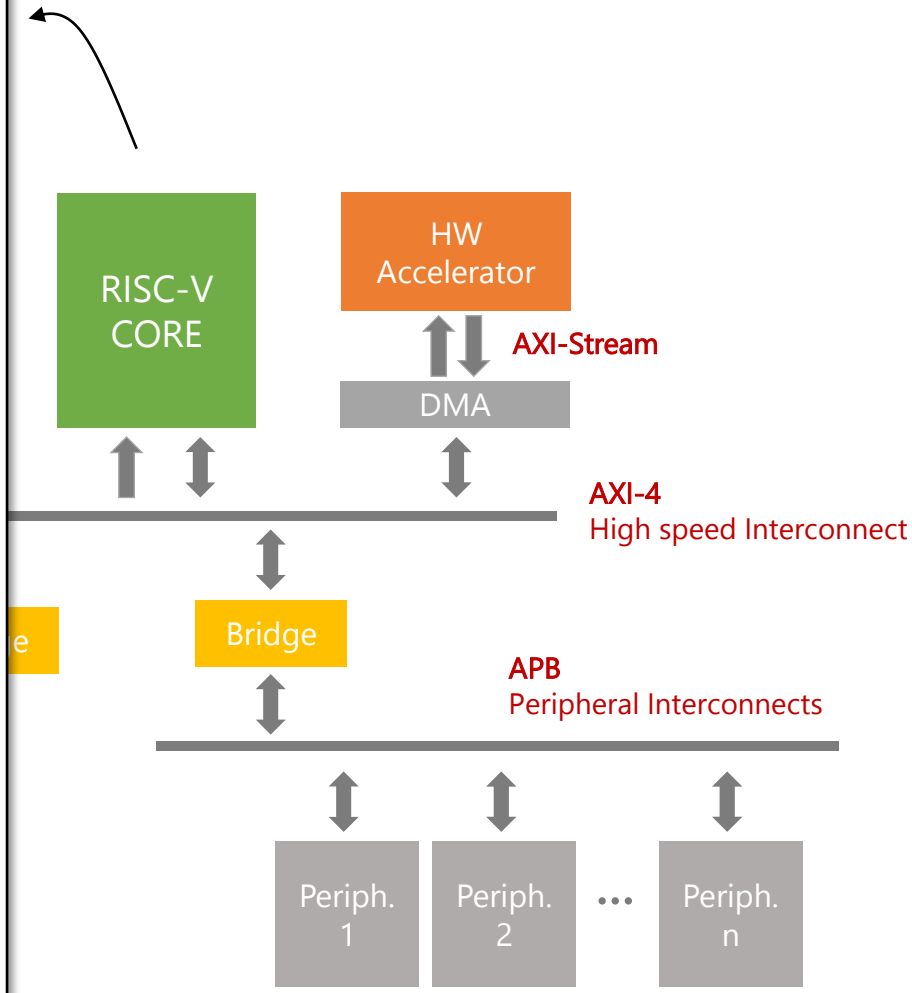


slide by Alessandro Caratelli

RISC-V®

- OPEN SOURCE ISA, MANY OPEN SOURCE IMPLEMENTATIONS
- ISA DESIGNED FOR SIMPLICITY, "EASY" TO IMPLEMENT
- VERY LIKELY TO TAKE OVER VARIOUS AREAS OF CPU MARKET
- FUNDED AND DEVELOPED BY MANY BIG COMPANIES
- NO LICENSE LIMITATION, NO VENDOR ROYALTIES
- PROFIT FROM COMMUNITY CONTRIBUTIONS

NB: NOT ALL RISCV CORES ARE WITH AN OPEN LICENSE



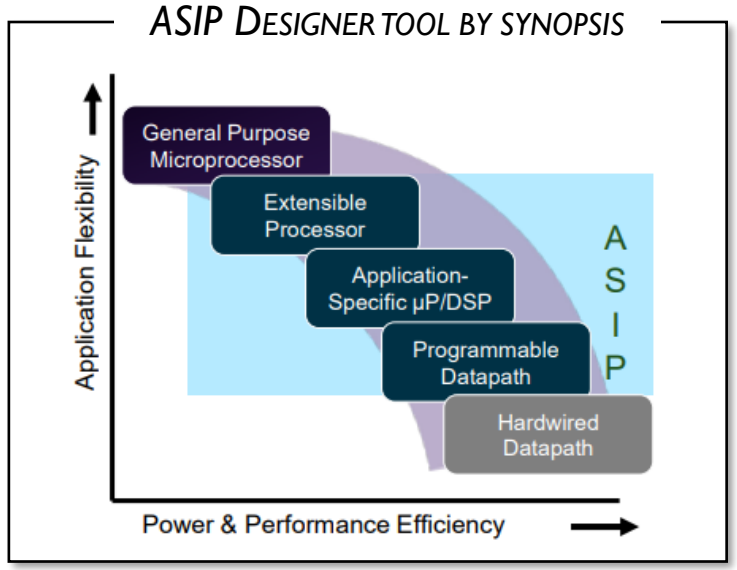
slide by Alessandro Caratelli

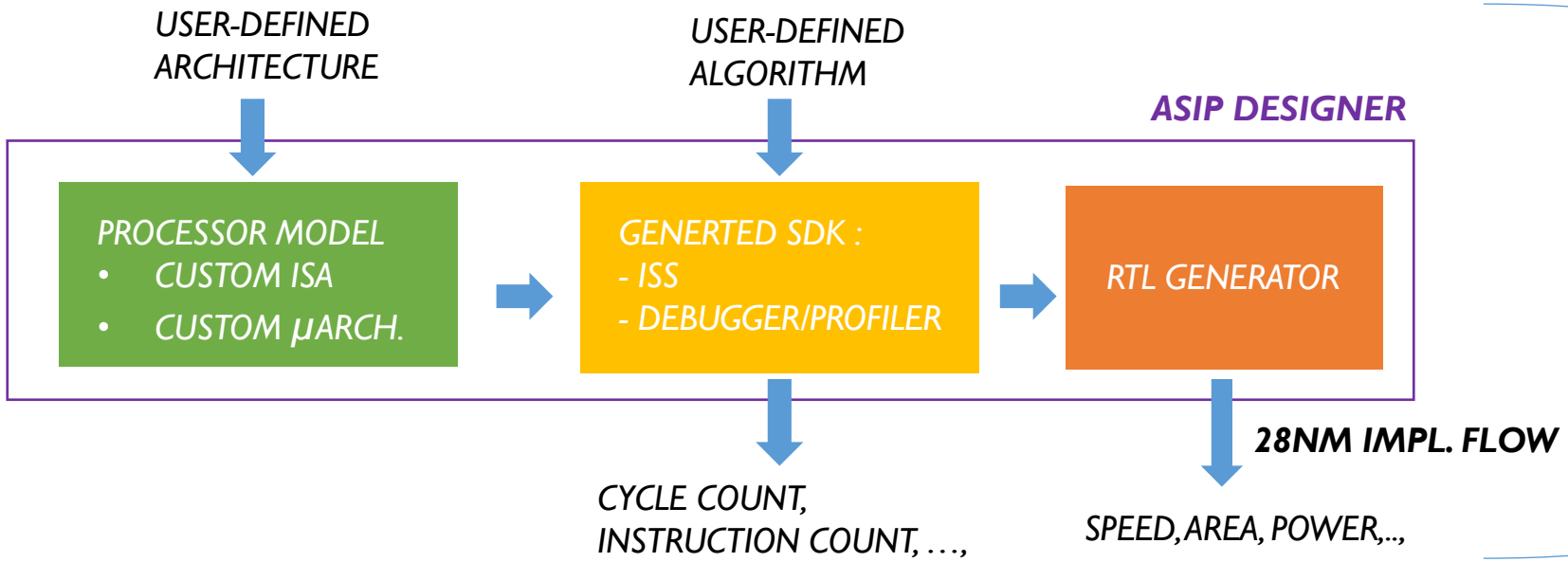
ON-CHIP DATA PROCESSING: A FEASIBILITY STUDY

PROVIDE PHYSICS DATA AND RUN EXISTING ALGORITHM

ON A CUSTOMIZED PROCESSOR:

- *TRAINEE STARTED ON FEBRUARY 2022*
- *ASIP DESIGNER LICENSE OBTAINED IN MARCH 2022*
- *COLLABORATION STARTED IN MAY 2022 – THANKS M. CAMPBELL*





WORKFLOW IN PLACE TO STUDY THE FEASIBILITY OF ON-CHIP DATA PROCESSING

Conclusions

Significant progress on 28 nm technology evaluation in the last year :

- TID chip submitted and charachterized
  - provides radiation tolerance performance at transistor level
- Exp28 suite submitted in December `22 - testing ( started in May `22) will provide:
  - TID and SEE evaluation of digital building blocks (std. cell and SRAM)
  - Charachterization of IP blocks
  - Design guidelines for analog and digital rad-tol design

Transition from tech. evaluation to investigation of new design solution is started:

- RISC-V based system-on-chip solution for control and monitoring application
- custom processor design solution for on-chip data processing application

EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

THANKS!

DAVIDE CERESA