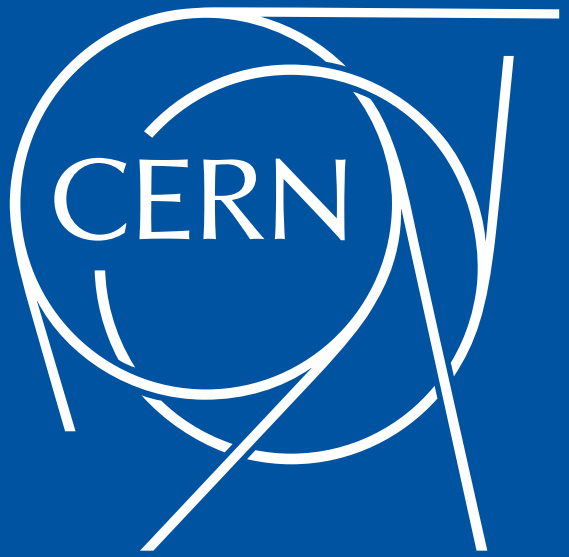
CERN

WP5.2a: IP Blocks in 28nm for the HEP Community

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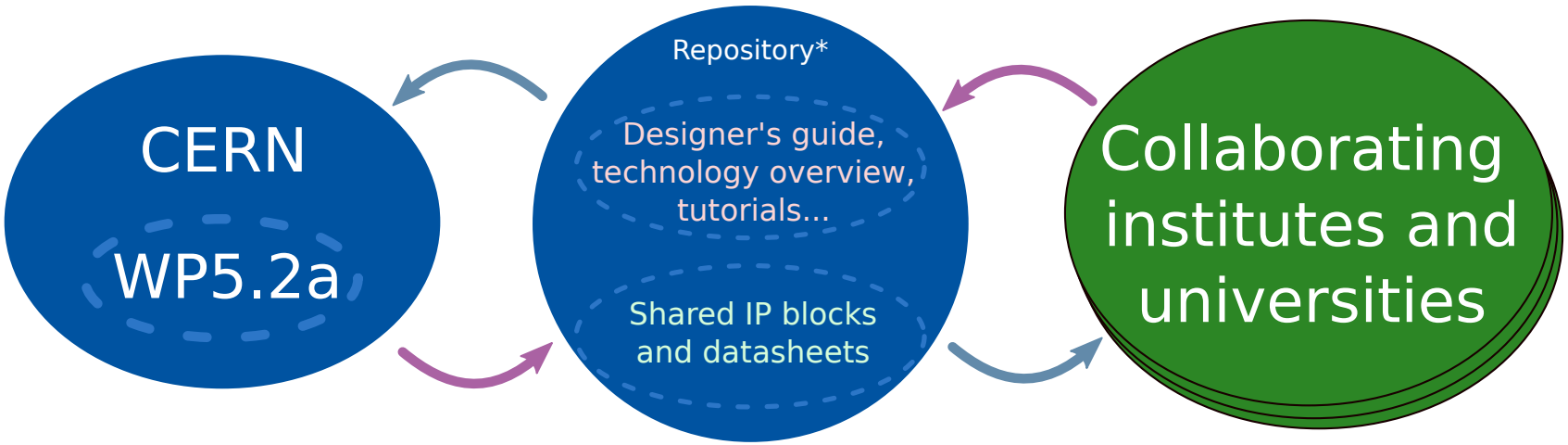
WP5.2a: What we do?



Intellectual Property (IP) blocks design

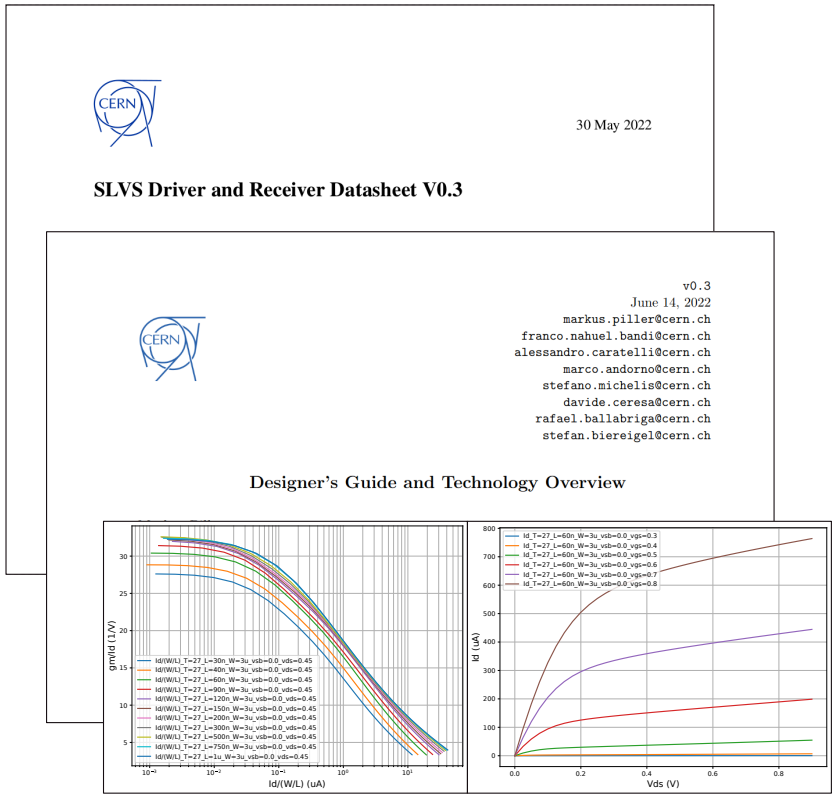
Intellectual Property (IP) blocks use

IP block example: DAC, ADC, voltage reference, transmitter, receiver, PLL...

*thanks to CERN ASIC Support Team: A. Caratelli and M. Andorno

Motivation

- Familiarize new designers with the technology (short document with practical information)[1].
- We propose guidelines to homogenize choices and enable block sharing within the community.



[1]The documentation is available (thanks to CERN ASIC Support Team: A. Caratelli and M. Andorno):

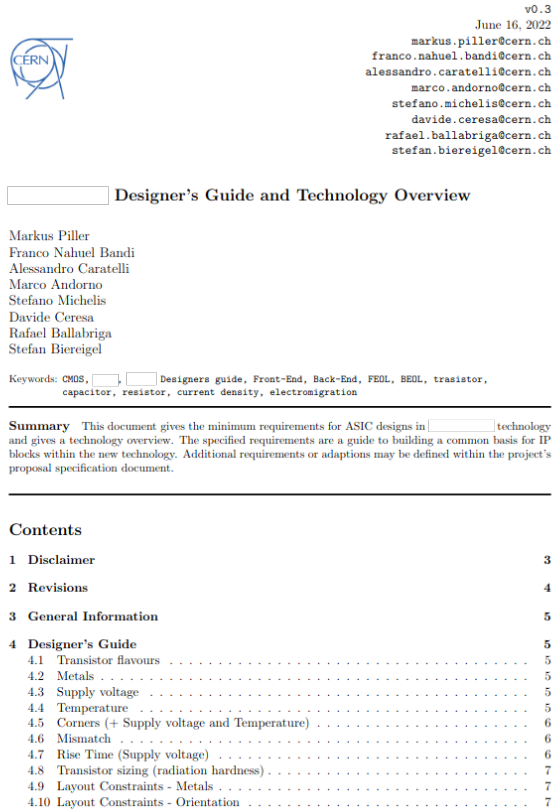
- Web page: https://asicsupport.web.cern.ch/
- Forum: https://asicsupport-community.web.cern.ch/

Designer's Guide and Technology Overview

We have prepared a "Designer's Guide" with selected technical information and proposed design guidelines that facilitate collaborative design work.

Features of the technology:

- 28nm CMOS process.
- Single poly and 9 metal stack + AP (AL RDL).
- 0.9V core transistors (ulvt, lvt, reg, uhvt and sr) and 1.8 I/O transistors.
- Retrograde twin well and Deep N-well.
- High-R, unsilicided diffusion, N-Well...
- MOMcap and MOScap.
- Only vertical poly is allowed[2].



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Designer's Guide and Technology Overview

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Rafael Ballabriga
Stefan Biereigel

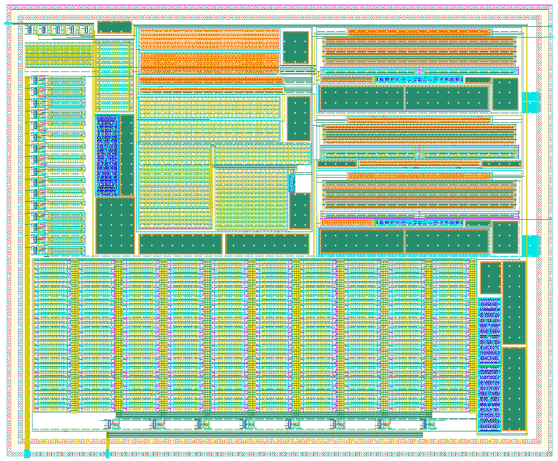
Keywords: CMOS, , Designers guide, Front-End, Back-End, FEOL, BEOL, trasistor, capacitor, resistor, current density, electromigration

Summary This document gives the minimum requirements for ASIC designs in technology and gives a technology overview. The specified requirements are a guide to building a common basis for IP blocks within the new technology. Additional requirements or adaptions may be defined within the project's proposal specification document.

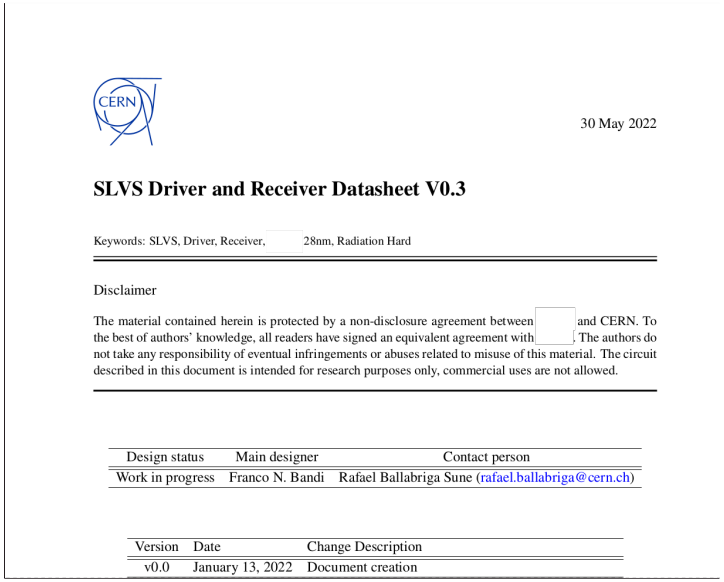
Contents

[2]Enclosed layout not possible. Also, some IP blocks need vertical and horizontal version (extra work!!).

Datasheets



8-bit DAC layout (M. Piller)



30 May 2022

SLVS Driver and Receiver Datasheet V0.3

Keywords: SLVS, Driver, Receiver, 28nm, Radiation Hard

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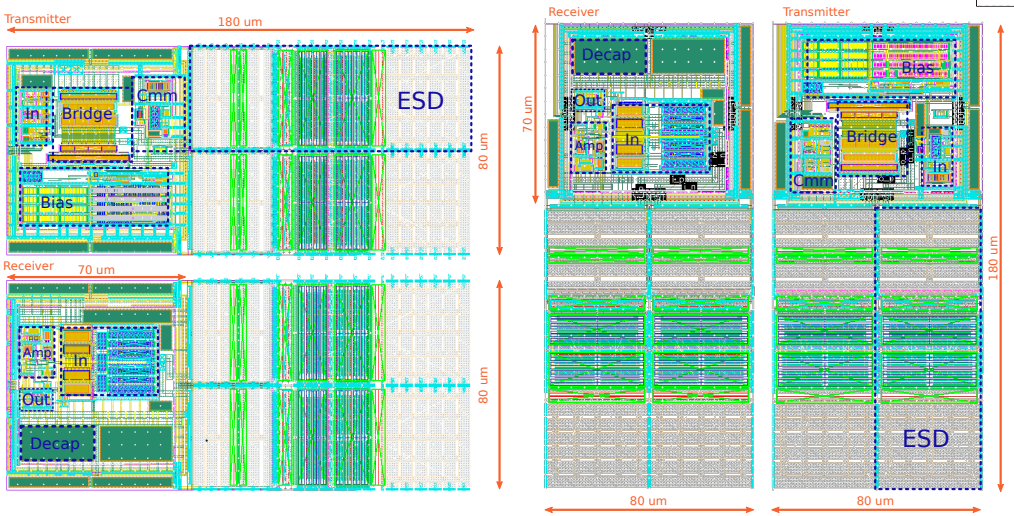
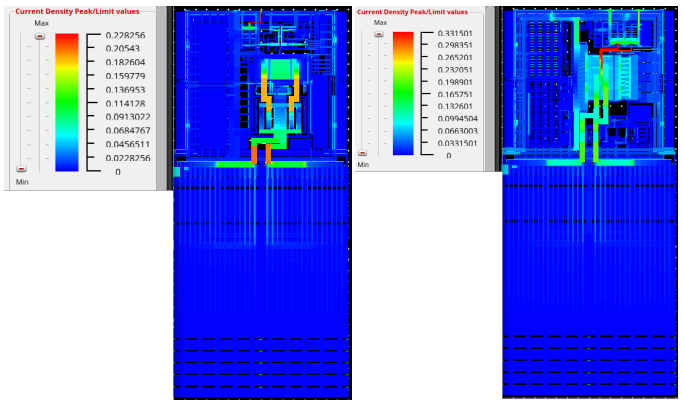
Design status	Main designer	Contact person
Work in progress	Franco N. Bandi	Rafael Ballabriga Sune (rafael.ballabriga@cern.ch)

Version	Date	Change Description
v0.0	January 13, 2022	Document creation



Transmitter and receiver layout



Electromigration analysis

Documentation

Analog IP Blocks

Conclusions

IP Block Library (Design Finished)

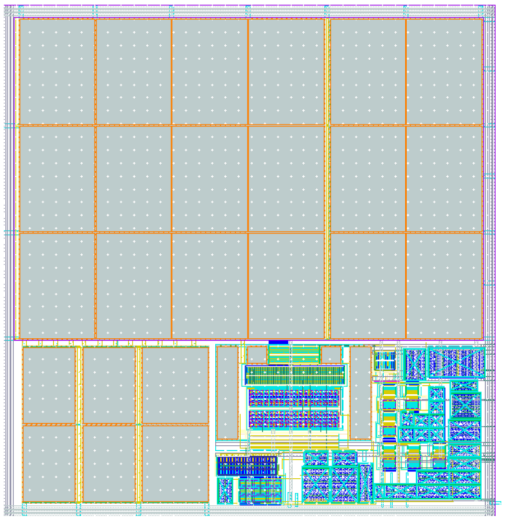
Circuits to share	Notes
Bandgap voltage reference and temperature monitor	Block submitted in January 2022. Development lead by **G. Traversi (Bergamo/Pavia) collaboration with the INFN Falaphel project** with support from CERN engineers.
Digital to Analog Converter (8-bit)	Core block submitted in January 2022. Development lead by M. Piller (DOCT, Austrian programme).
Differential line drivers and receivers	Block submitted in January 2022. Development lead by F. Bandi (WP5 FELL).
Rail to Rail Operational Amplifier	Completed. To be submitted in 2022. Development lead by J. Kaplon (STAFF).
Radiation tolerant ESD protections	Design outsorced to Sofics.

Design followed guidelines for radiation hardness from the initial technological characterization. Testing ongoing for validating the design.

Bandgap Voltage Reference (by G. Traversi)

Designed by **Bergamo-Pavia in collaboration with the INFN Falaphel project (Main designer: G. Traversi)** and technical support from CERN.

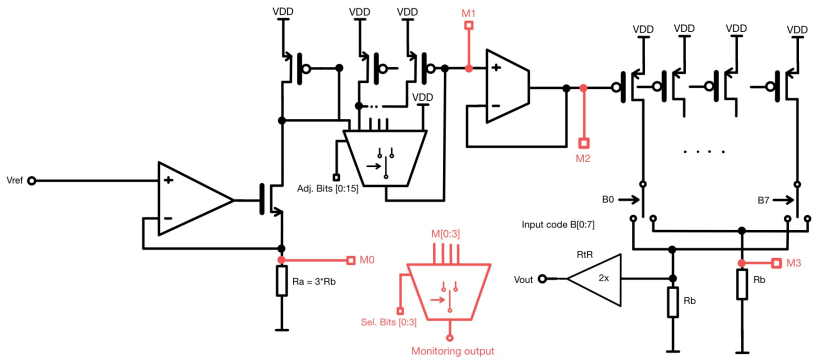
Parameter	Min	Typ	Max	Unit
Voltage supply	0.81	0.9	0.99	V
Output voltage		480		mV
Current supply		100		µA
Temperature	-40	25	60	°C
ΔVref max vs Temp		3		mV
ΔVref max vs Vdd±10 %		2		mV
Target PSR (low frequencies)		40		dB
Active element	lvt in weak inversion			



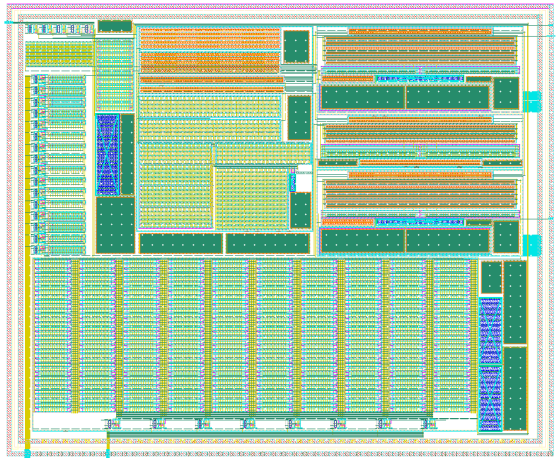
8 Bit DAC (by M. Piller)

The 8 bit digital-to-analog converter is intent to be a IP block for biasing purposes.

- 8 bit digital-to-analog conversion.
- Output voltage before RtR 0 to $V_{DD}/2$.
- INL < 0.5.
- I_{LSB} digital current adjustment.
- $I_{LSB} = 50nA$.



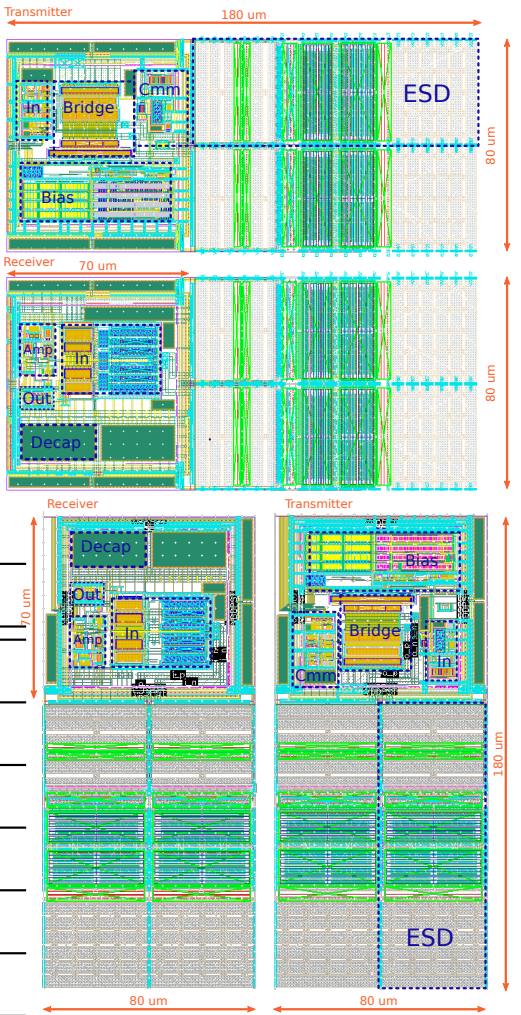
Parameter	Min	Typ	Max	Unit
Voltage supply	0.81	0.9	0.99	V
INL			0.38	
Temperature	-40	25	80	°C
Area		220×267		μm^2
Metal stack		1-2-3 (4,5 power)		metals



SLVS Transmitter and Receiver (by F. Bandi)

The design targets mainly on-board chip-to-chip communication in rad-hard applications (1 Grad). Therefore, only thin-gate transistor should be used to ensure higher radiation tolerance [1].

- Disable signal.
- Inverter function.
- Compatible with low voltage design ($V_{ddcore} = 0.8\,V$).
- Level shifting: from V_{ddcore} to V_{ddIO}.
- Tx: $I_{out} = 4\,mA$.
- Rx: termination on/off switch and fail-safe resistors.



Parameter	Min	Typ	Max	Unit
IO voltage supply	1.08	1.2	1.32	V
Core voltage supply	0.72	0.9	0.99	V
Data rate	0		1.28	Gbps
Temperature	-40		80	°C
Area with ESD		180×80		μm^2
Metal stack		1-2-3(4 power)		metals

Rail to Rail OPAMP (by J. Kaplon)

Parameter	Min	Typ	Max	Unit
Open loop Gain	70	75		dB
GBP (uncompensated)		1.6		GHz
Current supply			400	µA
PM (unity gain for 0-1nF load and 10 Ω series resistor required)	66	74		°
Settling time (1 %)			35	ns
Output noise (unity gain)			150	µV
Offset rms (unity gain)			1.5	mV
Area (amplifier and bias)		$44 \times 70 + 44 \times 90$		μm^2
Area (amplifier, bias, decoupling and compensation)		140×160		μm^2

Characterization Set-up

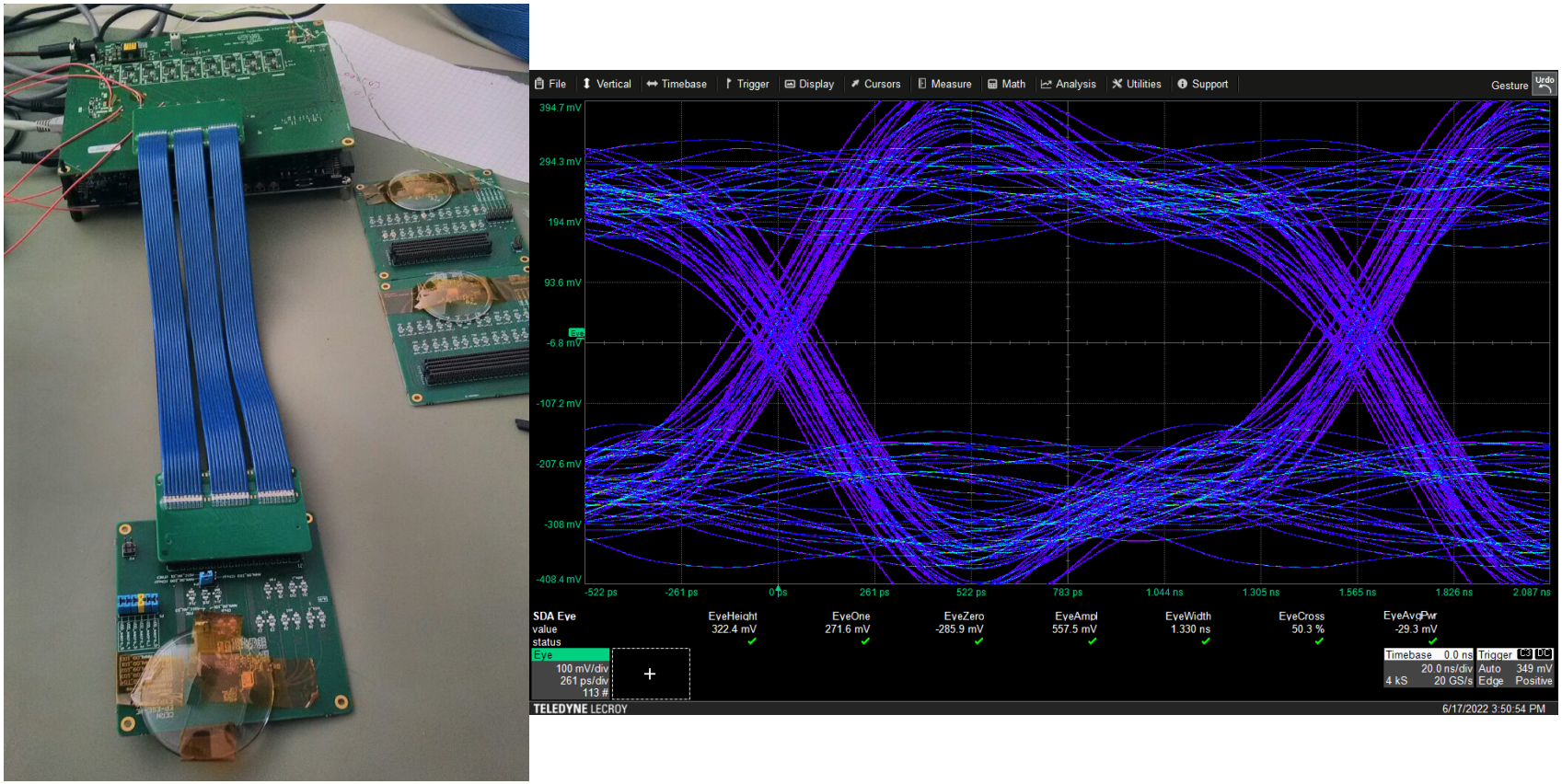


Figure: Left, PCB with wire-bonded chip (bottom) and common test system (top). Right, eye diagram at 640 MHz (preliminary). Acknowledgment: Giulio Borghello, Davide Ceresa, Francisco Piernas Díaz, Risto Pejasinovic.

IP Block Library (Work In Progress)

Circuits to share	Notes
Analog to Digital Converter for monitoring (12-bit)	In progress. Development lead by T. Hofmann (WP5 FELL). Synergies WP6.
Rail to Rail Operational Amplifier (slow (e.g. monitoring in unity gain configuration))	In progress. To be submitted in 2022. Development lead by M. Piller (DOCT, Austrian programme).
Analog PLL	In progress. Development lead by F. Bandi. Synergies with LHCb PicoPix project.
Digital PLL	Design start expected for Q4 2022. Development lead by T. Hofmann (WP5 FELL).
DCDC converter and LDO	In progress. Development lead by S. Michelis (STAFF) and G. Ripamonti (STAFF)
Radiation tolerant CMOS IO Pad	Design outsorced to Sofics

Application specific blocks (front-end): amplification, filtering and discrimination:

- For 2-D readout circuits (input cap. $<$100fF and leakage current per pixel $<$20nA). Collaboration WP1.1-WP5 (V. Sriskaran (WP1.1 FELL) and S. Emiliani (WP5 TECH)).
- For sensors with intrinsic amplification (SiPM, MCP, PMT). M. Piller (DOCT, Austrian Programme).

Documentation

Analog IP Blocks

Conclusions

Conclusions

- We have created documentation for quick adoption of the technology for the community (technology overview, designer's guide...).
- Some IP blocks were submitted in January 2022 and more circuits are under design. The blocks are documented.
- We have created synergies with other WPs and with external groups in the community:
  - WP1.1: Charge sensitive amplifier, shaper and comparator for 2-D readout circuits. V. Sriskaran (FELL WP1.1) and S. Emiliani (TECH WP5).
  - WP6: 12-bit Analog to Digital Converter for monitoring. T. Hofmann (FELL WP5).
  - Bandgap codesign by **G. Traversi at University of Bergamo/Pavia in collaboration with the INFN Falaphel project.**

Future Work

- The characterization of prototypied blocks has started (functional). TID measurements will start in the following weeks (see Davide's presentation).
- A design programme has been determined for the coming years (APLL, DPLL, high resolution ADC).
- However, the results from testing will determine the future efforts:
  - Iterate on some of the blocks to make them more rad hard.
  - Focus the design effort on new IP blocks (for example in case of SRAMs not being radiation-hard enough).

Bibliography

[1] Giulio Borghello, *Advantages of 28nm technology in ultra-high-TID environments*, Forum on 28nm CMOS (CERN), Login and access required., 2020. https://indico.cern.ch/event/970389/contributions /4097899/attachments /2141534/3608590/Advantages%20of%2028nm %20CMOS%20Technology%20in%20Ultra-High-TID%20Environments %20-%20Giulio%20Borghello.pdf

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[3] Davide Ceresa, *EXP28 – Test chips to explore and experience a 28 nm technology*, PJVU (CERN), Login and access required., 2021. https://indico.cern.ch/event/1091795/


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