EP R&D Day 2022 WP5.2 powering solutions

S. Michelis, G. Ripamonti, P. Antoszczuk, G. Bantemits, K. Khalife, M. Balutto, L. Johansson , N. Galante 20/06/2022



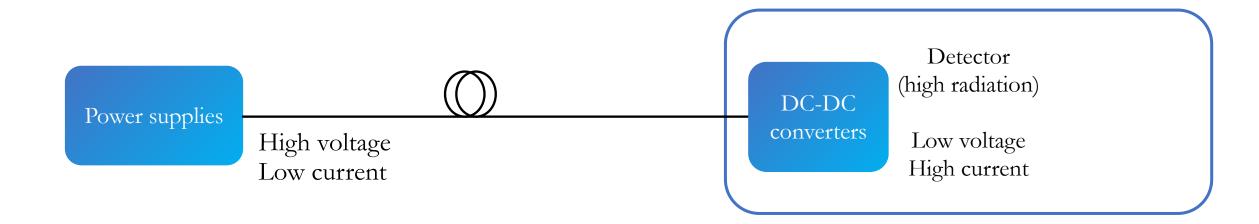
Team players

Today working on the RD WP5.2:
Stefano Michelis (Staff, DCDC project coordinator)
Giacomo Ripamonti (Staff)
Pablo Antoszczuk (WP5 Fellow)
Georgios Bantemits (WP5 Fellow)
Khalil Khalife (WP5 Internship from EPFL)
Marco Adorno (Fellow, ASIC support team)
Alessandro Caratelli (Staff, ASIC support team)

People that have contributed in the past: Mattia Balutto (WP5 Technical Student) Leo Johansson (WP5 Internship from EPFL) Nicolas Galante (WP5 Internship from EPFL)



Power management and distribution



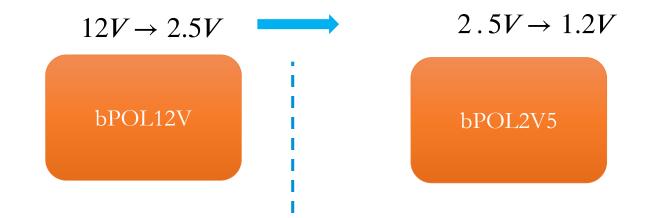




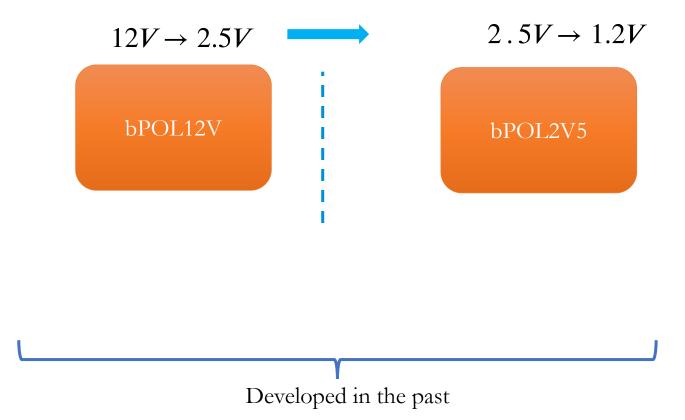
 $12V \rightarrow 2.5V$



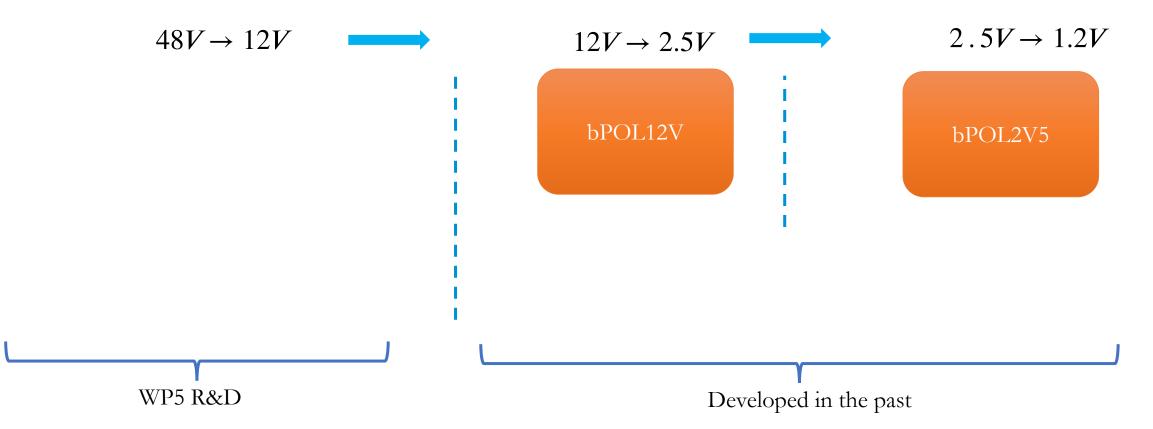




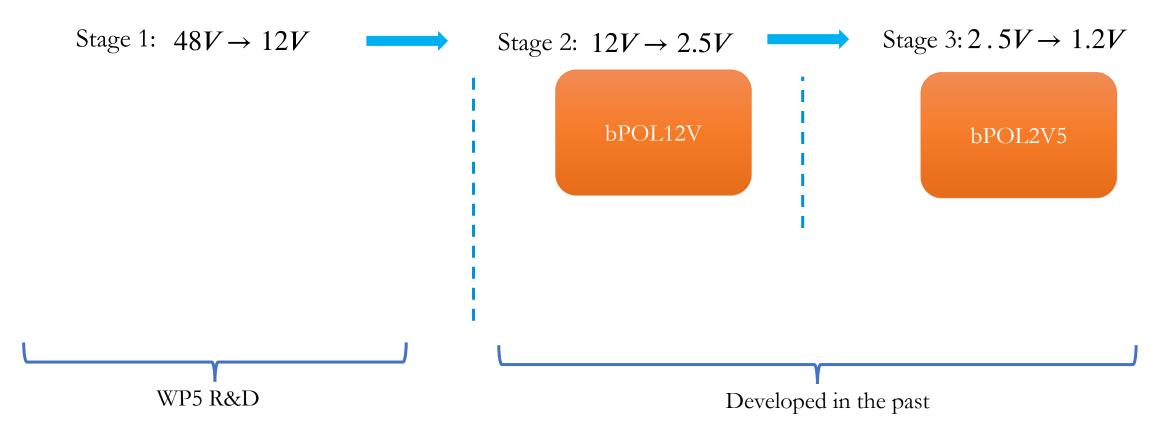




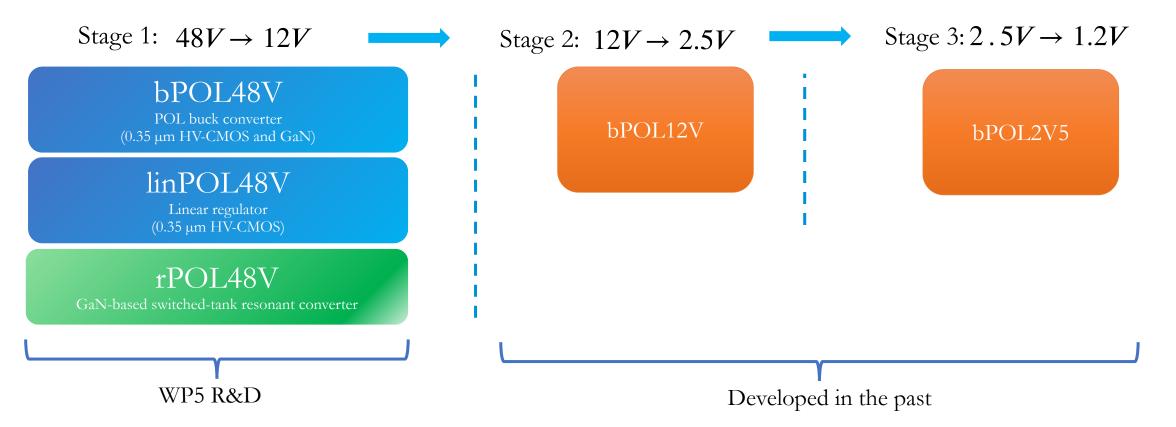












WP5 R&D and now in production grade/in production WP5 R&D and KT funds

Already developed outside WP5



bPOL48V is composed by:

a commercial Gallium Nitride (GaN) power stage EPC2152

a rad-hard controller designed by CERN (Si_Buck_Controller) in the Silicon HV-CMOS OnSemi I3T80 technology

specs	Vin max	48V
	Typ Vout	12V
	Iout max	12A
Rad specs	TID max	228 Mrad
	SEE max	88 MeV/(mg/cm ²)
	DD max	4e14 n/cm2 2.23e14 p/cm2(30MeV)
Production	26000 dies produced	

NB TID=Total Ionizing Dose SEE= Single Event Effect DD= Displacment Damage



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RD with WP5 of only 2.5 years. Already in production

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Possible big customers:

- ATLAS Lar calorimeter
- Space industry

Success of this project due to:

- maturity of the EP-ESE-ME knowledge in High Voltage CMOS technology
- maturity of the GaN technology
- close collaboration with GaN manufacturer



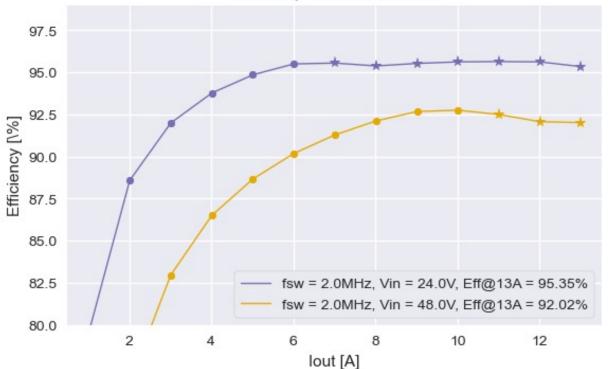
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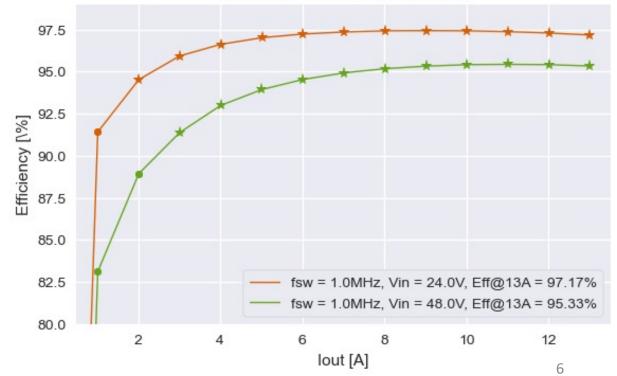


Efficiency - 220nH Air Core

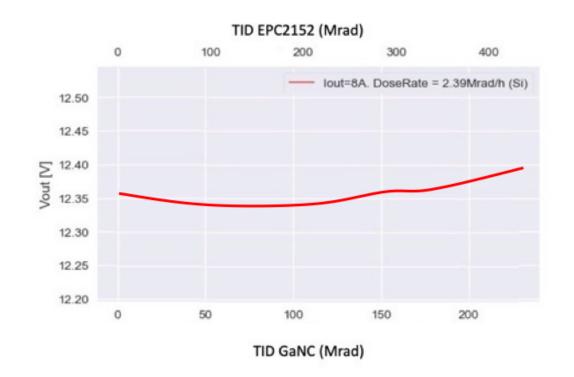




Efficiency - 2.2un Ferromagnetic



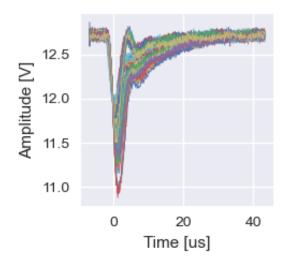
TID (Total Ionizing Dose)

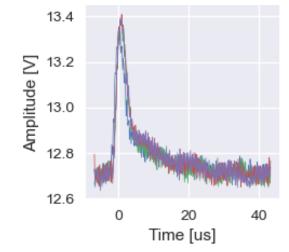


SEE (Single Event Effect)

Succesfully tested up to LET=88 MeV/(mg/cm²) (space grade) Only fast transients seen (2-3us), no permanent damage or long-resets

For CERN applications LET=46 MeV/(mg/cm²) transients are less than 20% of Vout







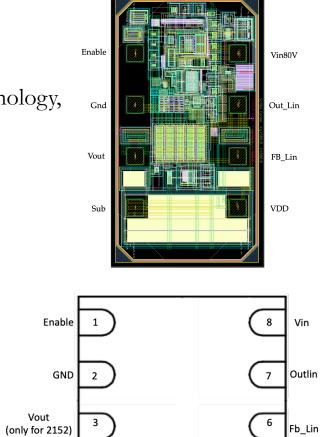


Stage1 linPOL48V: 48V-input linear regulator

LinPOL48V is a rad-hard linear regulator designed in the HV-CMOS OnSemi I3T80 technology, available in DFN8 package

RD with WP5 of only 2.5 years. Already in production

specs	Vin max	48V	
	Typ Vout	12V	
	Iout max	200mA	
Rad specs	TID max	700 Mrad	
	SEE max	88 MeV/(mg/cm ²)	
	DD max	4e14 n/cm2 2.23e14 p/cm2(30MeV)	
Production	30000 dies produced		



Top view 8-lead plastic DFN (2x2mm) Therm pad must be soldered to PCB Gnd

Vout

GND

NB TID=Total Ionizing Dose SEE= Single Event Effect DD= Displacment Damage VDD

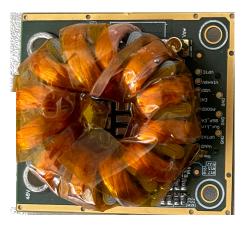
(only for 2152)



Stage1 R&D rPOL48V: 48V-input Switched Tank Converter (STC)

rPOL48V is a WP5.2/KT-fund development **in collaboration with University of Udine**, aiming to a 50A very compact and efficient DCDC converter, fixed ratio 4. First prototype is built with commercial non-rad hard controller, as demonstrator

bPOL48V (buck) production grade



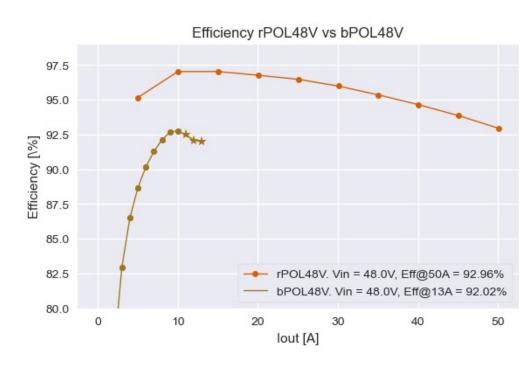


VS.

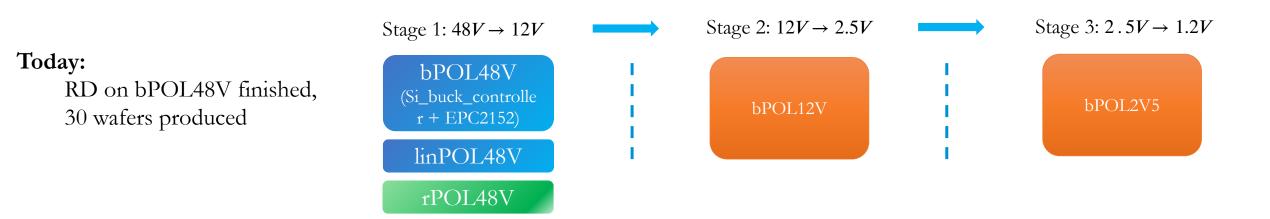
rPOL48V (resonant)



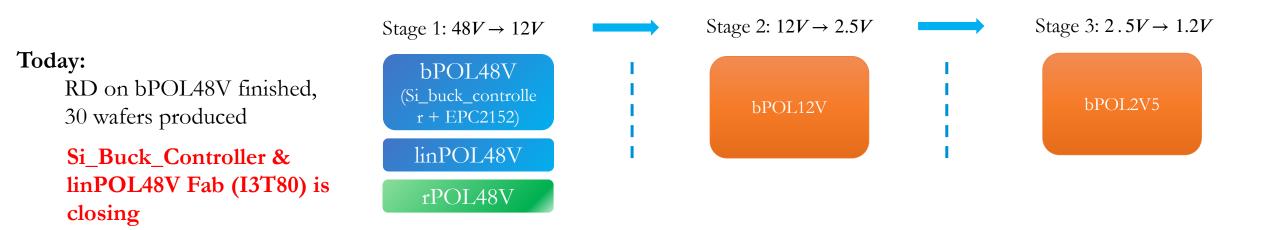




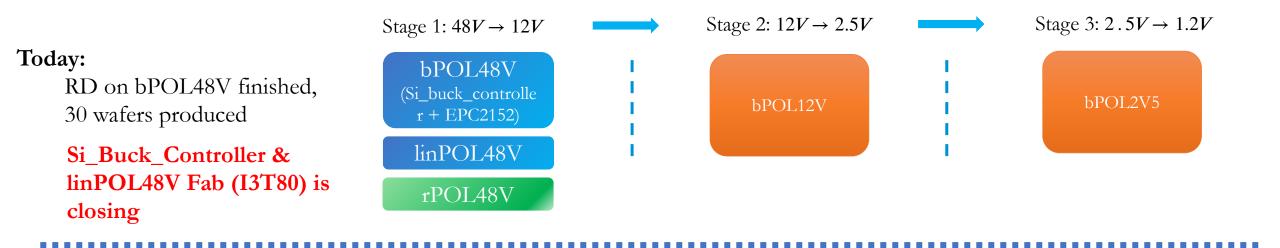








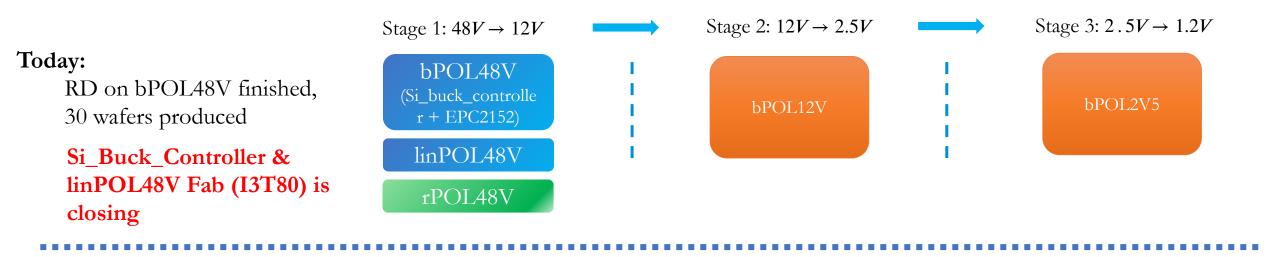




Future R&D:

Not originally included in the WP5 RD program

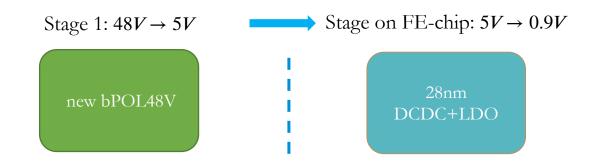




Future R&D:

Not originally included in the WP5 RD program

New HV Stage1 (HV CMOS technology and GaN) DCDC converter in 28nm TSMC





Future development for long term R&D in WP5

Stage 1: $48V \rightarrow 5V$



We need to find a new suitable High Voltage technology and test it for radiation. Full radiation caracterization takes at least 1 year

- Design and production of test chips
- Radiation testing:
 - TID (Total Ionizing Dose)
 - SEE (Single Event Effect)
 - DD (Displacement Damage)

Stage on FE-Chip: $5V \rightarrow 0.9V$

Fully integrated DCDC in 28nm TSMC All On-Chip (caps, inductor, 200MHz) + LDOs

28nm TSMC technology already fully characterized for radiation



Future R&D Stage 1: HV technology

Work in progress to find an alternative for:

• HV CMOS technology

OnSemi I4T: 2 testchips submitted in 2021 in I4T OnSemi technology. Outcome not very promising

OnSemi I3T80 in Gresham: Onsemi is moving the production to the US Fab. Testchips are being manufactured

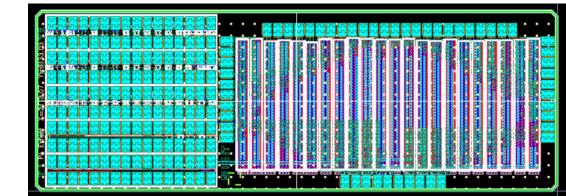
ST 0.16 BCD SOI: we try to get the PDK and design testchips

• GaN technology:

close collaboration with EPC

IMEC GaN 200V: testchips are in their way to CERN

OnSemi I4T radiation results					
Transistor Voltage (V)	TID (total Ionizing dose)	SEE (Single Event Effect), mainly SEB (Single Event Burn-out)		DD (Displacement Damage)	
1.8	ok	О	k		
3.3	Leakage, very large Vth degradation	ok		On-going in	
15	High leakage in	e in All NMOS suffers of SEB PMOS OK	SEB at 11V	Irrad facility	
30			SEB at 20V		
45	NMOS			SEB at 25V	
70			SEB at 30V		





Future R&D Stage On-Chip in 28nm technology 5V -> 0.9V

Added value:

precise power distribution on-chip

possible to have different voltage domains from only one input voltage at 5V

large reduction of input current (factor 4)

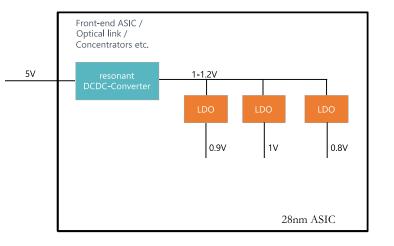
radiation tolerance up to 1Grad

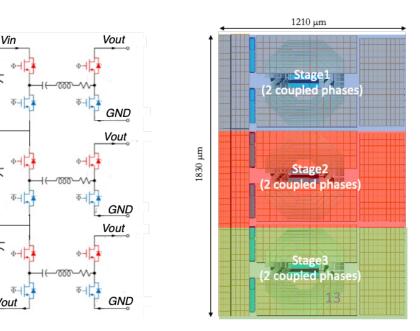
fully integrated including all passive components, relaxing PCB design

based on a resonant modular architecture

Design started, submission of the first prototype in Nov 2022

Linear regulator design is ongoing in collaboration with TU university of Graz





UNE



Summary

Name	Status	Availability	WP5 plan
bPOL48V	Fully tested Radiation tolerance OK	Already produced 30 wafers available ~30k samples	Originally the only planned activity
linPOL48V	TID, DD, SEE		
rPOL48V	First prototype Tests ongoing Commercial drivers FPGA control Rad-hard controller being designed at CERN		Side development with also KT funds
Technology characterization	OnSemi I4T OnSemi I3T80 from Gresham Fab ST 0.16 BCD SOI IMEC GaN 200V		New WP5 R&D added
DCDC converter in 28nm	Design in progress		