In-System Parameter Update and I/O Capture for Machine Learning IP Cores

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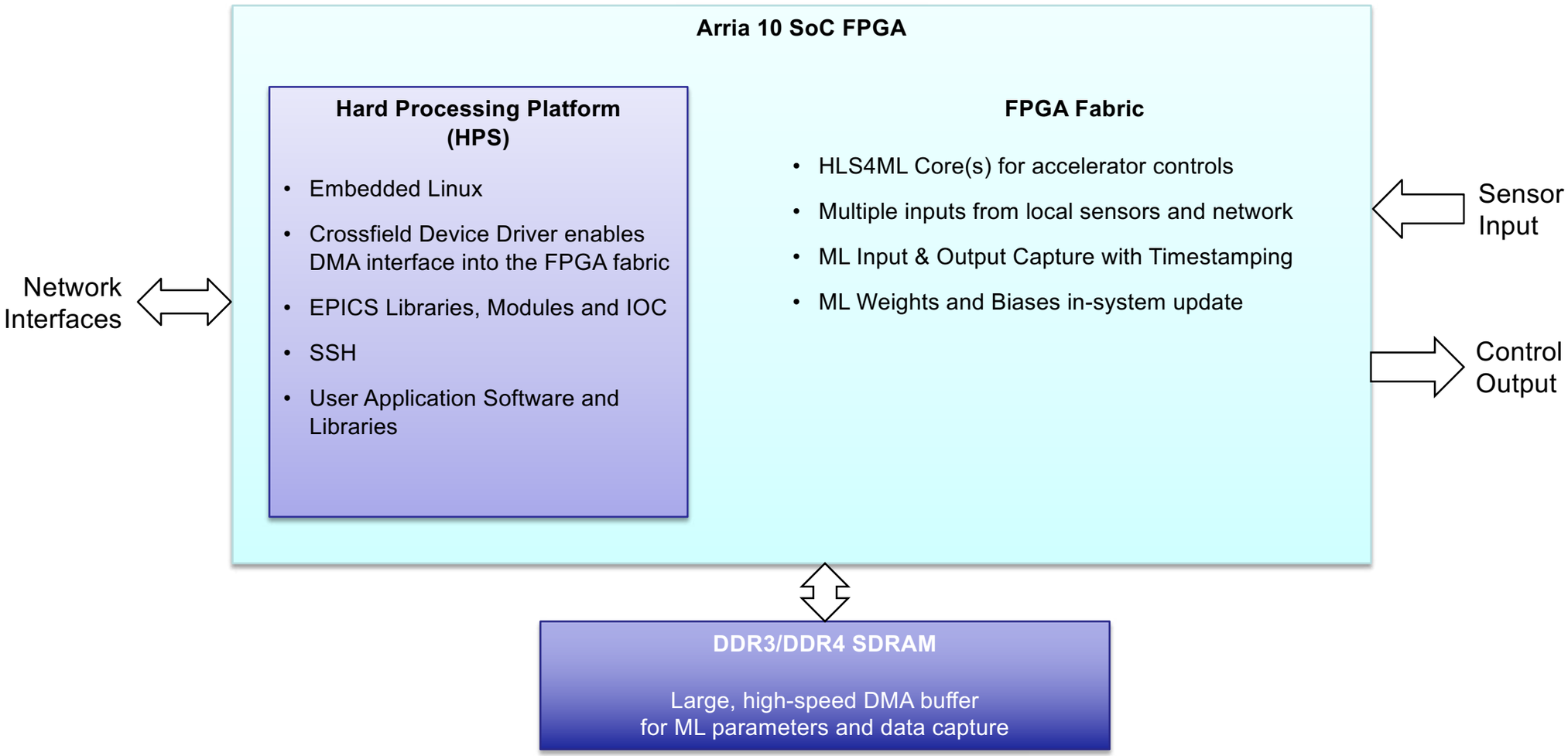
Overview

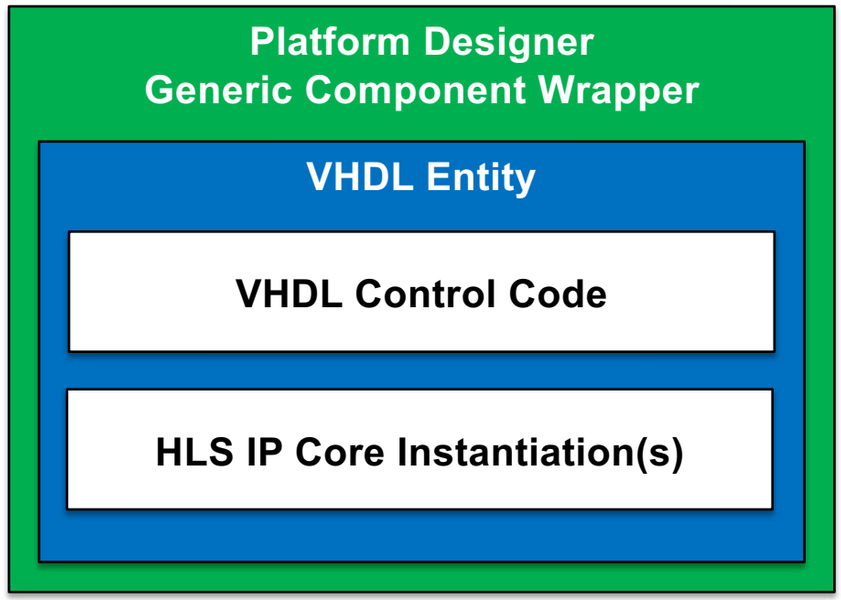
- Crossfield Technology & U.S. Department of Energy SBIR Program (currently in Phase II)
  - Teaming with Fermilab READS and Booster groups
- Update ML weights and biases from the embedded Linux running in the ARM Hard Processing System (HPS) using Direct Memory Access (DMA) to transfer the parameters between SDRAM and FPGA memory
- Capture input into and output out of the HLS4ML IP core through the HPS
- Provide a method to write input into the HLS4ML IP core from the HPS
- Develop a graphical application to remotely update parameters in the FPGA and capture input & output feedback (in development)
- Focus on Intel FPGAs

Top Level View



Reusable, User-Friendly Components

- HLS Components wrapped with VHDL (including HLS4ML component)
- Customized for Platform Designer
- Contains control logic so end users only connect components graphically
- Crossfield provides source code for customization
- Minimal programming for rapid development and dropping in new HLS4ML components



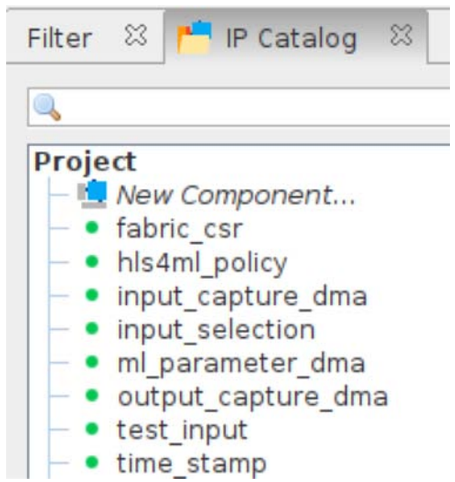
Simple Hardware Design Customization

- config.h
  - Number of inputs
  - Number of parameters
  - Number of outputs
  - Enable/disable input capture
  - Enable/disable output capture
  - Enable input from HLS
- config.tcl
  - Input bus bit width
  - Output bus bit width

- Modify VHDL/hls4ml.vhd to to replace instantiated HLS4ML component
- Add symbolic link to Quartus project
- Run script to build and copy IP cores into Quartus Project

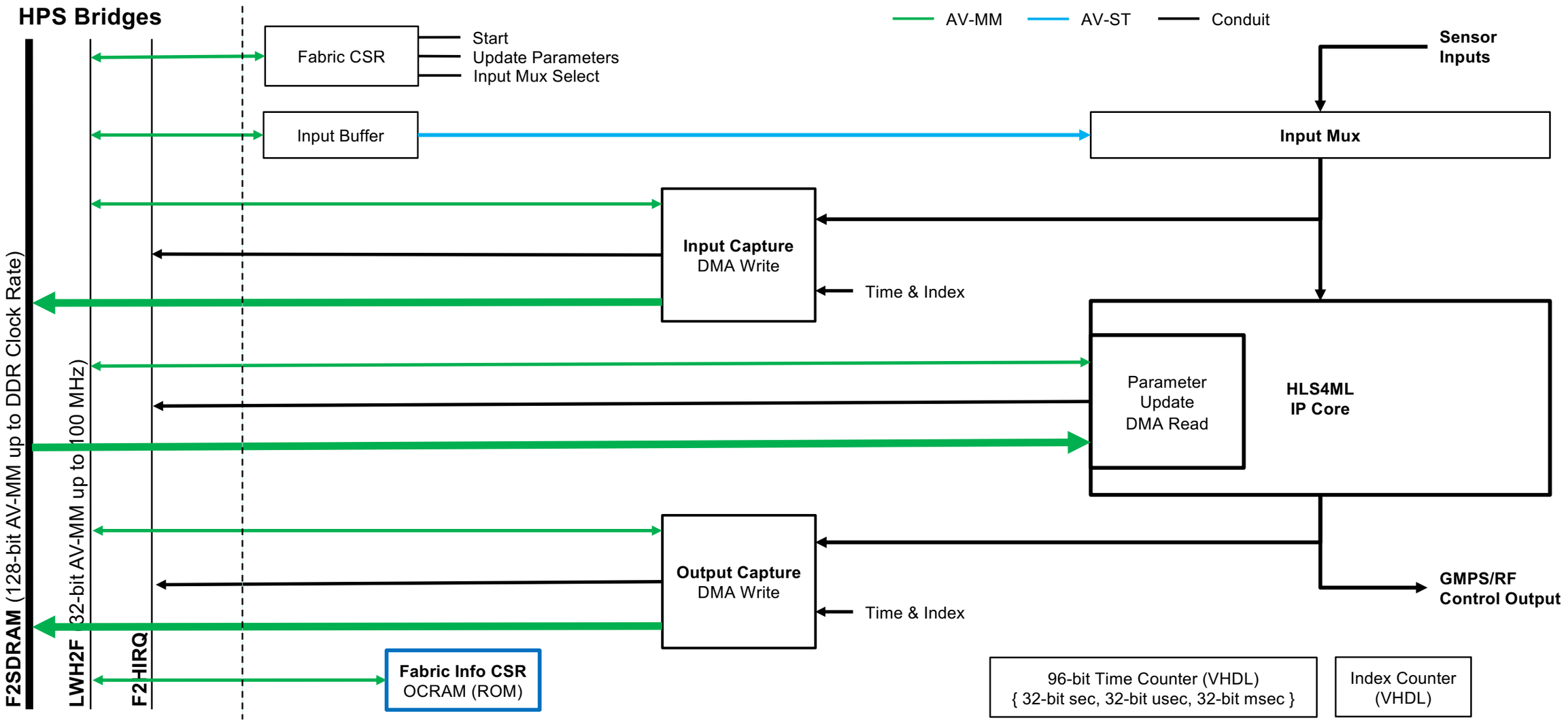
Platform Designer

- Components appear in IP library
- Run “File->Refresh System and Reload All Components” to update the example design
- Or add components to existing design, wire up components following the example project and adjust address map to match address offsets shown here
- CSRs wire to LWH2F HPS bridge
- DMA buses wire to F2SDRAM HPS bridge



Slave	a10_hps.h2f_lw_axi_master
ILC.avalon_slave	
a10_hps.f2h_axi_s...	
a10_hps.f2sdram...	
a10_hps.f2sdram...	
button_pio.s1	
capture_in_compl...	0x0002_0100 - 0x0002_011f
capture_in_dispat...	0x0002_0000 - 0x0002_003f
capture_out_com...	0x0004_0100 - 0x0004_011f
capture_out_disp...	0x0004_0000 - 0x0004_003f
control_register_0...	0x0001_0000 - 0x0001_003f
dipsw_pio.s1	
fabric_info_0.s1	0x0001_0100 - 0x0001_013f
input_buffer_0.avs...	0x0005_0000 - 0x0005_003f
led_pio.s1	
ml_completion_0....	0x0003_0100 - 0x0003_011f
ml_dispatcher_0.a...	0x0003_0000 - 0x0003_003f
ocm_0.s1	
pb_lwh2f.s0	0x0000_0000 - 0x0000_01ff
sys_id.control_slave	
ILC.avalon_slave vi...	0x0000_0100 - 0x0000_01ff
sys_id.control_sla...	0x0000_0000 - 0x0000_0007
led_pio.s1 via pb_l...	0x0000_0010 - 0x0000_001f
button_pio.s1 via ...	0x0000_0020 - 0x0000_002f
dipsw_pio.s1 via p...	0x0000_0030 - 0x0000_003f

Hardware Design Components



Software

- Driver source code and device tree binding provided by Crossfield to build into embedded Linux kernel and DTB images
- The Linux device driver handles FPGA component controls and DMA operations for user applications
- Example application software source also provided to:
  - Update parameters in the HLS4ML component
  - Get info about the HLS4ML component running in the fabric
  - Capture Input to and Output from HLS4ml component
  - Write inputs to HLS4ML component
- In the process of integrating capability with EPICS

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QUESTIONS?