RD53B ITkPixV1.1

Data Merging Tests with BDAQ53

Mechanical Trombone phase shifts between the clock of the sampler of the primary chip and the received frames of the secondary
SETUP

- Secondary chip frames are emulated by the FPGA
- ITkPixV1.1 in LDO mode
- Send 50 hit data and 50 service frames
- Mechanical Trombone: Insert controllable delay in the data merging link as well as in the control link
- Reinitialize the chip before each test
- The range of the trombone is [0,625ps] so I had to use extra SMA cables to cover a full cycle, 10ps resolution
DATA MERGING LINK
DATA MERGING LINK
CLK FINE DELAY SWEEP

Graph showing the CLK FINE DELAY SWEEP with a line plot and a heatmap.
CONTROL LINK

Trombone delay: Correct frames percentage for CMD link

- 240ps
- 310ps
- 250ps
- 230ps

Percentage of correct frames

Trombone delay (ps)

- 785ps
- 730ps
- 1500ps

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CONCLUSIONS

• Windows of failure every 781.25ps

• ¼ is missing

• Would the windows become wider if we add jitter?

• Would it make sense to test with two SCCs? If yes, does BDAQ53 support driving two SCCs?

• Would it make sense to test without reinitialization?