RD50-MPW3: General details and pixel matrix

Chenfan Zhang*

on behalf of the RD50 CMOS group

*University of Liverpool, Department of Physics

chenfan@hep.ph.liv.ac.uk

UNIVERSITY OF LIVERPOOL

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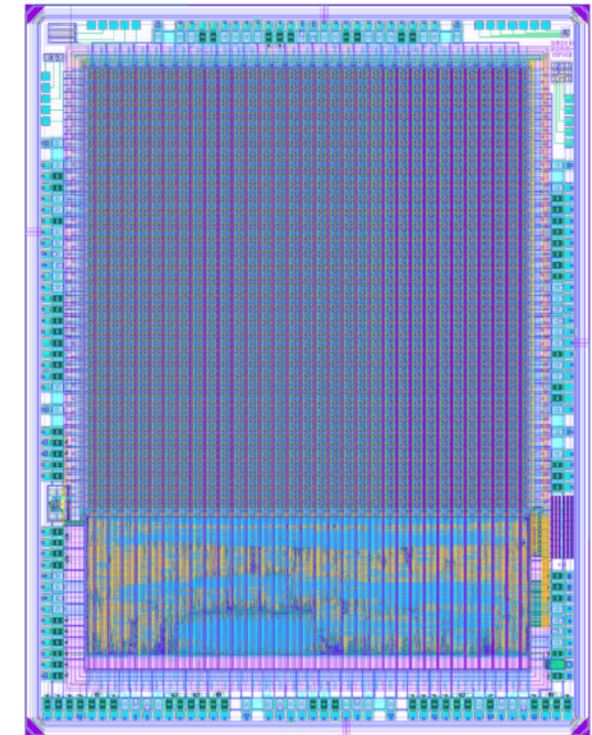
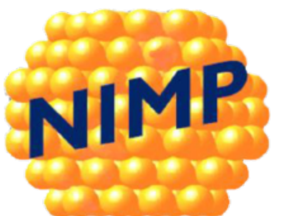
Introduction

- This talk gives general details of **RD50-MPW3** and focuses on the design of its pixel matrix.
- Developed within **CERN-RD50 CMOS Working Group**.
- We make efforts in:
  - ASIC design; TCAD simulations; DAQ development; Chip performance evaluation
- Currently involves 17 institutes:

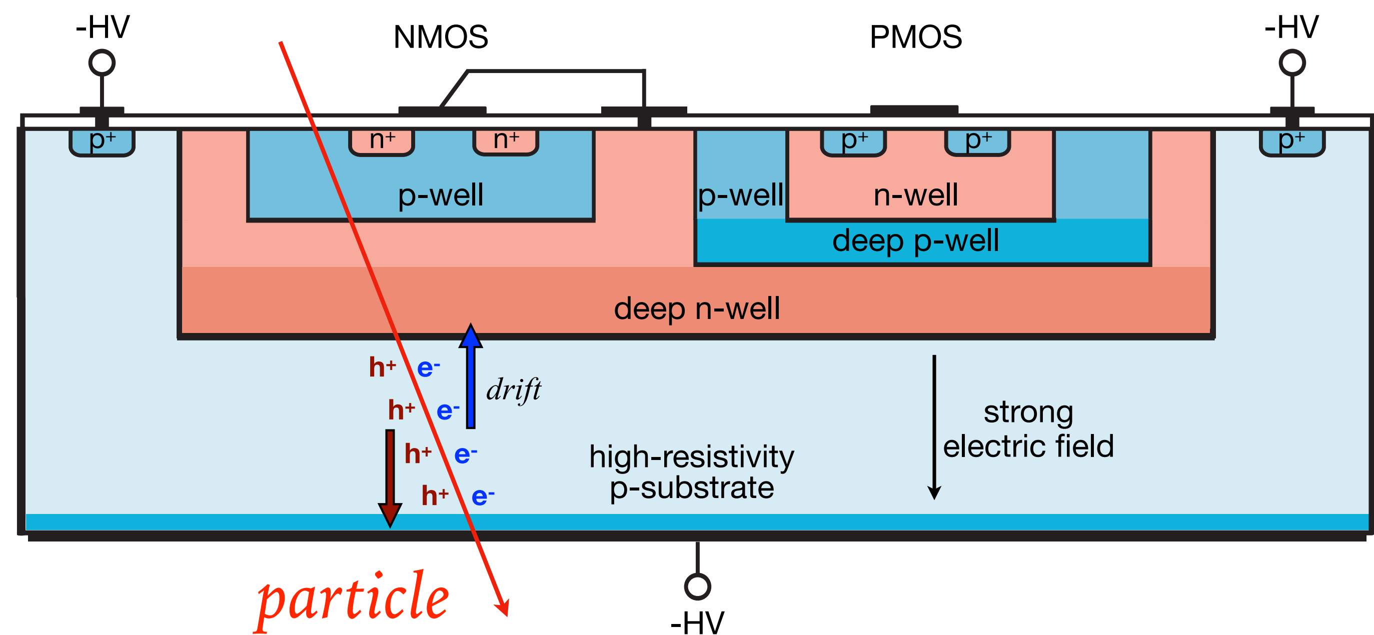


RD50-MPW3



HV-CMOS: Monolithic Pixel Detectors

- Monolithic: Sensor and readout electronics in a single silicon wafer.
  - Single layer structure: **low material thickness** (50 μm);
  - No bump-bonding: **Small pixel size** (< 50 μm × 50 μm); **reduced production cost** (~ £100k/m^2);
  - High bias voltage: **fast charge collection** by drift (~ 200 ps) and **high radiation tolerance** (5×10^{15} 1 MeV n_{eq}/cm^2).

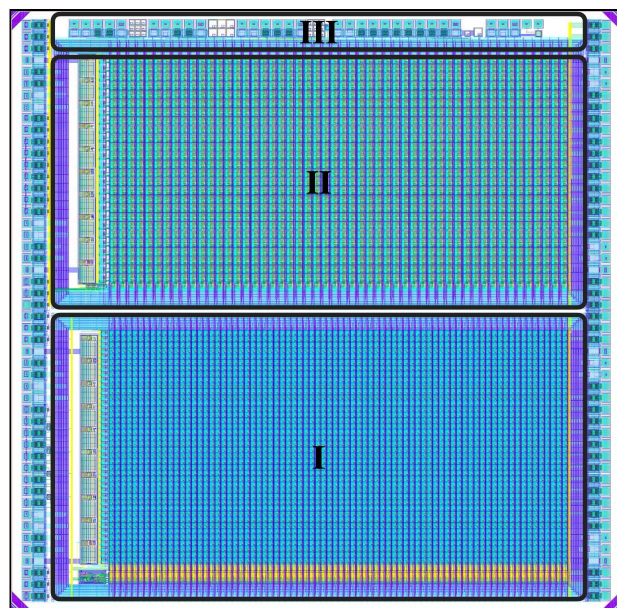


- The Mu3e experiment has chosen HV-CMOS pixel detectors and many others are considering them: LHCb, proton EDM, PANDA.
- We aim to further improve performance of HV-CMOS sensors.

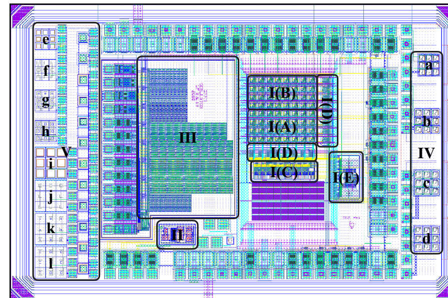
RD50 HV-CMOS Prototype Chips

- Three HV-CMOS prototypes have been designed by RD50 CMOS group.
- Fabricated in LFoundry 150 nm HV-CMOS process.

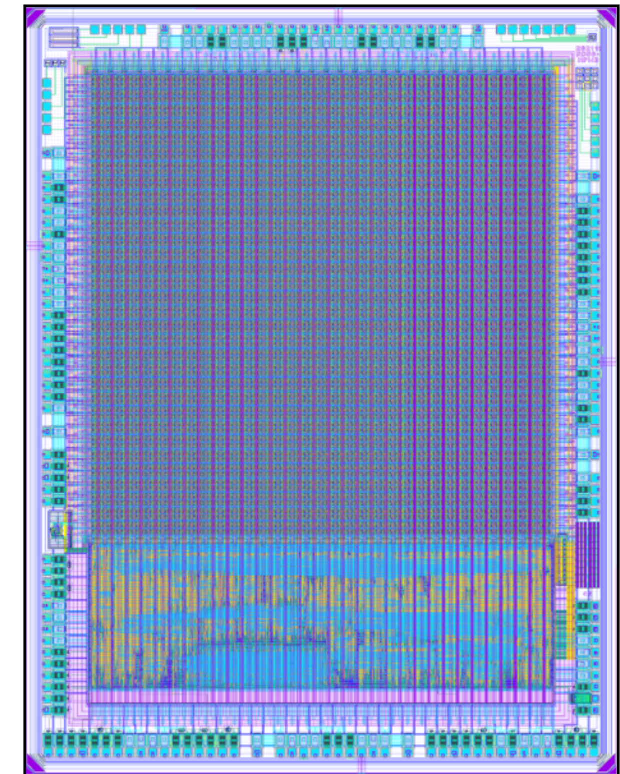
RD50-MPW1
fabricated in Apr. 2018



RD50-MPW2
fabricated in Feb. 2020



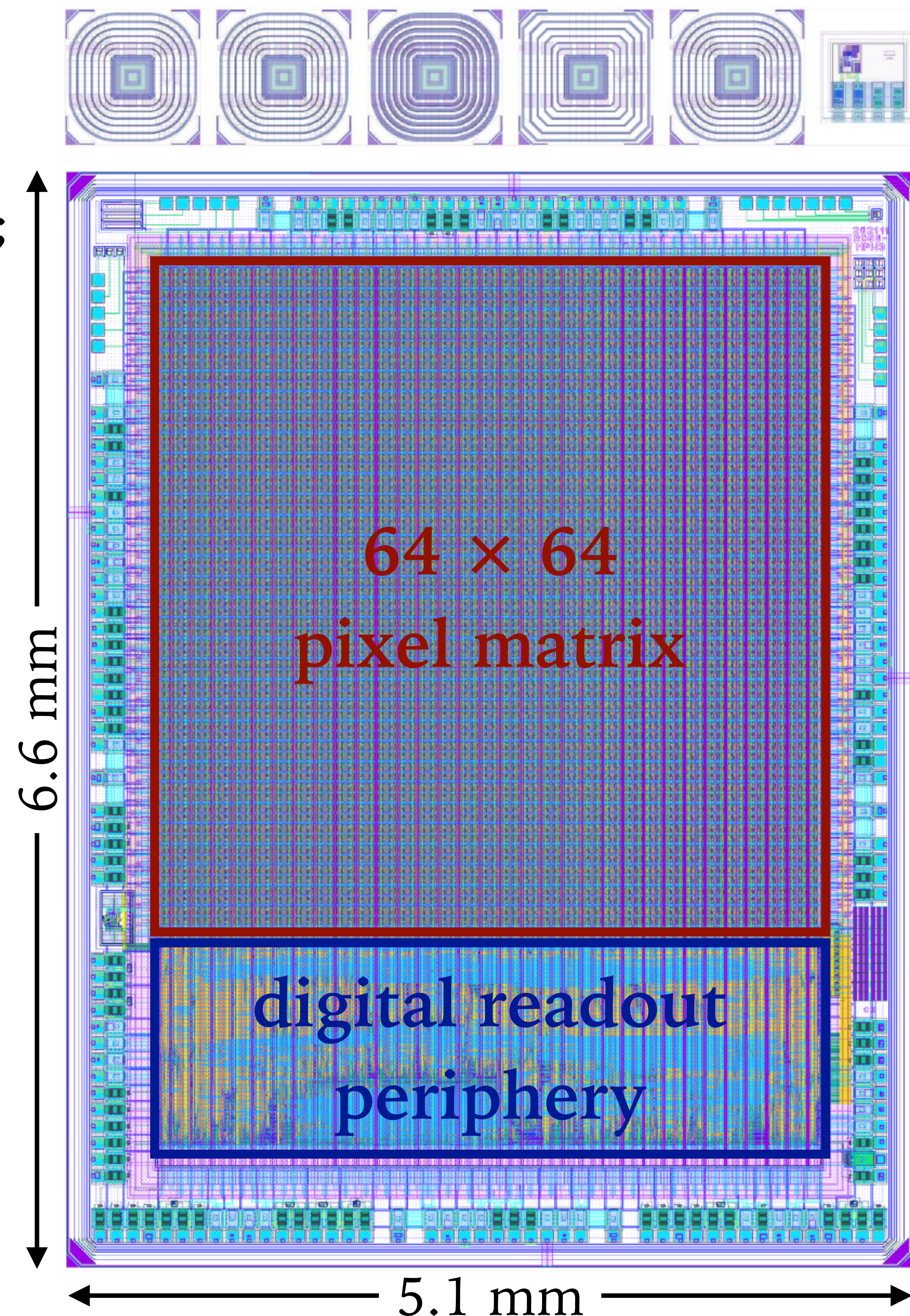
RD50-MPW3
submitted in Dec. 2021



- **RD50-MPW1** - test the LF150 process, low V_{BD} (55 V) and high I_{Leak} ($\sim \mu$A).
- **RD50-MPW2** - high V_{BD} (130 V), low I_{Leak} ($\sim$ nA) and fast analog front-end. Small pixel matrix (8×8), no in-pixel digital readout, no peripheral digital readout: only analog readout.
- **RD50-MPW3** - larger pixel matrix (64×64) with in-pixel digital readout and advanced peripheral readout.

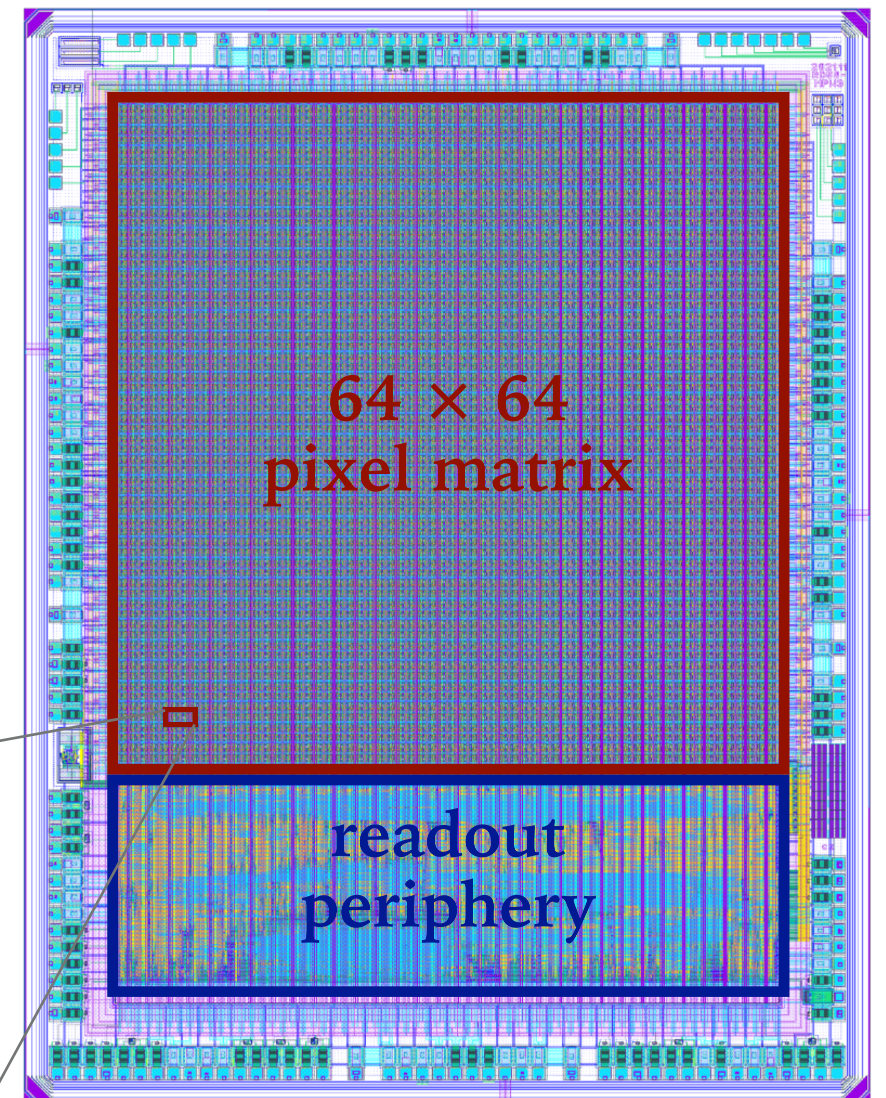
General details of RD50-MPW3

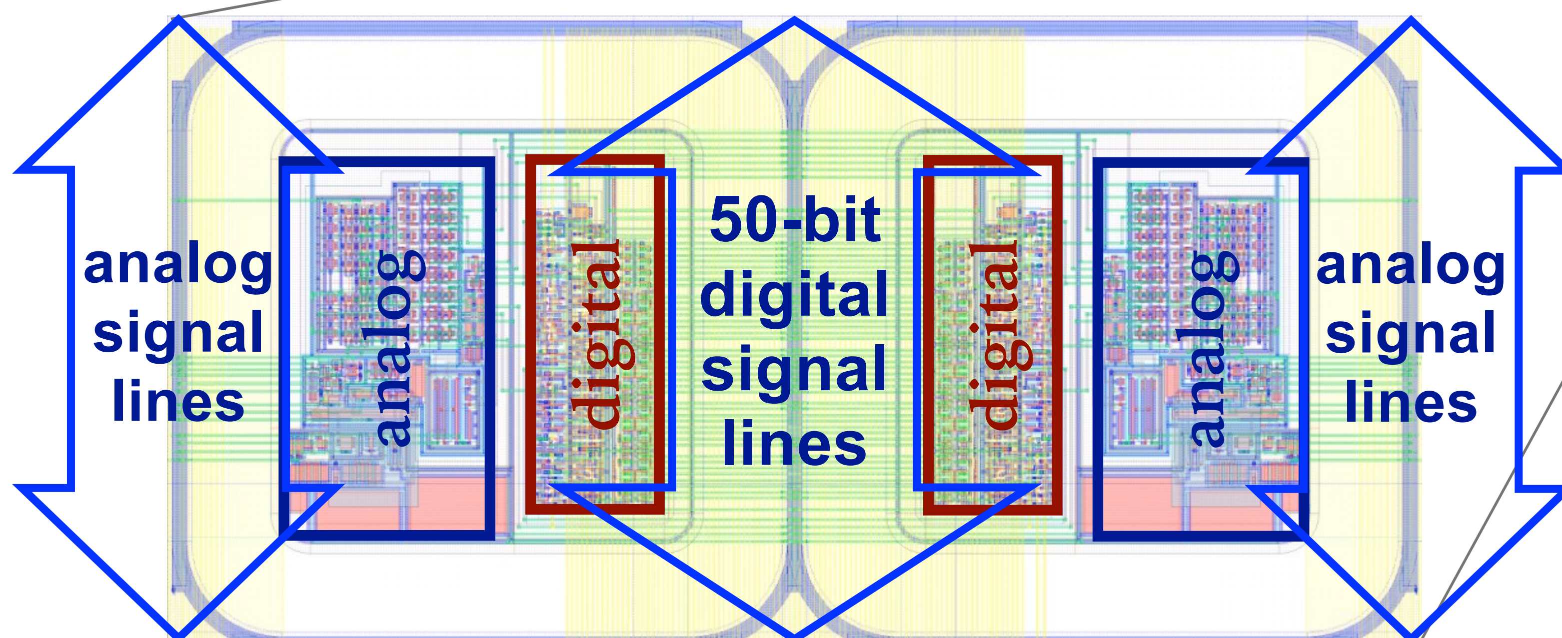
- **RD50-MPW3** is designed based on lessons learnt from the previous two chips and inherits the advantages:
  - ➤ high breakdown voltage; low leakage current; fast analog front-end.
- New features in RD50-MPW3 include:
  - ➤ double-column architecture;
  - ➤ FE-I3 style in-pixel digital readout circuits;
  - ➤ optimised digital periphery for effective chip configuration and fast data transmission.
- Mainly composed of a pixel matrix, a digital readout periphery and test structures.
- Final chip assembly uses Analog-on-Top flow.
- 5 wafers are ordered (1 × 10 Ω·cm, 3 × 1.9 kΩ·cm and 1 × 3 kΩ·cm).
- **RD50-MPW3** was submitted in Dec. 2021, expected in **mid-Jul. 2022**.



Pixel Matrix

- 64 columns are organised into 32 double columns.
- To save area and avoid crosstalk between digital and analog signals:
  - ➤ 50 Digital signal lines are placed in the middle of each double column;
  - ➤ Analog lines are placed between double columns;
  - ➤ Shielding lines (grounded) are inserted between digital signal lines to minimise coupling.
- A power grid using Metal 5 and Metal 6 is used to minimise IR voltage drop.

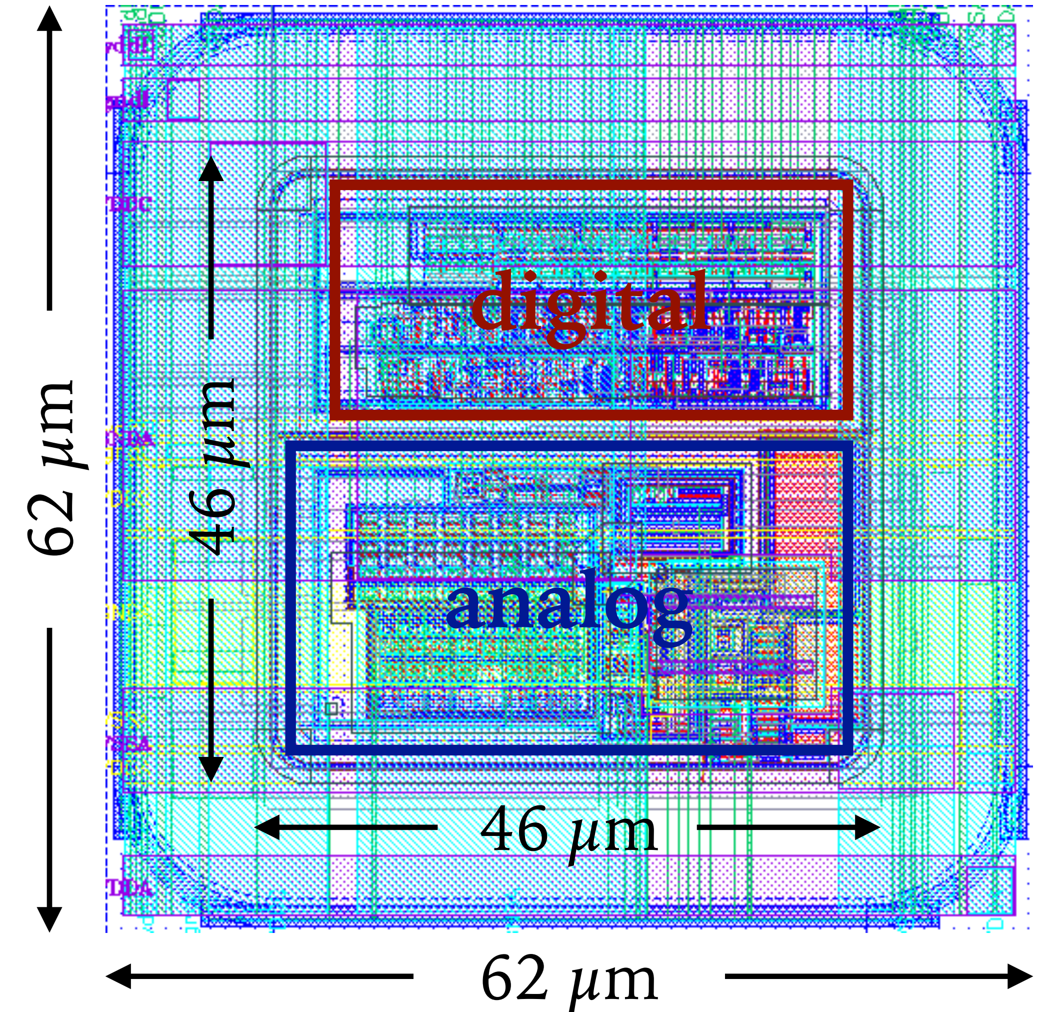


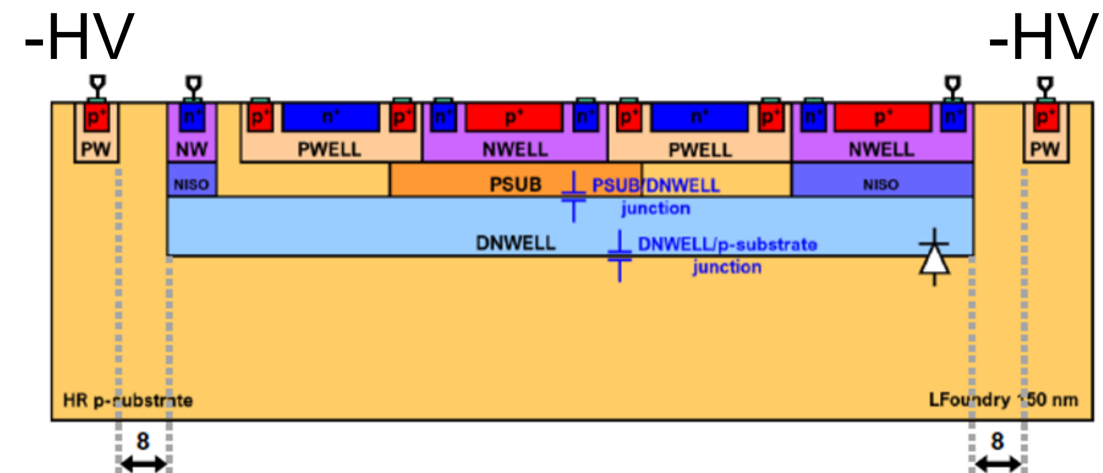


- Each double column is controlled based on the column-drain architecture.

Pixel

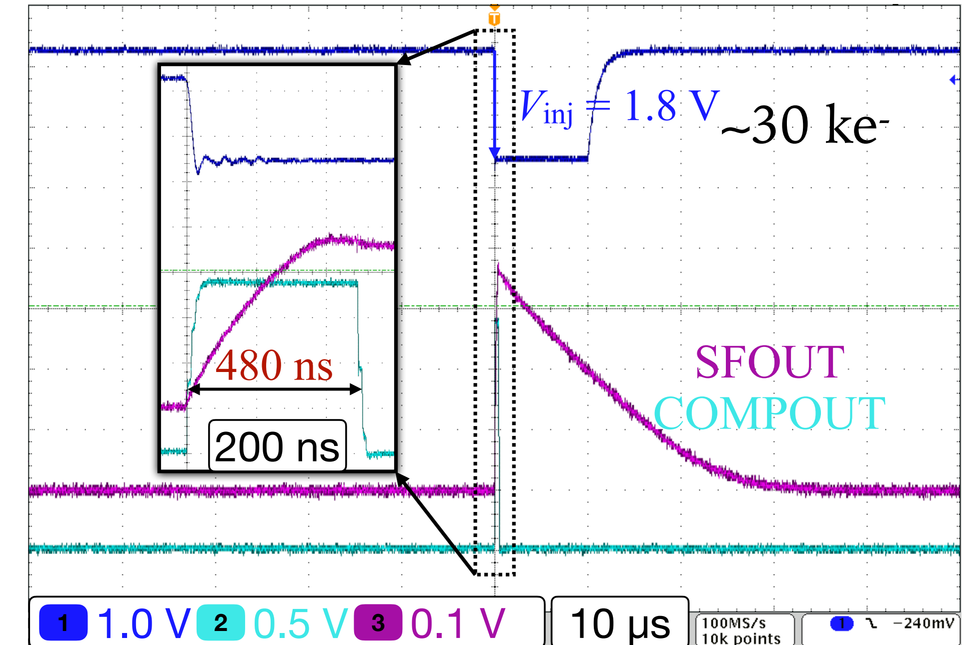
- Large fill-factor pixel.
- High voltage applied from top side.
- Both analog and digital electronics are included inside the collection electrode (55% pixel area).
- Analog and digital circuits are placed into separate deep p-wells and have different power lines to minimise crosstalk noise.
- Analog circuits amplifies the collected charge signal.
- Digital circuits monitor the comparator output signal from the analog part.



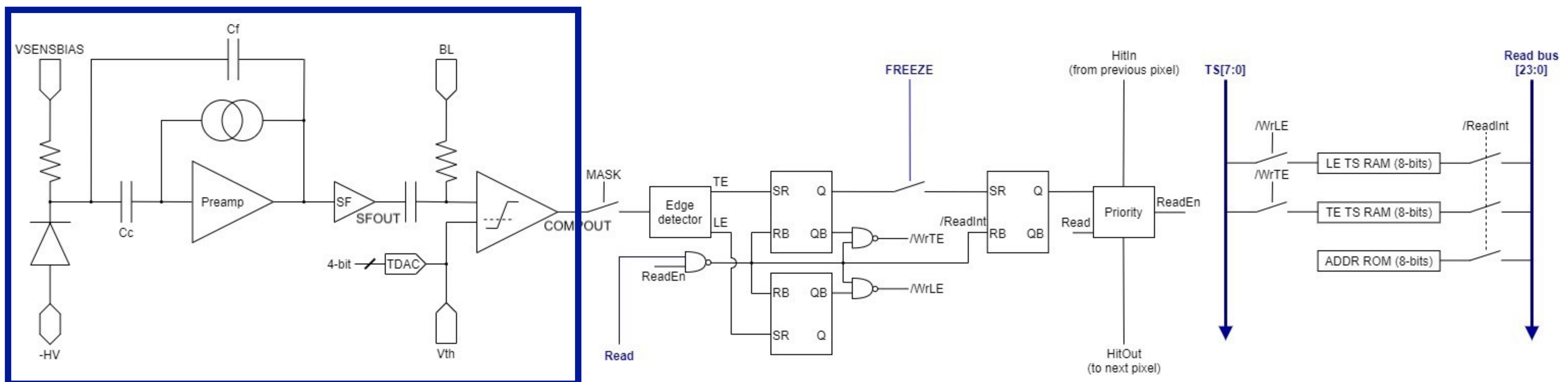


Pixel: Analog Front-end

- Analog front-end is from RD50-MPW2 pixels.
- Continuous-reset CSA has been tested and proven to have high processing speed.
- Each pixel has a comparator to digitise its analog signal.
- A 4-bit trim-DAC inside each pixel tunes comparator threshold.
- Injection circuit is included to characterise pixel performance.

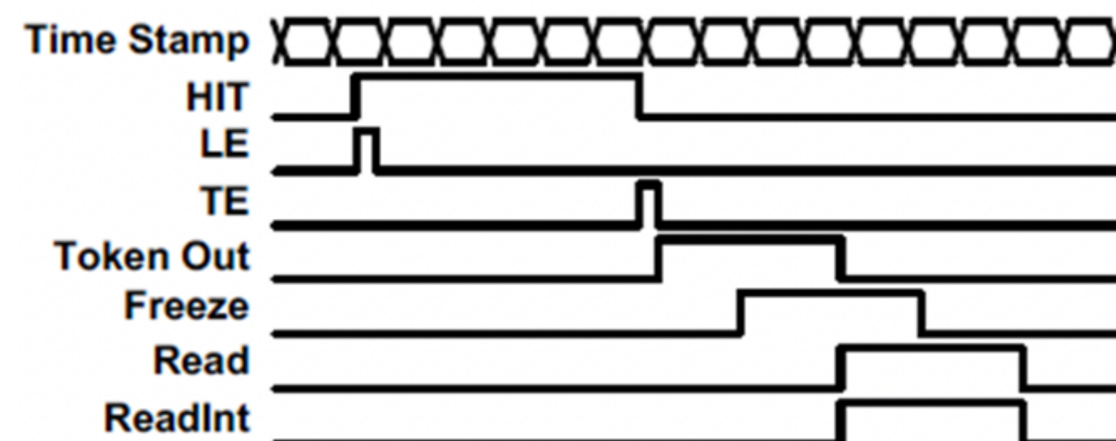


Analog output of RD50-MPW2

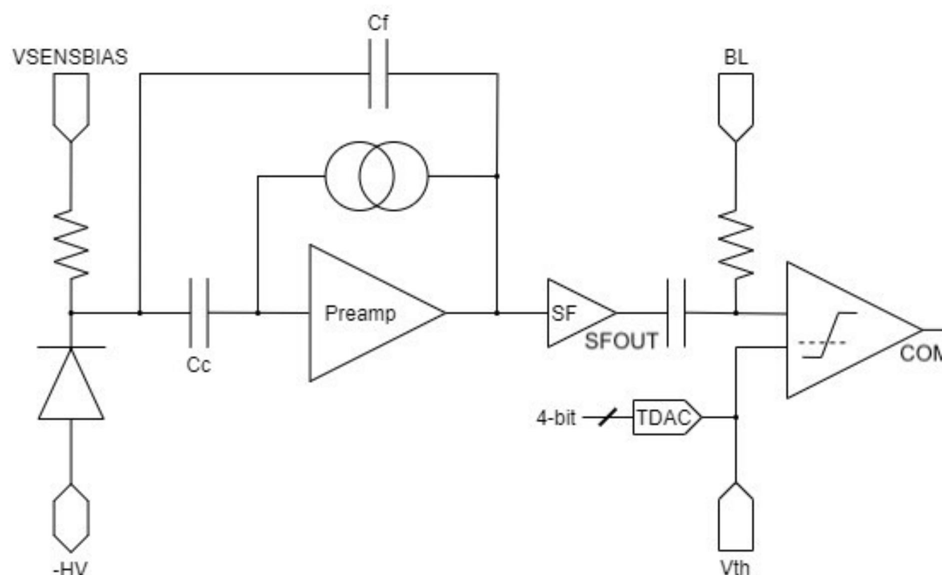


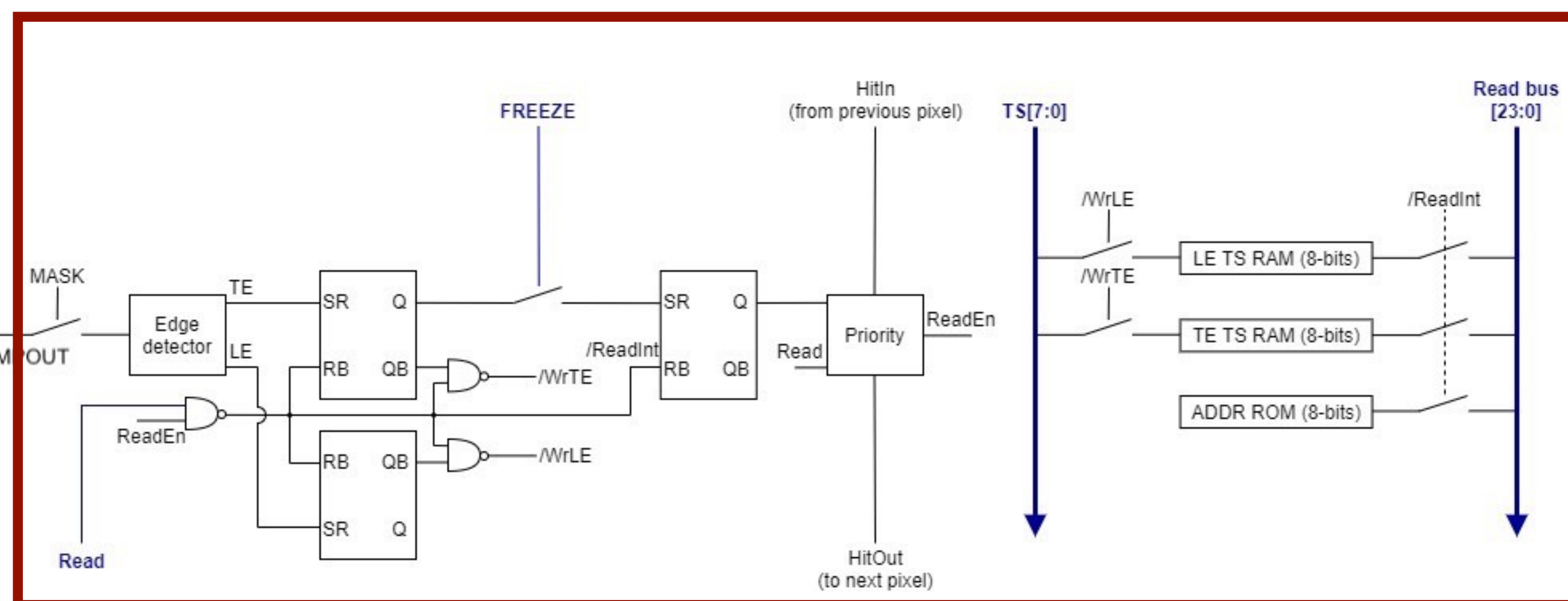
Pixel: Digital Readout

- in-pixel Digital readout is based on column drain architecture.
- An 8-bit time stamp (40 MHz) is sent to all pixels.
- Time stamps of the rising and trailing edges of the comparator output are recorded to measure Time of Arrival **(ToA)** and Time over Threshold **(ToT)**.
- These two time stamps are stored in two 8-bit RAMs, which are sent out together with an 8-bit pixel address via a shared readout bus.
- Full custom design to minimise area.



digital





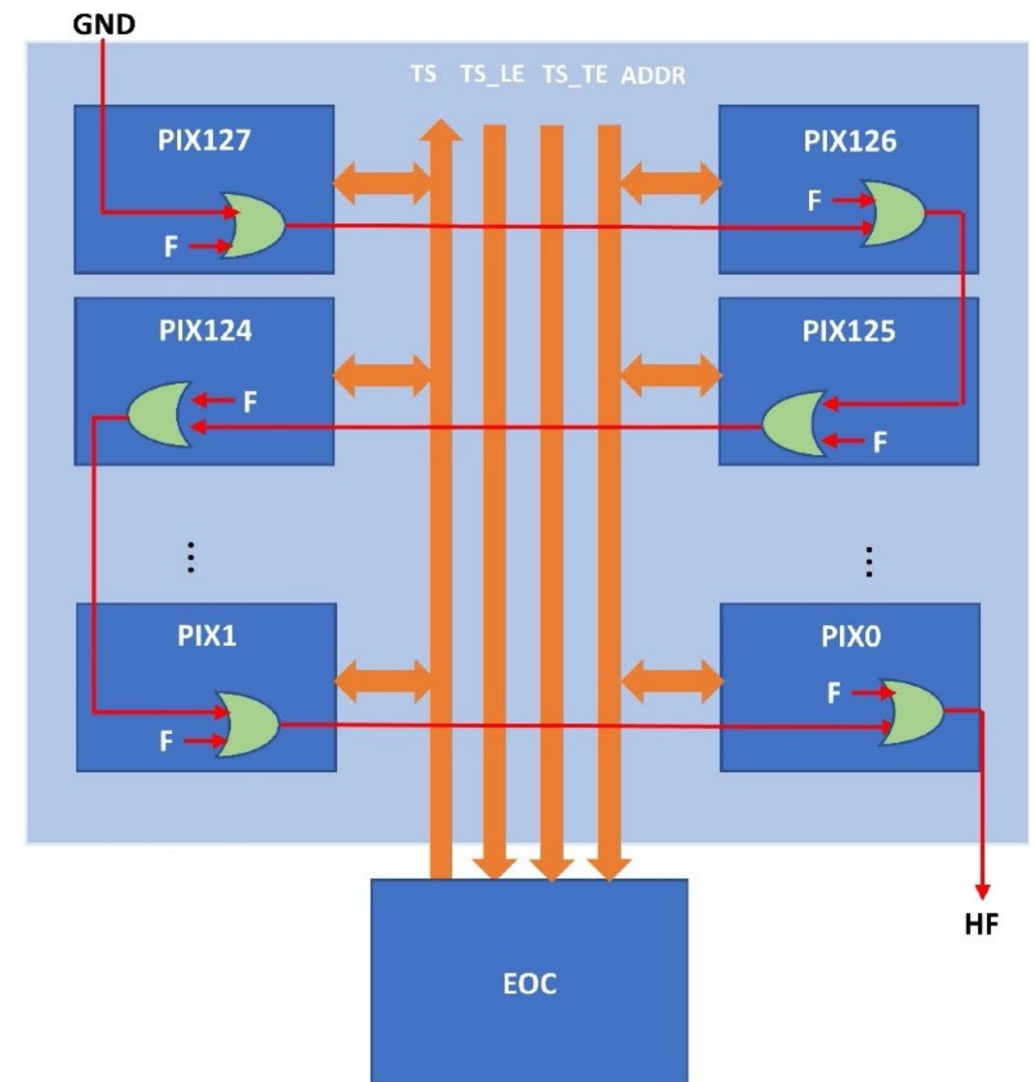
Pixel Parameters

- Pixel parameters according to simulation.

Pixel size	62 μm × 62 μm
Cd	~ 250 fF
Power	22 μW/pixel (VDD = 1.8 V)
Gain	230 mV (for 5 ke^-)
ToT	55 ns (for 5 ke^-)
ENC	120 e^-
Time walk	9 ns

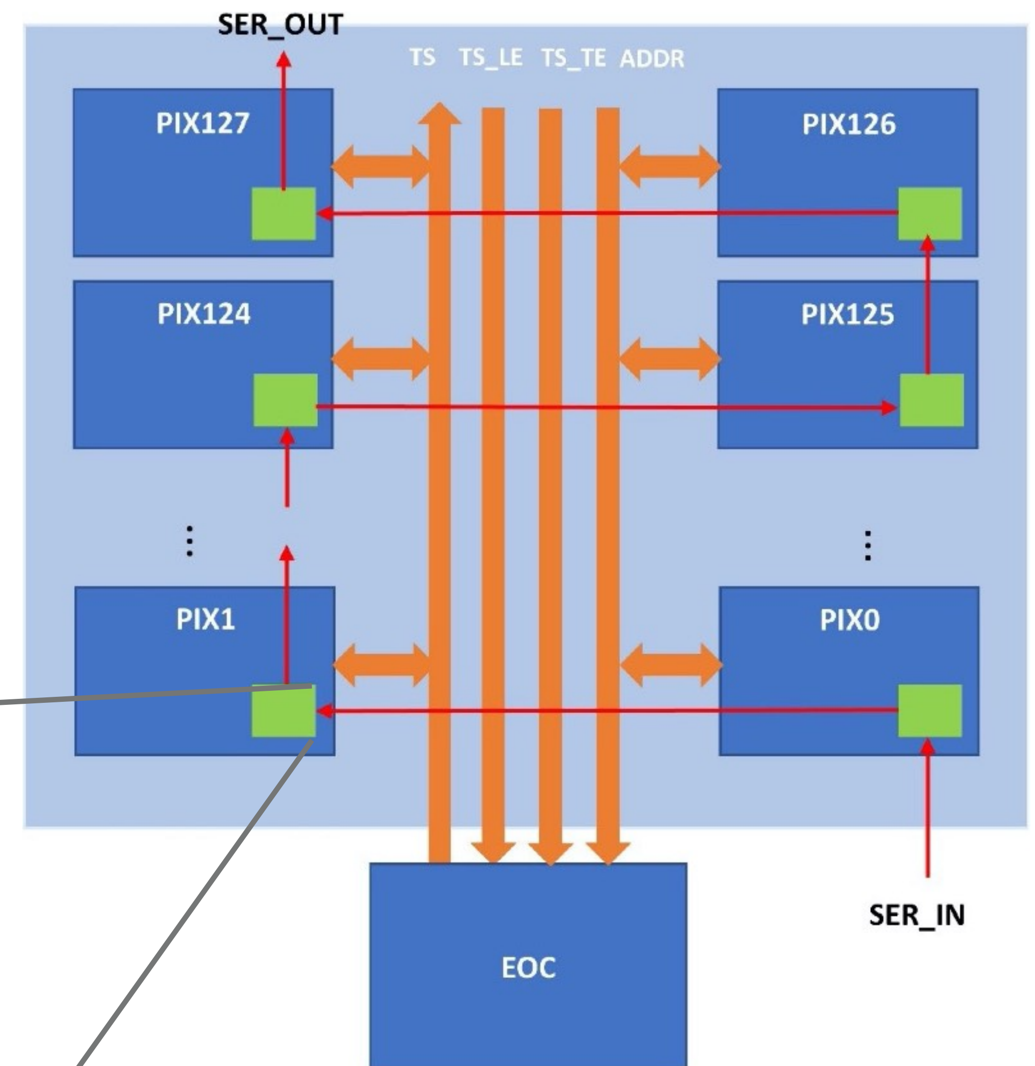
Readout Process

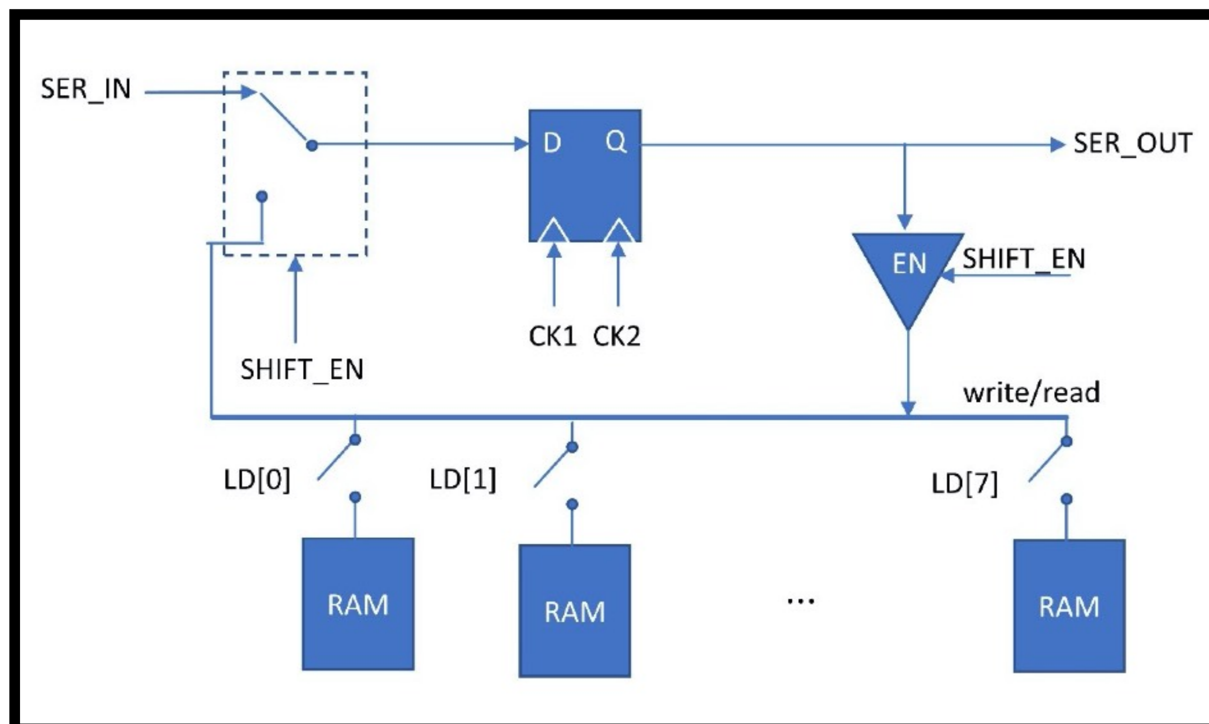
- Readout process is controlled by a chain of Priority Blocks within each double column.
- Each pixel has a Hit Flag (F) to indicate particle detection.
- A chain of OR gates passes the Hit Flag status down to an End-of-Column (EOC) block.
- The pixel that has asserted its Hit Flag and with the highest address has the priority to access the readout data bus.
- EOC collects the hit data (time stamps and pixel address) and sends them to the periphery where the data are packaged and transmitted out in serial (640 Mbps).



In-pixel Configuration Registers

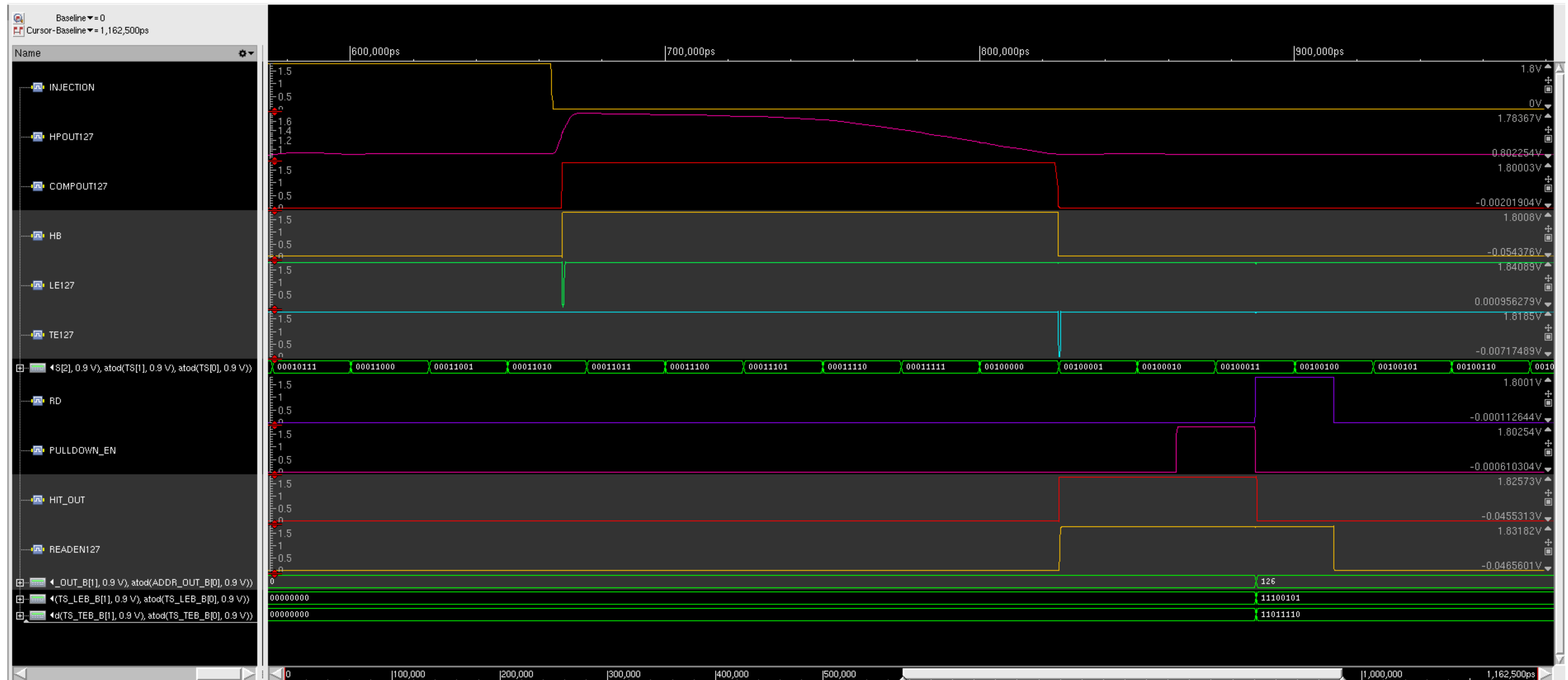
- Each pixel has an 8-bit configuration register.
- All registers inside a double column are serially connected.
- Configuration bits are shifted-in to set each pixel individually (4-bit trim-DAC setting, masking noisy pixel, injection enabling and analog outputs(SFOUT and HB) enabling).
- The data shifted in can be read back for verification.





Verification

- Mixed-mode simulations were made on single pixel and one double-column.



Summary

- **RD50-MPW3** inherits the advantages from RD50-MPW2, and has improvements of having a **larger pixel matrix** with **in-pixel digital readout** and **advanced peripheral readout**.
- It will be delivered in **mid July 2022**.
- Beam test at CERN has been planned in October 2022
- This talk focuses on the design of its pixel matrix. The design of the digital readout periphery and of the electronics beyond the chip will be presented in the following talk by Patrick.