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RD50-MPW3: General details and pixel matrix

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The CMOS Working Group of CERN-RD50 has designed and submitted RD50-MPW3, which is the third High Voltage CMOS (HV-CMOS) pixel chip developed by the collaboration to further study these sensors for future physics experiments. The design of RD50-MPW3 incorporates the lessons learnt from the previous two chips, RD50-MPW1 and RD50-MPW2. It inherits the structures for high breakdown voltage and low leakage current, the fast analog readout circuits and the well-performing bias block and analog buffer from its two predecessors.

RD50-MPW3 is a more advanced prototype with a matrix of 64 × 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes. To alleviate routing congestion and minimise crosstalk noise, the pixels are serially configured and organised in a double-column architecture. This prototype has optimised digital peripheral readout electronics for effective chip configuration, based on the I2C protocol with internal Wishbone bus, and fast data transmission.

This contribution gives an overview of the general details of RD50-MPW3 and focusses on the design aspects of the pixel matrix. The design of the digital periphery of the chip, and of the electronics beyond the chip, will be presented in a separate contribution to this workshop.

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