DAQ-ROC4Sens Update

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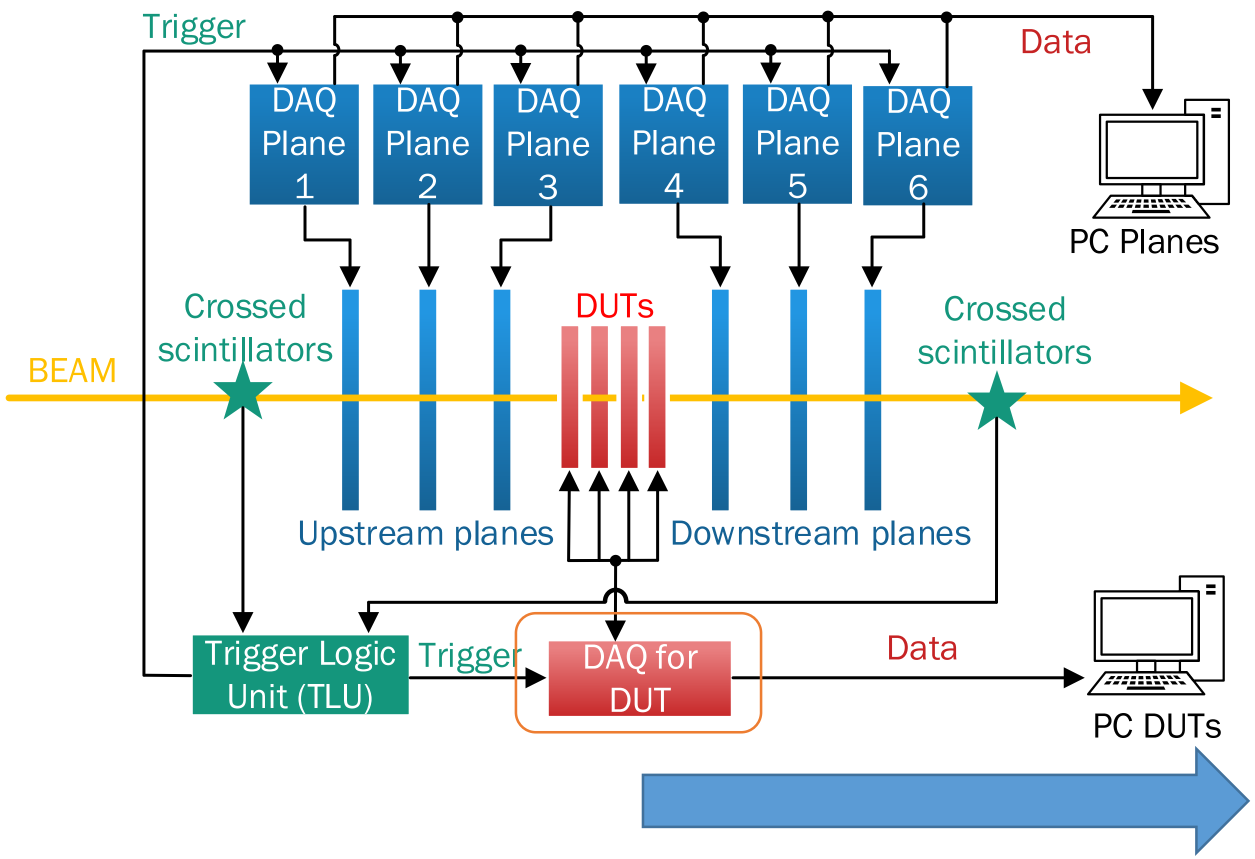
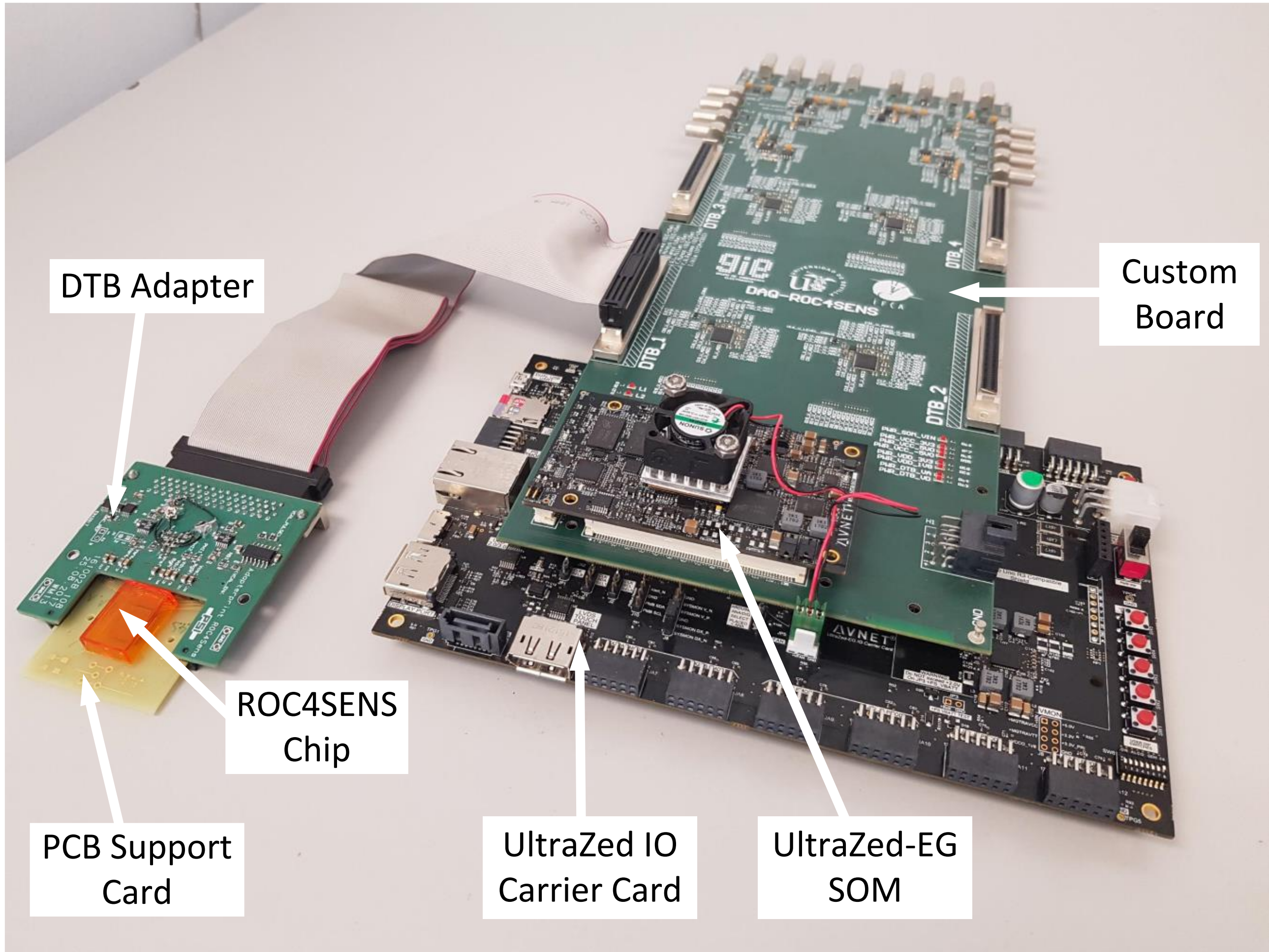
In a Nutshell

- Backend DAQ ROC4Sens
  - System Description
  - Technologies involved
  - FPGA Logical Design
  - Human Interface
  - Custom Hardware
  - State of the Project and prospectives

General Description: A Telescope DAQ





The main idea is to simplify the typical testbeam backend setup (e.g., AIDA2020 telescope) by a <u>standalone device</u> based on a powerful novel hybrid FPGA, which integrates a programmable logic to implement the readout controllers and a set of multicore ARM processors to provide high-level programmability, such as application based on an architecture client-server, high-bandwidth communications, and high processing capability.

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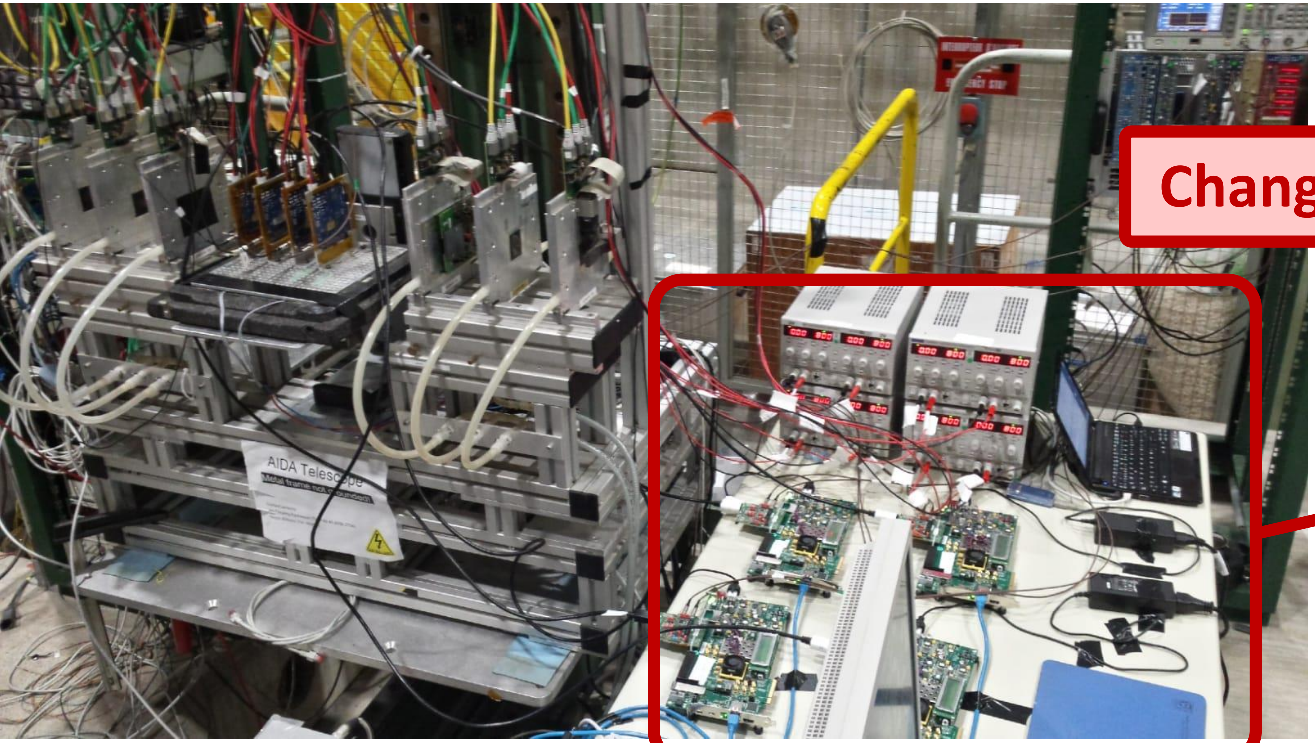

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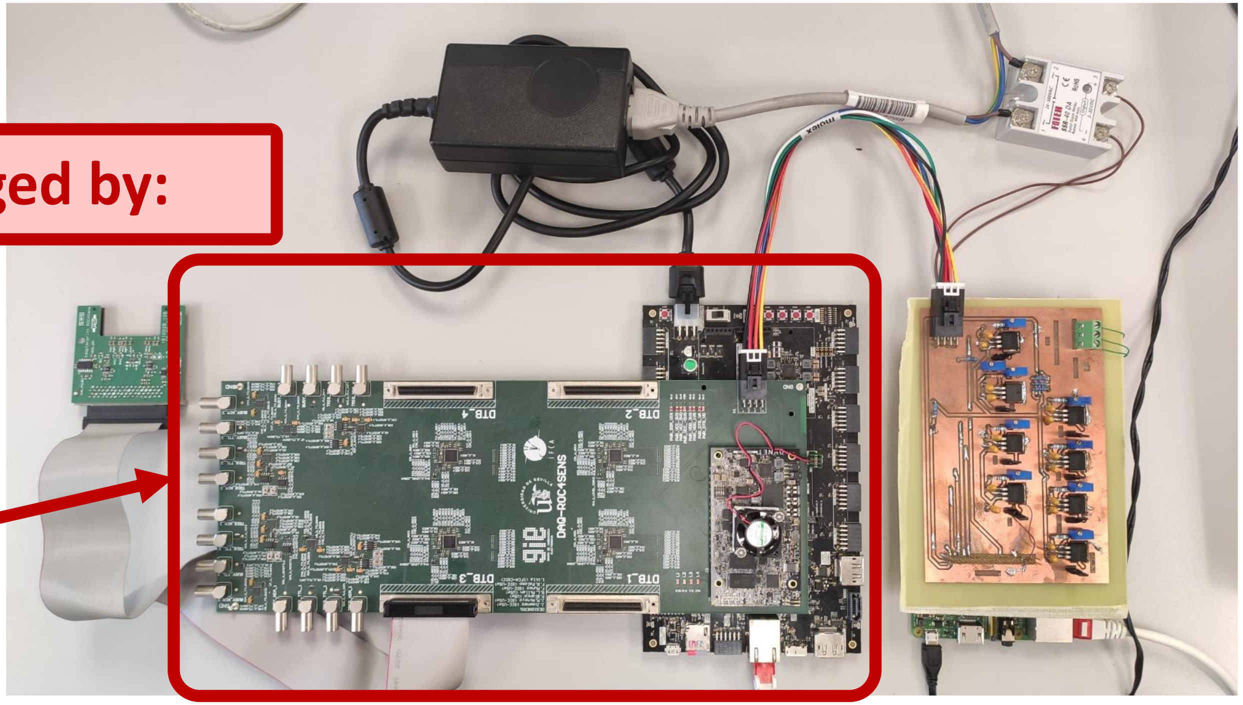

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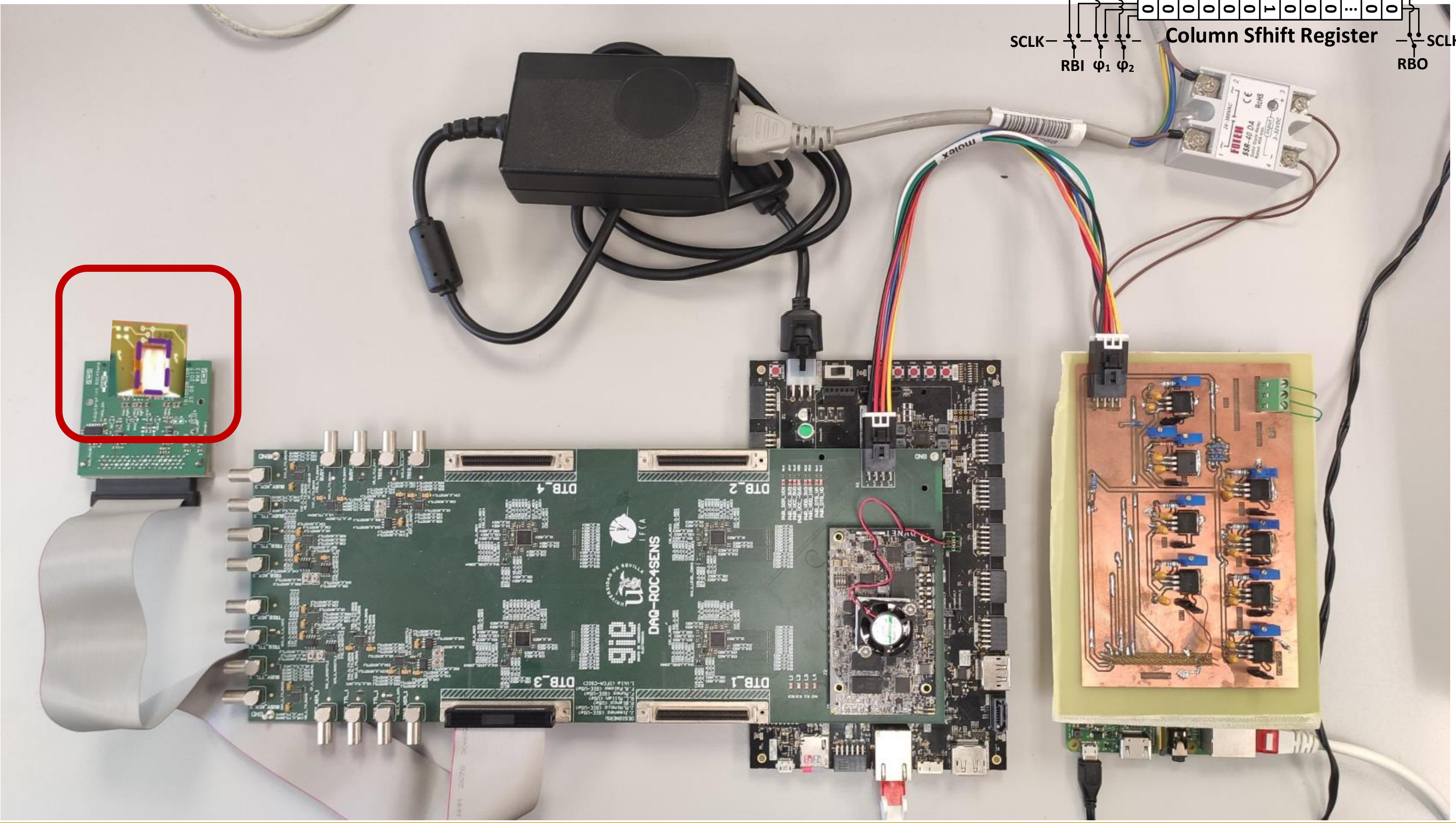
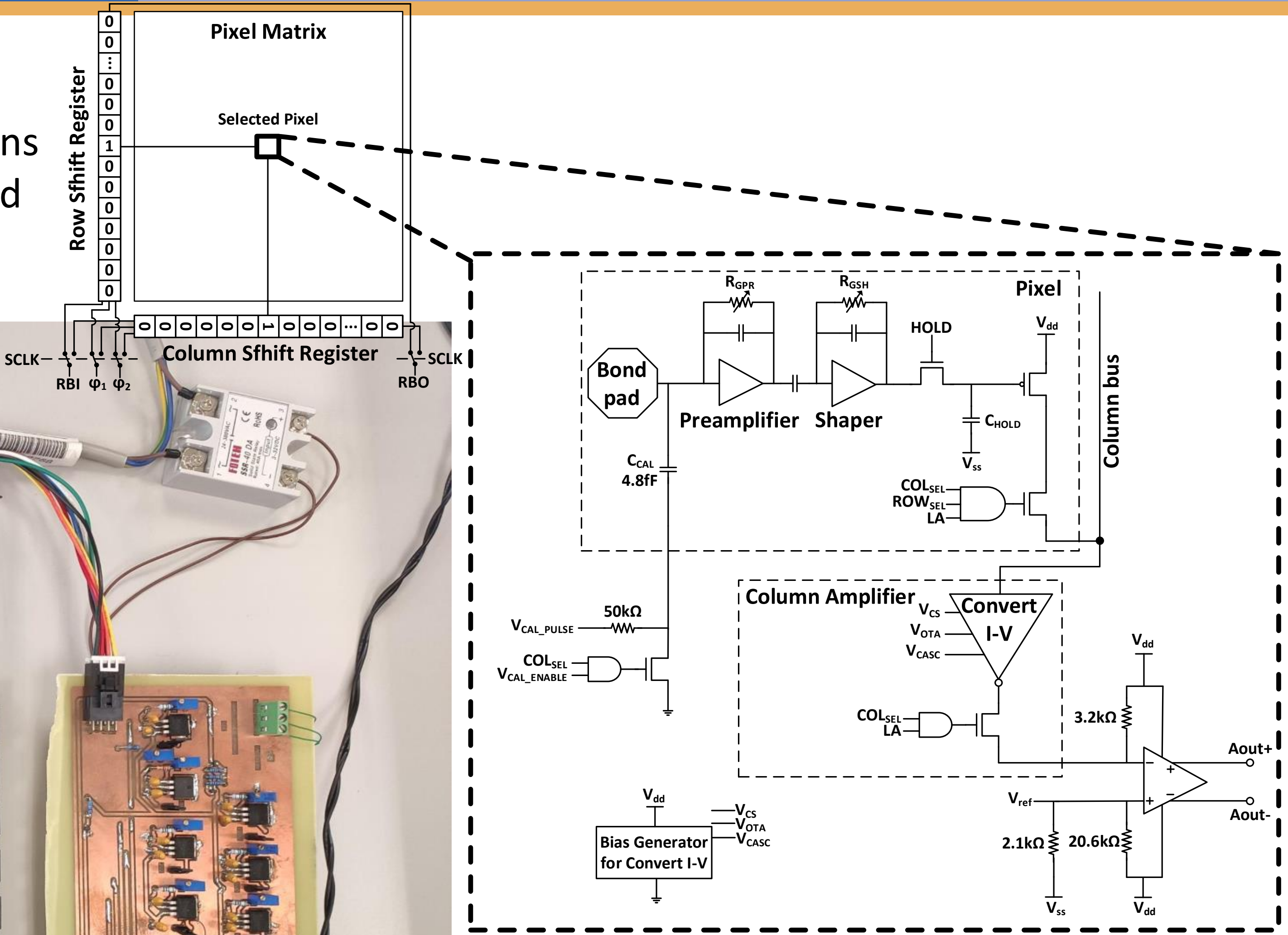
System Description

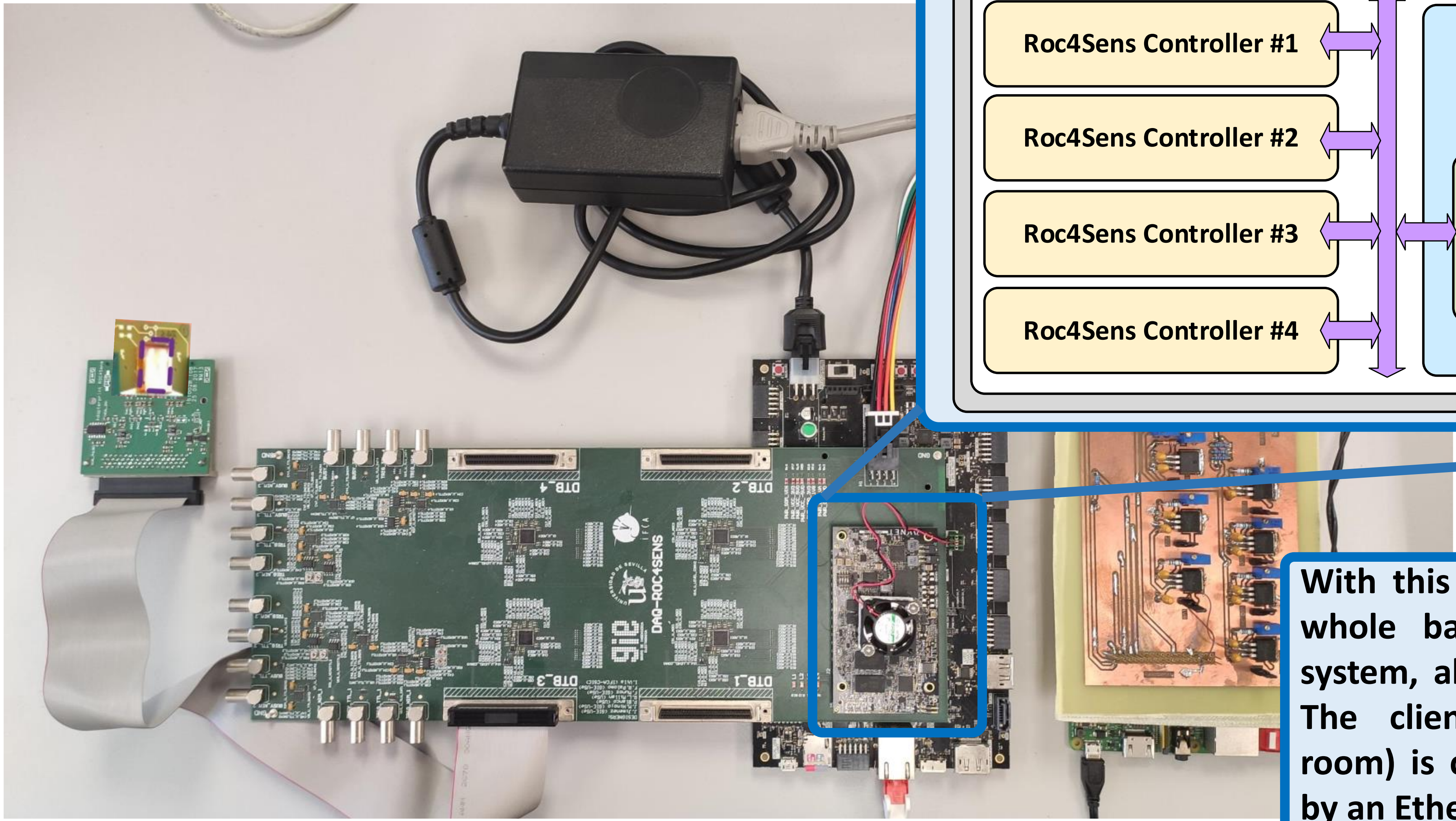
The actual DRAD implementation works with the RoC4Sens readout chip from PSI. It is versatile enough to be adapted to other ROCs.

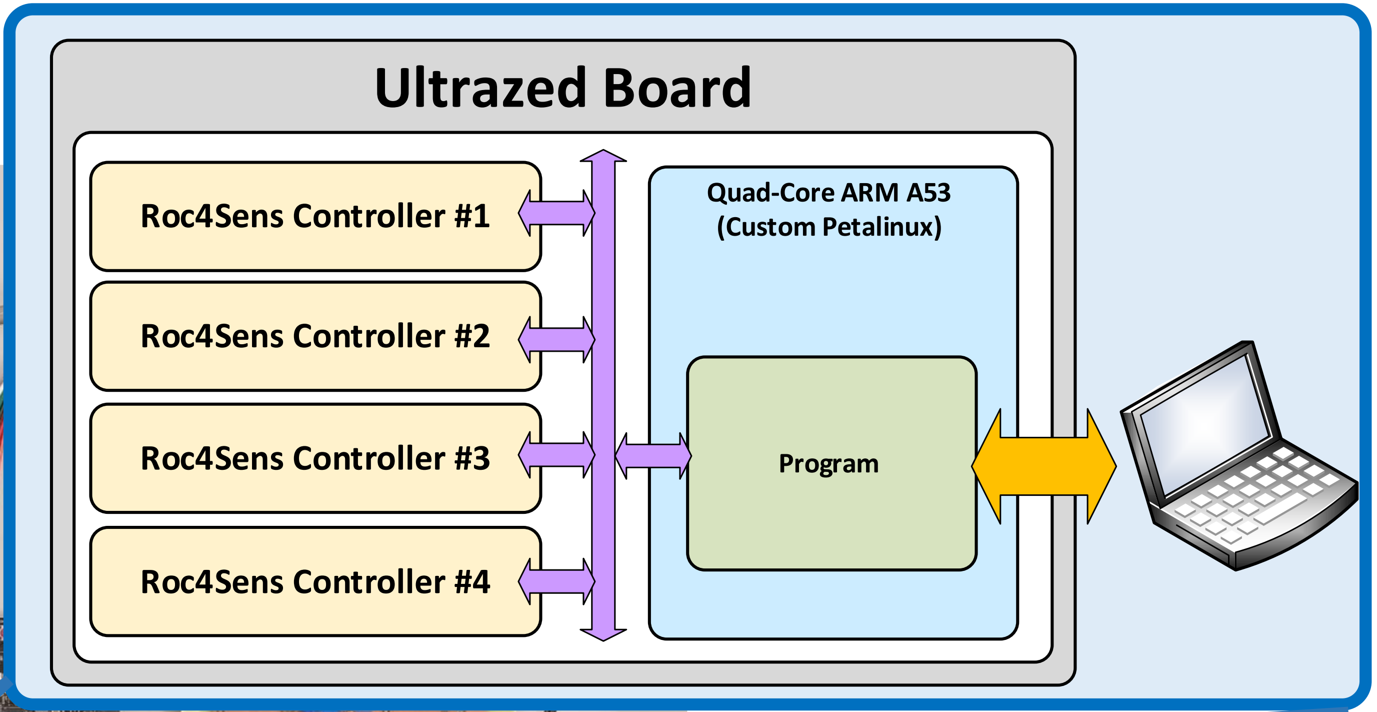




RoC4sens pixel electronics detail.
The RoC4sens is a very simple to control design, with fully analog pixel output.

System Description

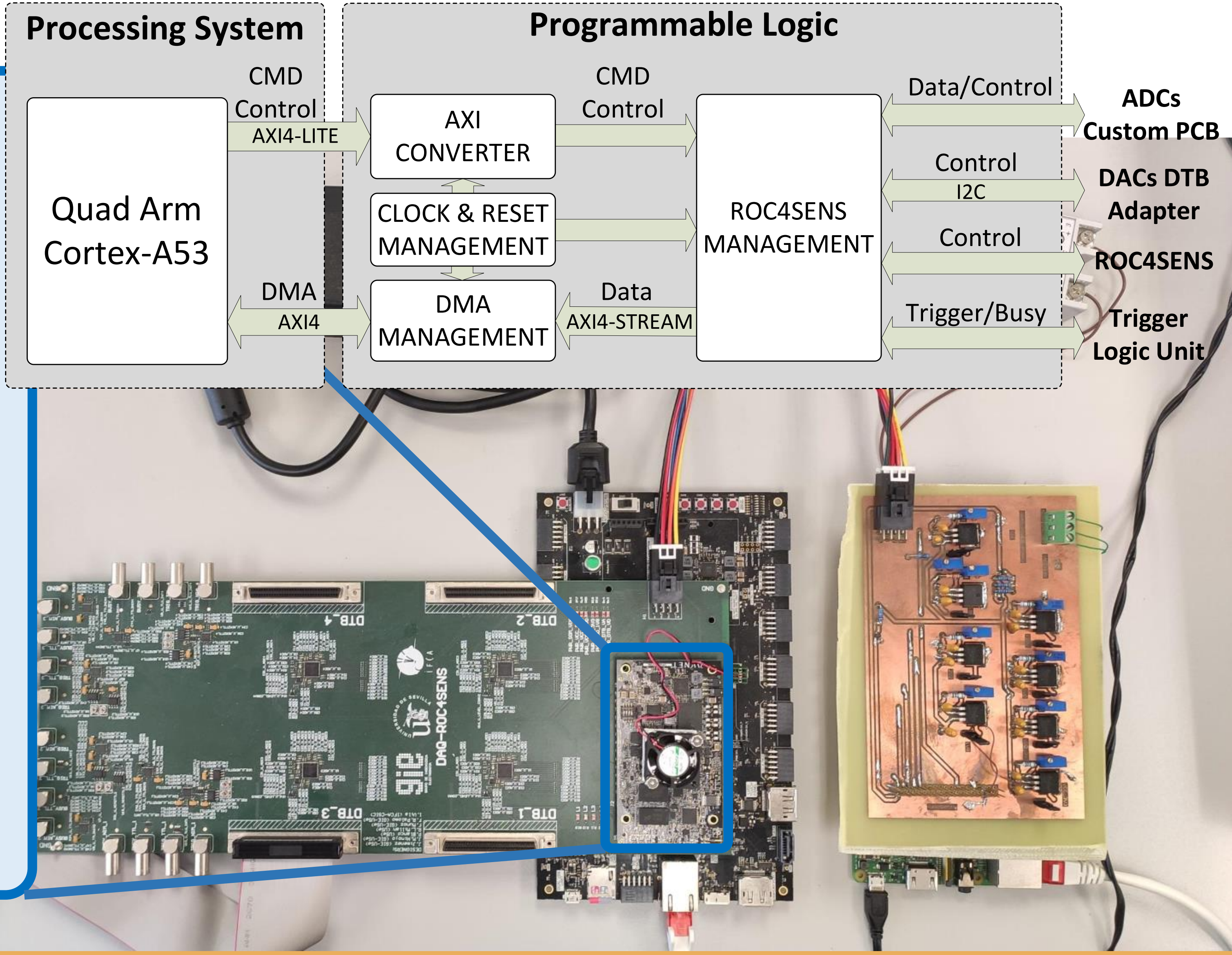




With this computing power at hand the whole backend collapses to only one system, able to manage a full testbeam. The client remote computer (control room) is connected to the DAQ backend by an Ethernet cable.

System Description

- **Hybrid FPGA (Zynq Ultrascale SoC)**
  - **Programmable System (Zynq)**
  - **Processing System**
    - **1 ARM A53 quad core (1.5GHz)**
    - **1 ARM R5 dual core (600 MHz)**
- **AXI internal fast bus for connection between programmable logic and microprocessors**
- **Shared memory for communications between cores**
- **ARM R5 for fast microprocessor tasks (no operating system, tipically proxy patterns)**
- **ARM A53 quad core able to run a custom Petalinux**



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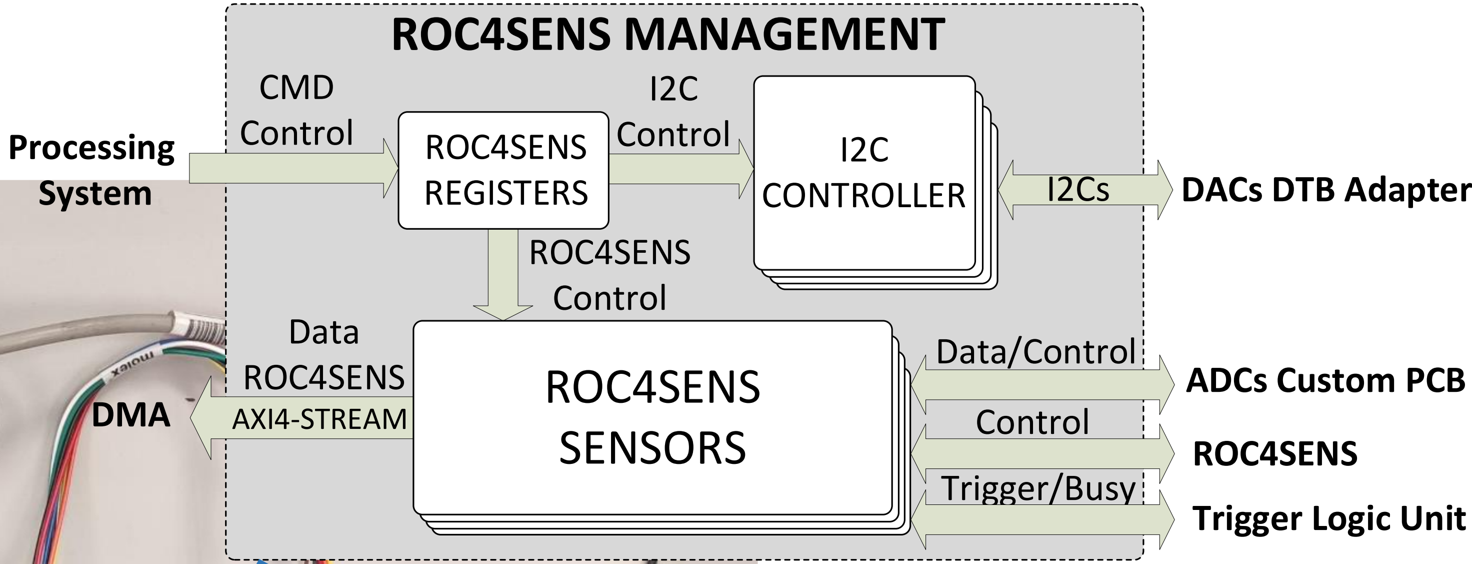
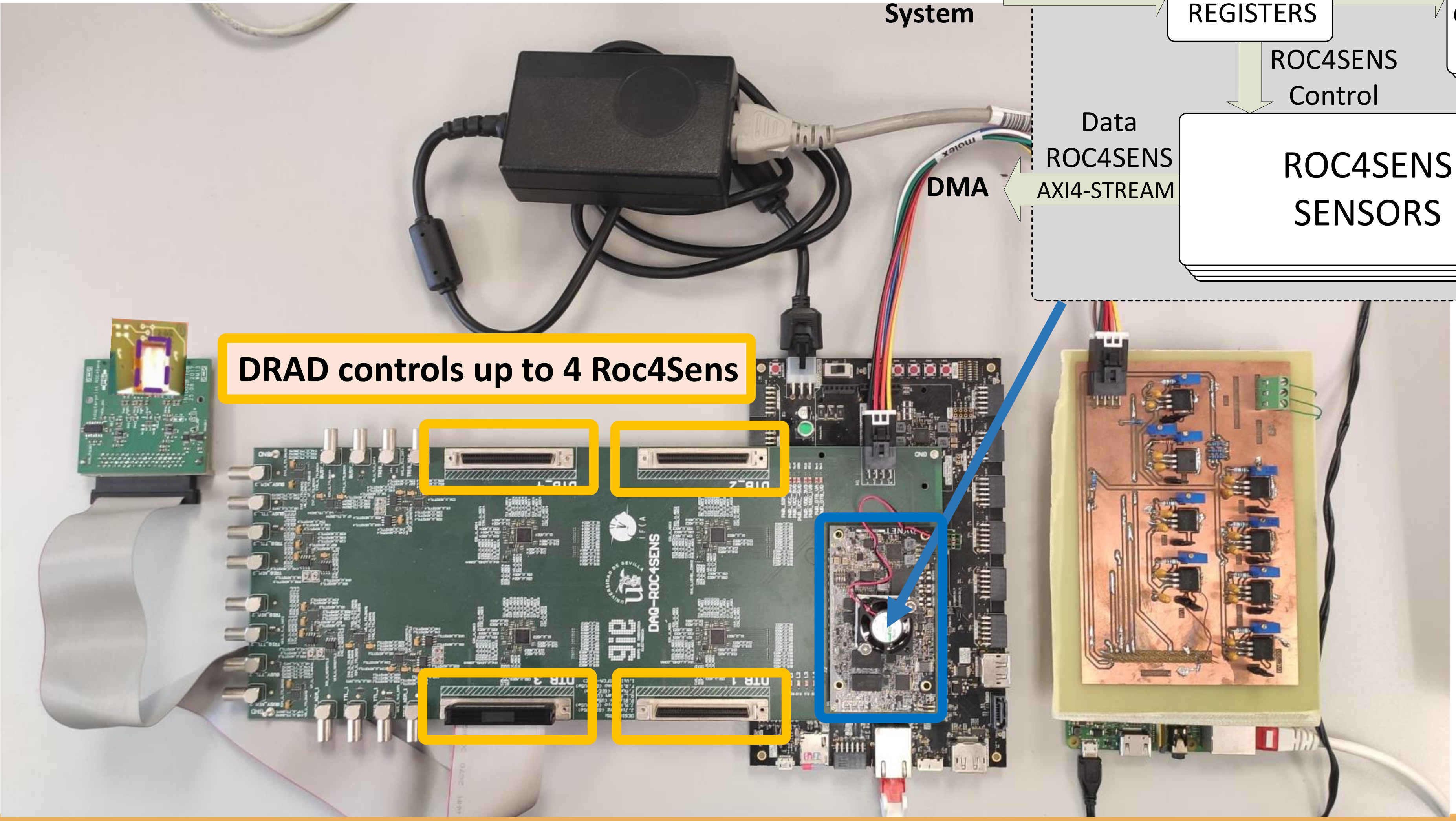
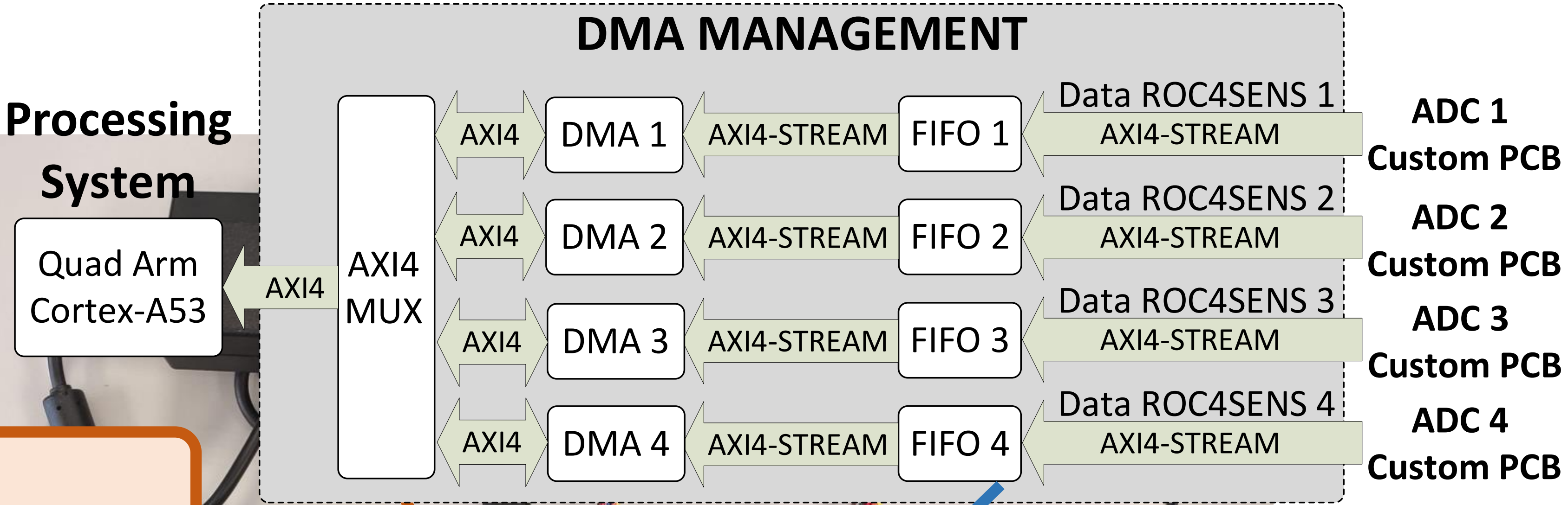
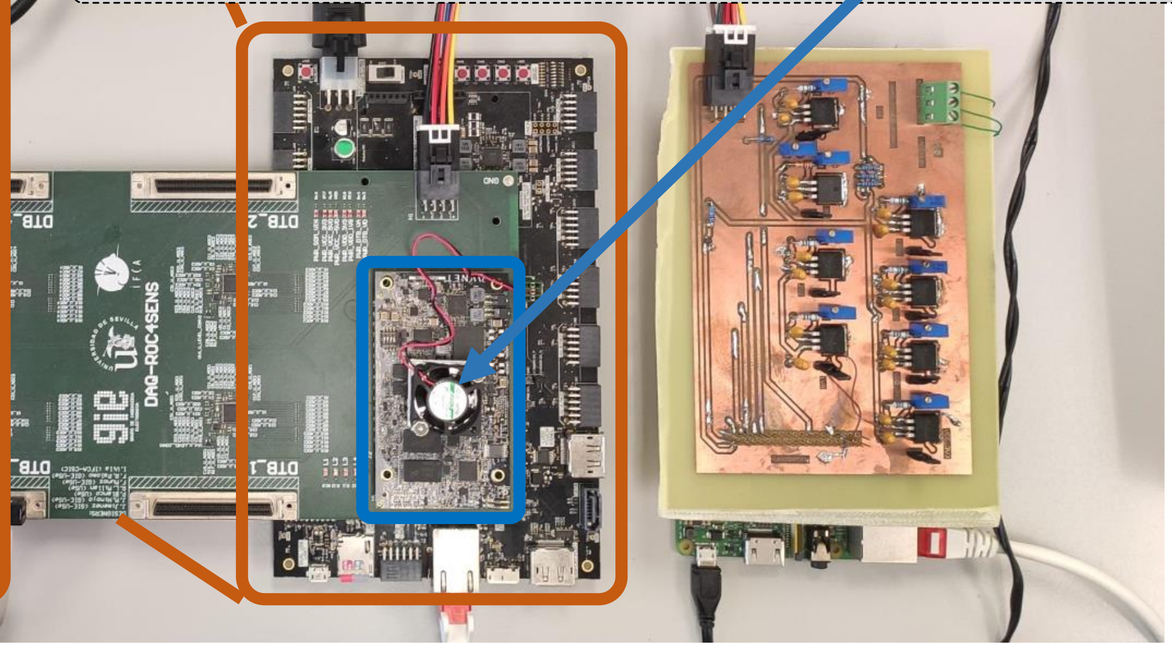




A RoC4Sens chip needs an external logical driving unit, responsable of Command, Control and Data Acquisiton. In DRAD, the FPGA logic fabric implements that logical management. The ROC4SENS sensors blocks process the commands to the RoC4Sens chips. The I2C controller process the commands for auxiliary elements as the DAC's in the adapter card.

System Description





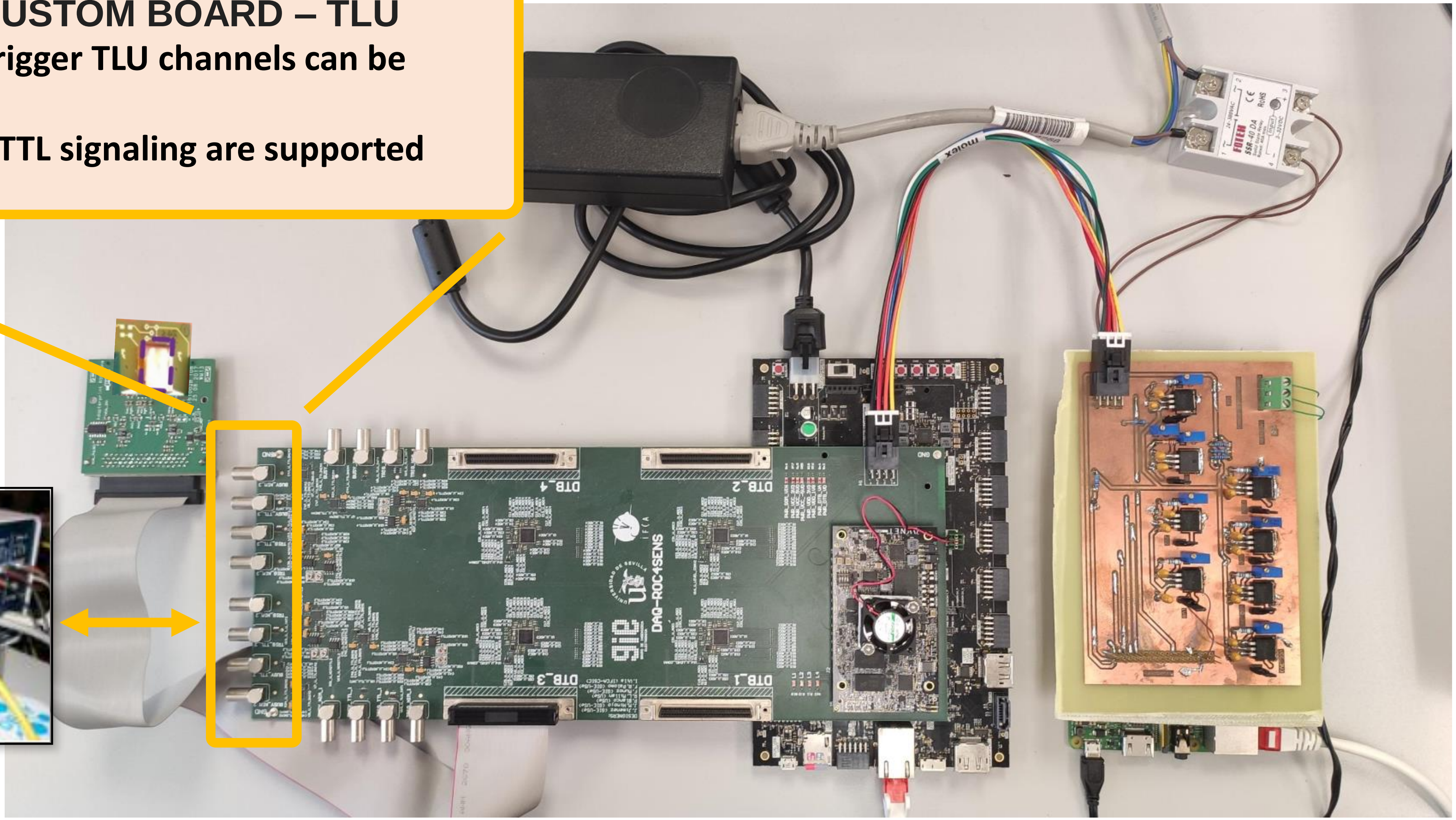
- **UltraZed-EG IO Carrier Card Board:**
  - **It provides input/output interfaces to the Ultrazed SOM**
    - **JTAG**
    - **USB 2.0/3.0**
    - **SATA**
    - **PMOD interface to connect additional devices such as temperature or DAC converters**
    - **SDCard**
    - **Gigabit Connection**

System Description

Interface CUSTOM BOARD – TLU

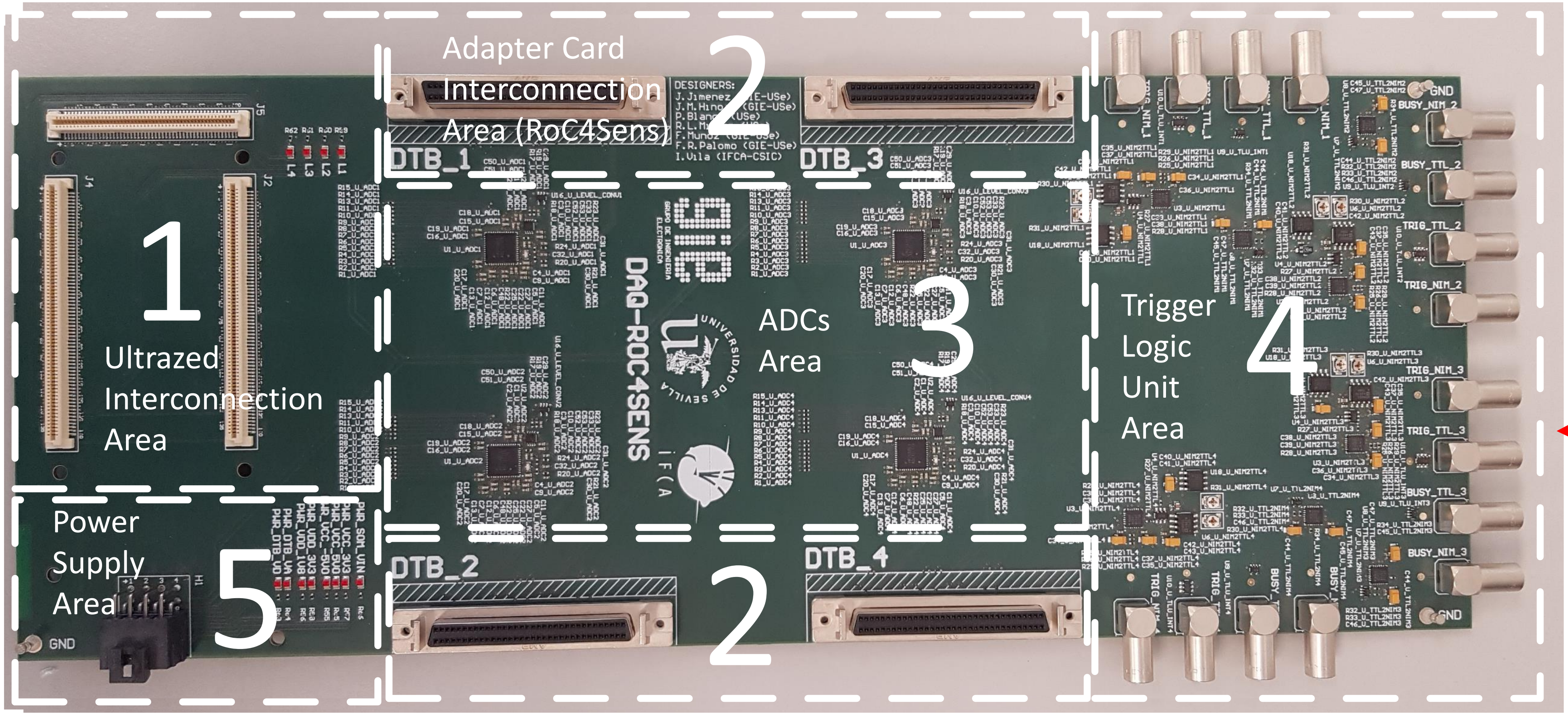
- **Up to 4 Trigger TLU channels can be used**
- **NIM and TTL signaling are supported**

Trigger Logic Unit (TLU)



Custom Board

- Printed Circuit Board, responsable of ADC's (x4), Trigger ports (x4) and NIM2TTL conversión (TLU Area)
- HV bias pixel sensor goes in parallel by a dedicated cable (not in the PCB, it is safer)
- High frecuency design (differential and single ended lines fully isochronous)
- Ten layers stacked



Interface
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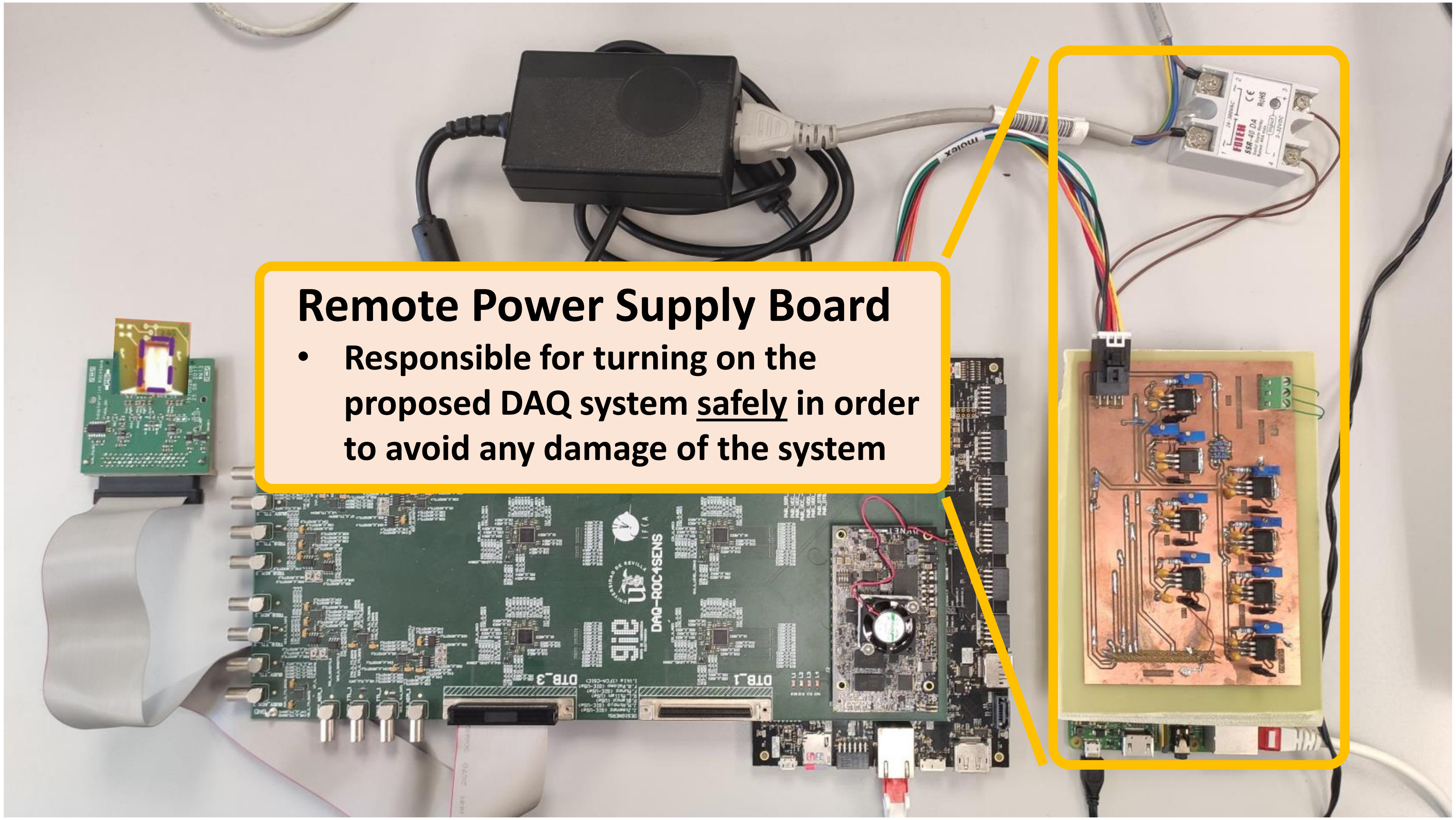
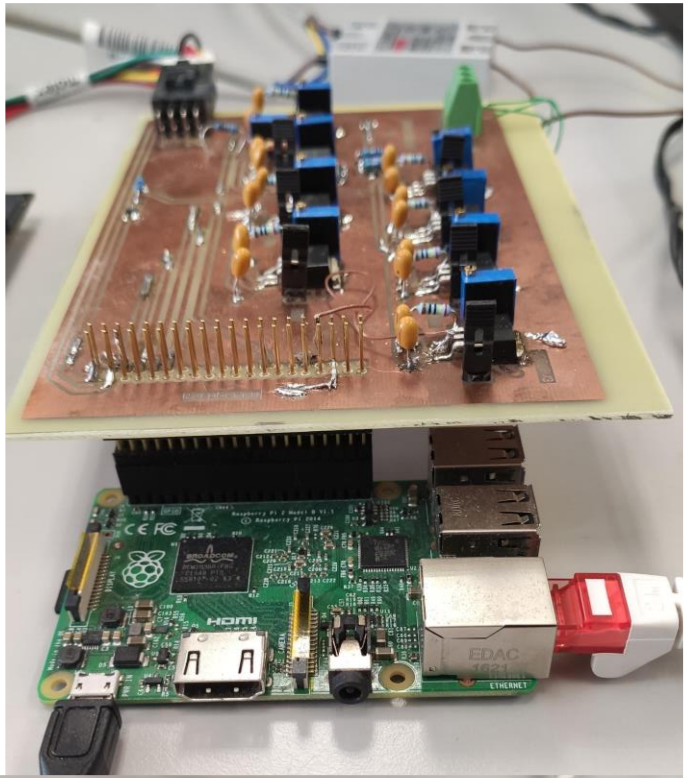
System Description



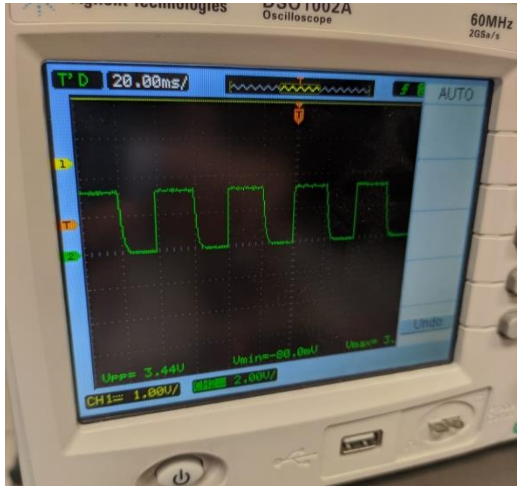
Remote Power Supply Board

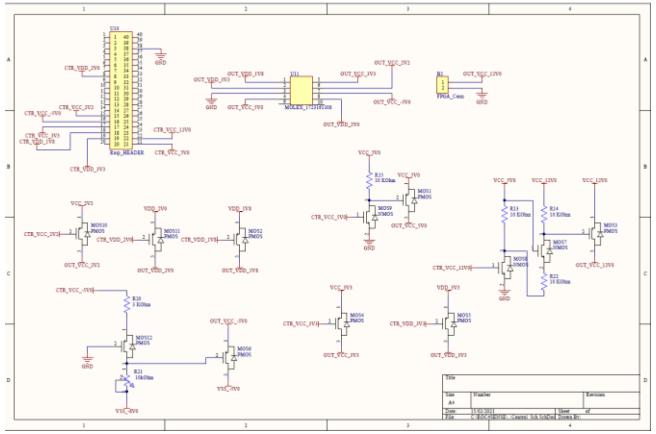
- Responsible for turning on the proposed DAQ system <u>safely</u> in order to avoid any damage of the system

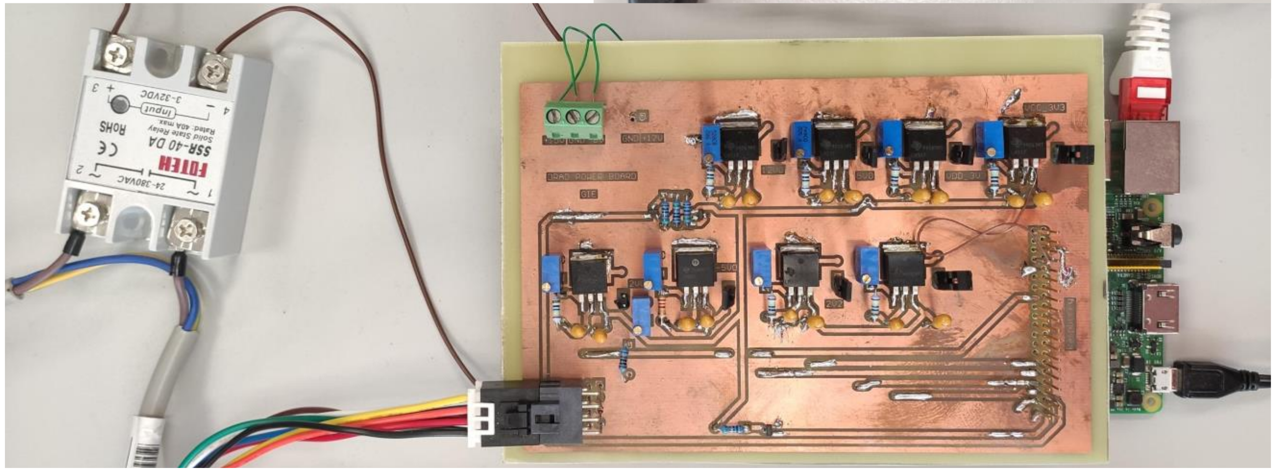
Remote Power Supply Subsystem (R2PS)



- The RP2S allows to turn on the proposed DAQ system remotely and safely
  - The start up sequence is programmed into a Python app.
- It comprises:
  - Raspberry PI: responsable for managing the start-up sequence and providing remote access
  - Master switch relay that turn on/off the FPGA
  - A Raspberry PI HAT that implements the switches to turn on/off each supply voltaje that must be provided to the CB
  - The HV bias will be managed by SCPI or LXI commands. A second switch relay can be included to turn on/off



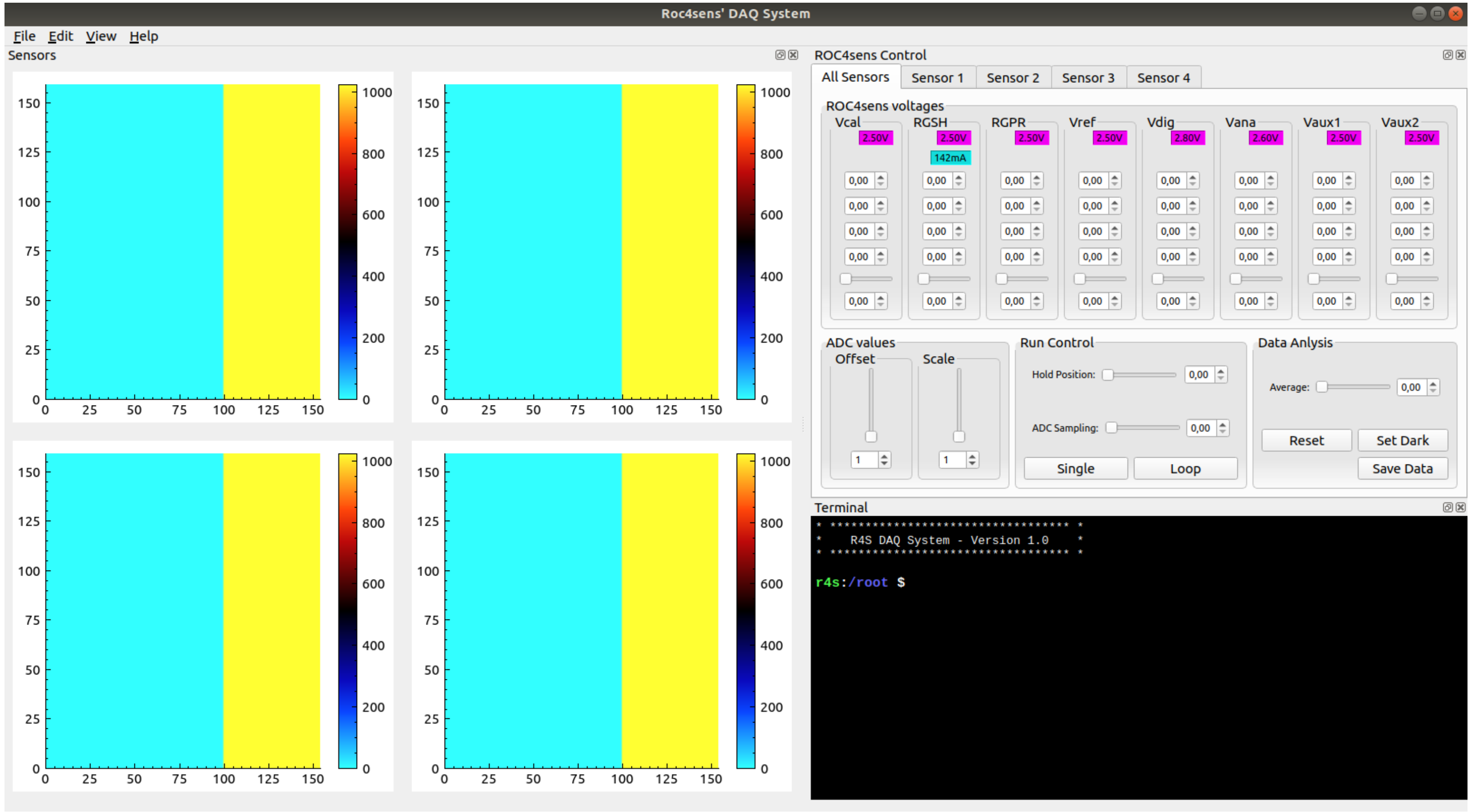




Remote Interface (remote laptop)

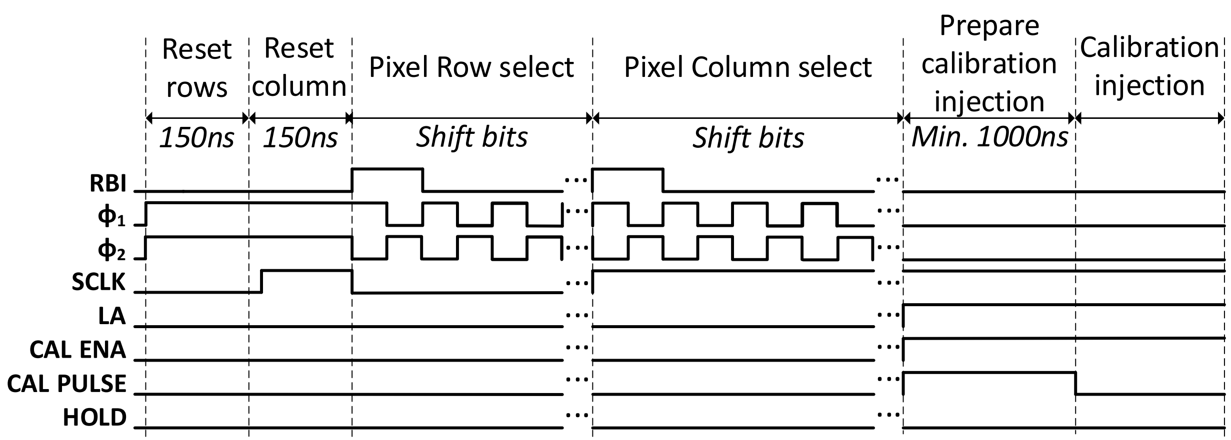
Human Interface (running remotely in a laptop)

- Runs on a remote laptop
- The Client Communicates with the backend by Remote Procedural Calls (RPC) and by UDP/TCP data transfer
- Four pixel displays
- Full set of configuration controls
- Shell available for Python scripts
- Full Duplex (8 ports, 2 associated to each ROC for 2 simultaneous data transfer, triggered and not triggered)
- Client/Server and Server/Client if necessary (architecture duality)

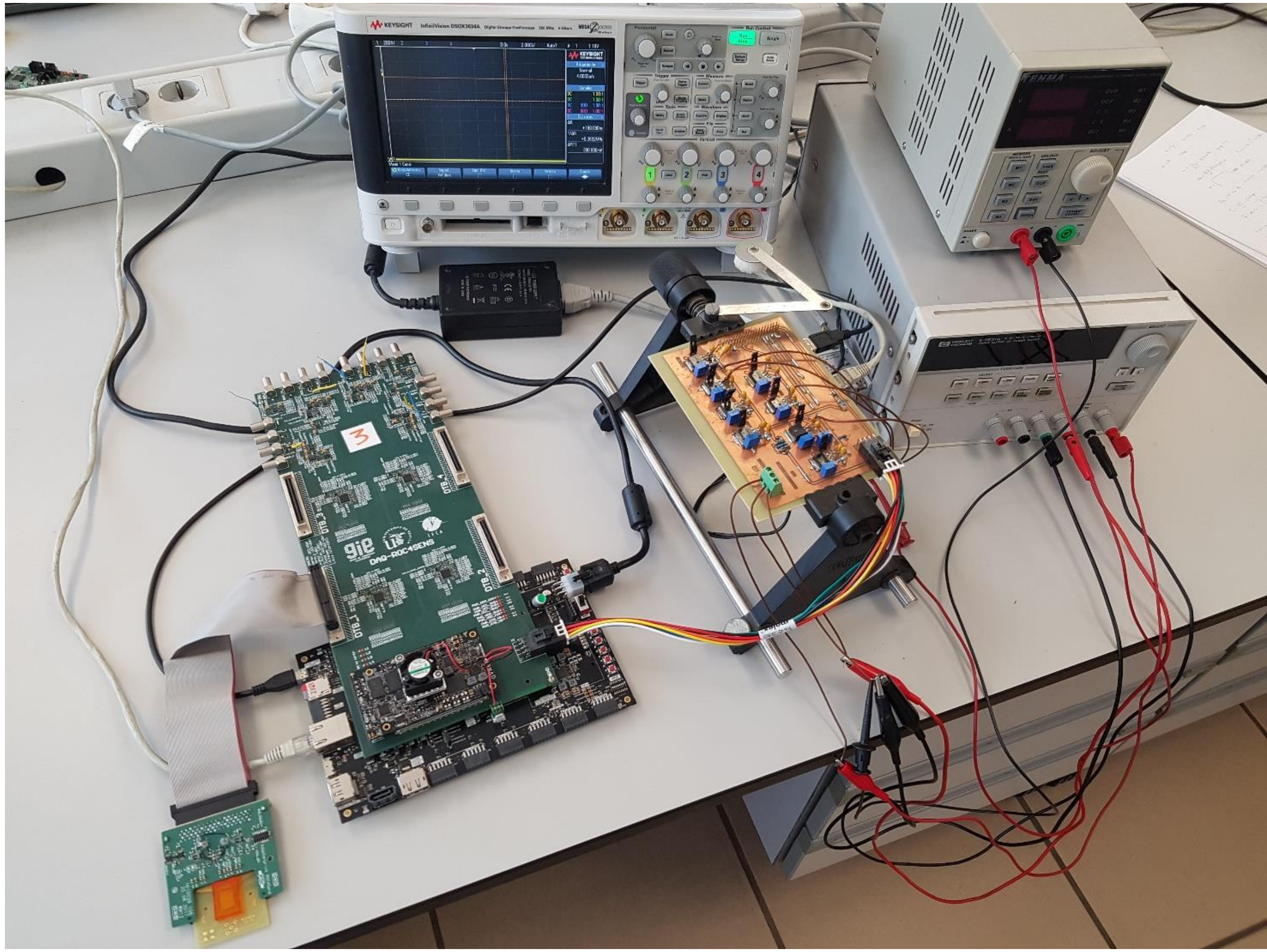


DAQ Roc4Sens: State of the Project

- **DRAD is working in basic modes**



- **We can send commands and receive signals from the RoC4Sens chip**



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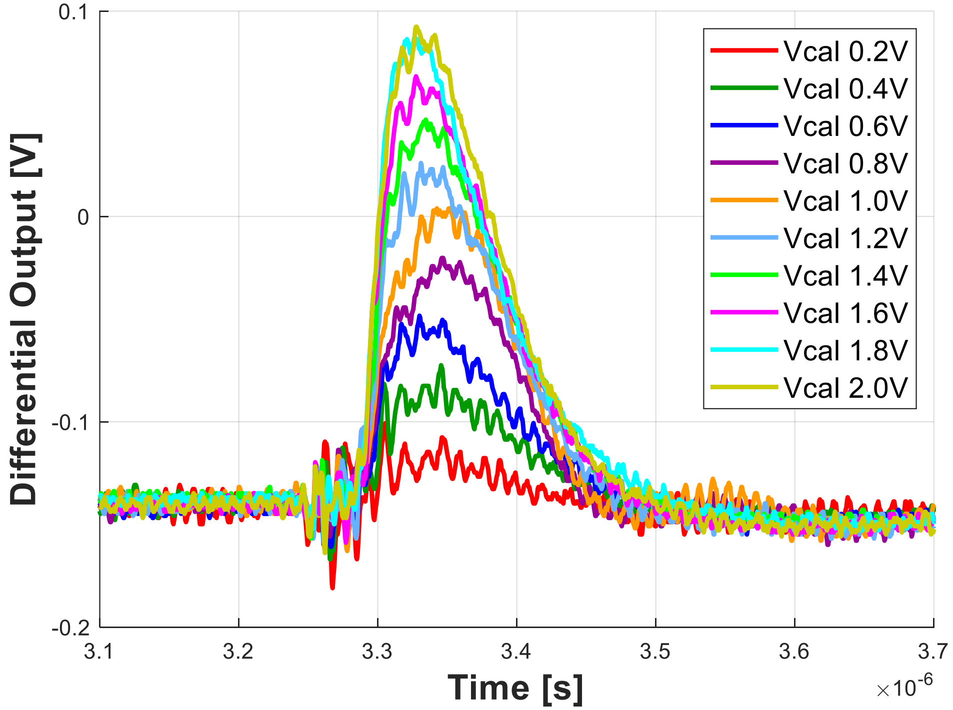
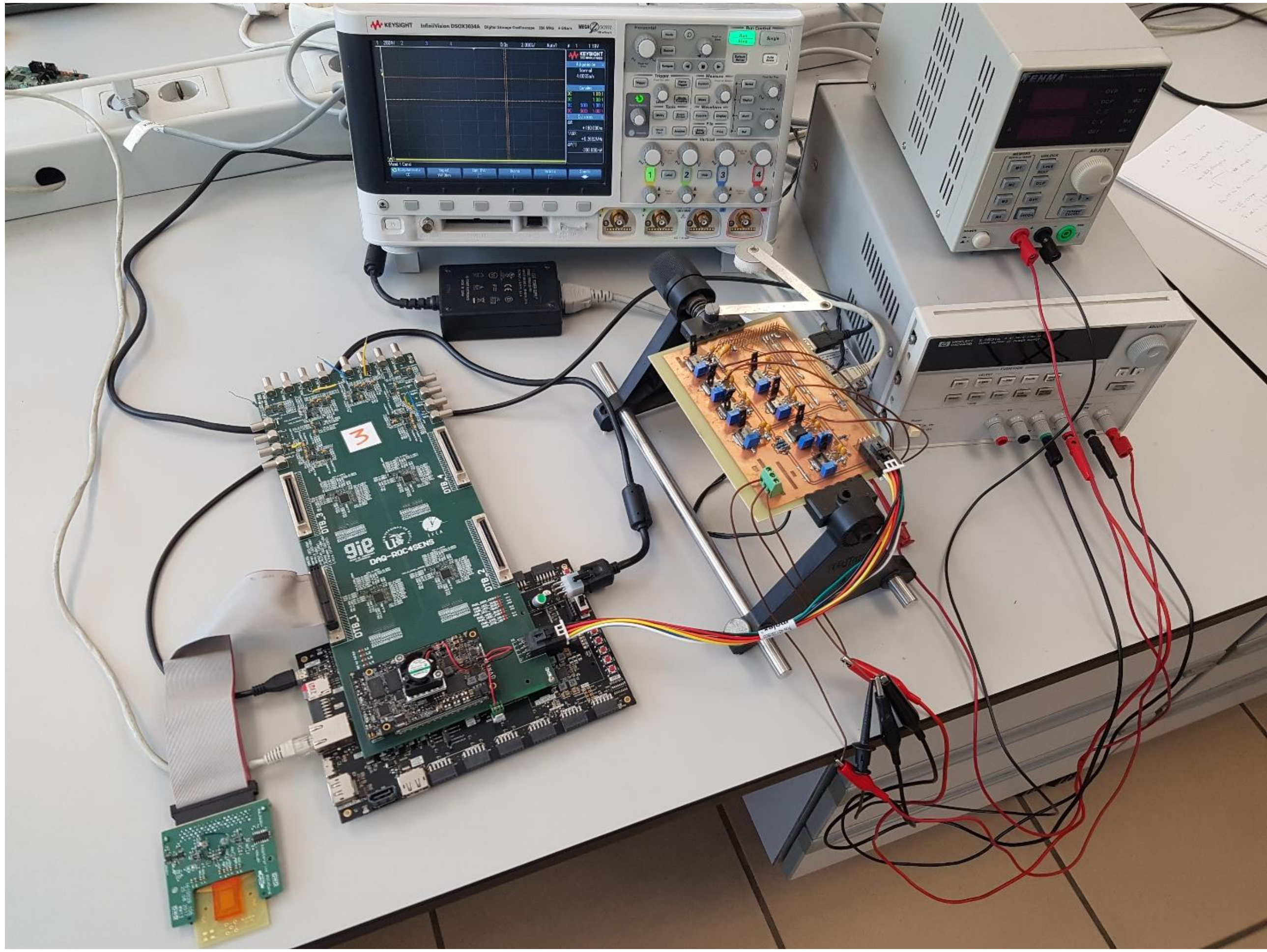
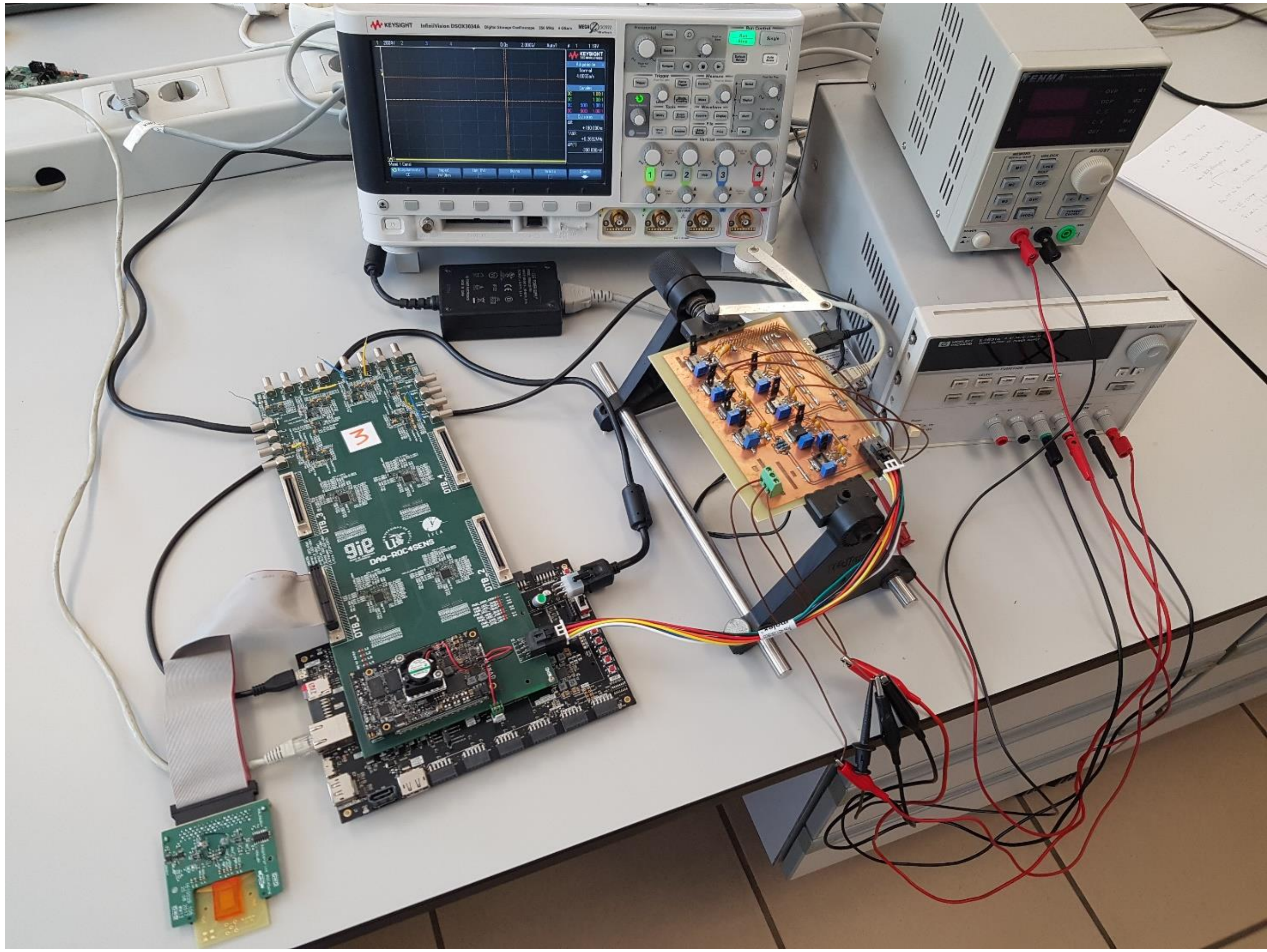




- **We got signals from the test pulse circuitry in every RoC4Sens pixel**

DAQ Roc4Sens: Next steps

- To finalize the ADCs integration phase
- To test the RoC4Sens+Sensor chip in a realistic environment (with radioactive sources, pulsed laser and particle beams)
- We recently received full assembled hybrid pixel detectors from PSI to reach the next goal: a fully working telescope DAQ system.



Conclusions

- DAQ-Roc4Sens at 85% of finalization
- Drastic simplification of the typical testbeam backend arrangement: only one backend acting as a server
- High Data Rate Transfer (>> Mbs), it allows data processing in real time
- Fully comprehensive interface (shell included)
- Full Availability expected in Q3 2022

Thanks for your attention

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