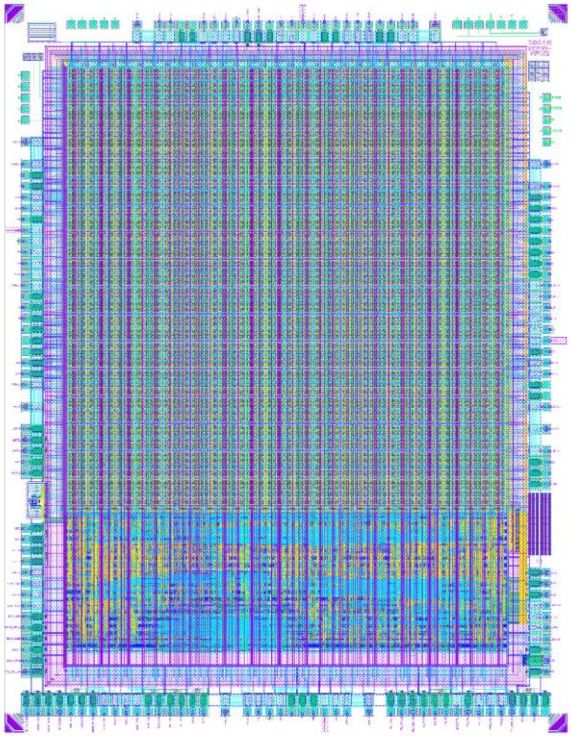


RD50-MPW3:
Digital readout and DAQ developments

Patrick Sieberer, on behalf of the RD50 CMOS working group

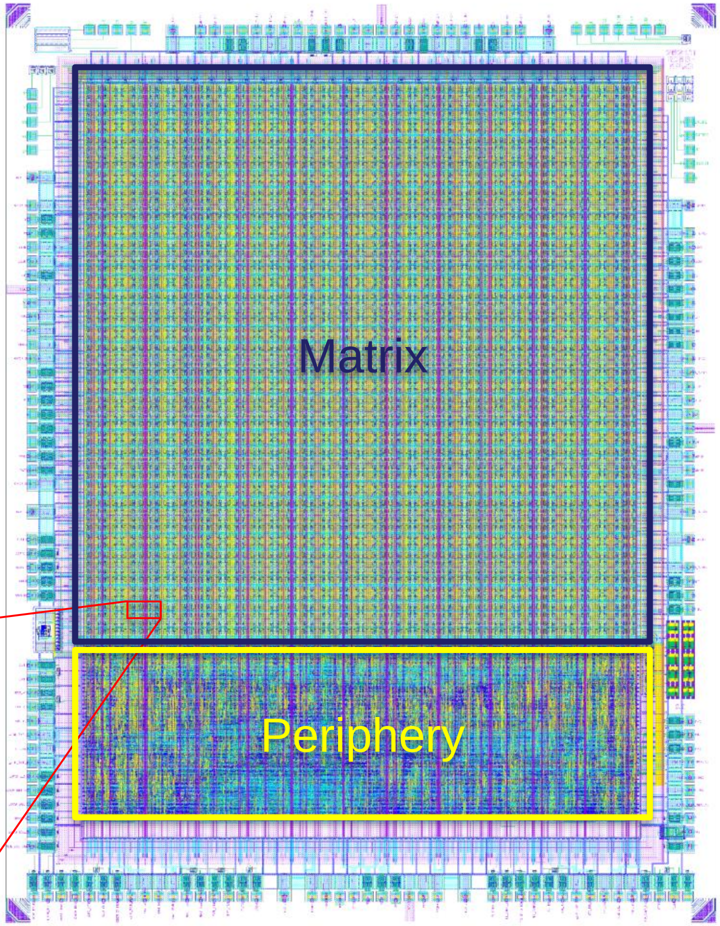
CERN-RD50 CMOS

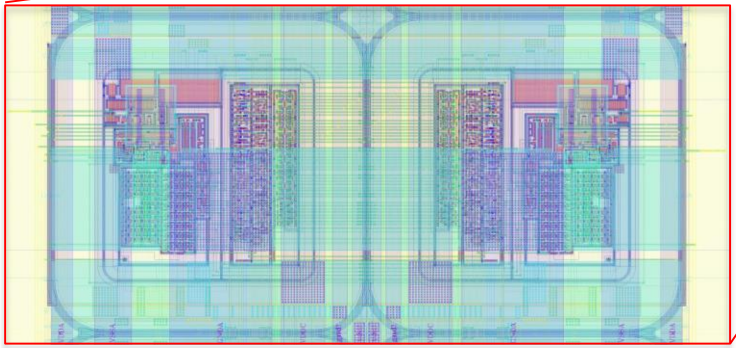
- CERN-RD50 collaboration
  - Radiation hard semiconductor devices for very high luminosity colliders
  - >400 people
  - 63 institutes
- CERN-RD50 CMOS Working Group
  - Program to study and develop monolithic CMOS sensors with
    - High granularity
    - High radiation tolerance
    - LFoundry 150nm HV-CMOS
  - Our program includes
    - TCAD simulations
    - ASIC design
    - DAQ development
    - Performance evaluation
  - Involved resources
    - >40 people
    - 17 institutes

Overview

- Overview of the chip and analog part see presentation by Chenfan
  - Not repeated here

- Content of this presentation:
  - Digital Design
  - Readout chain
  - Off-Chip hardware, firmware + software



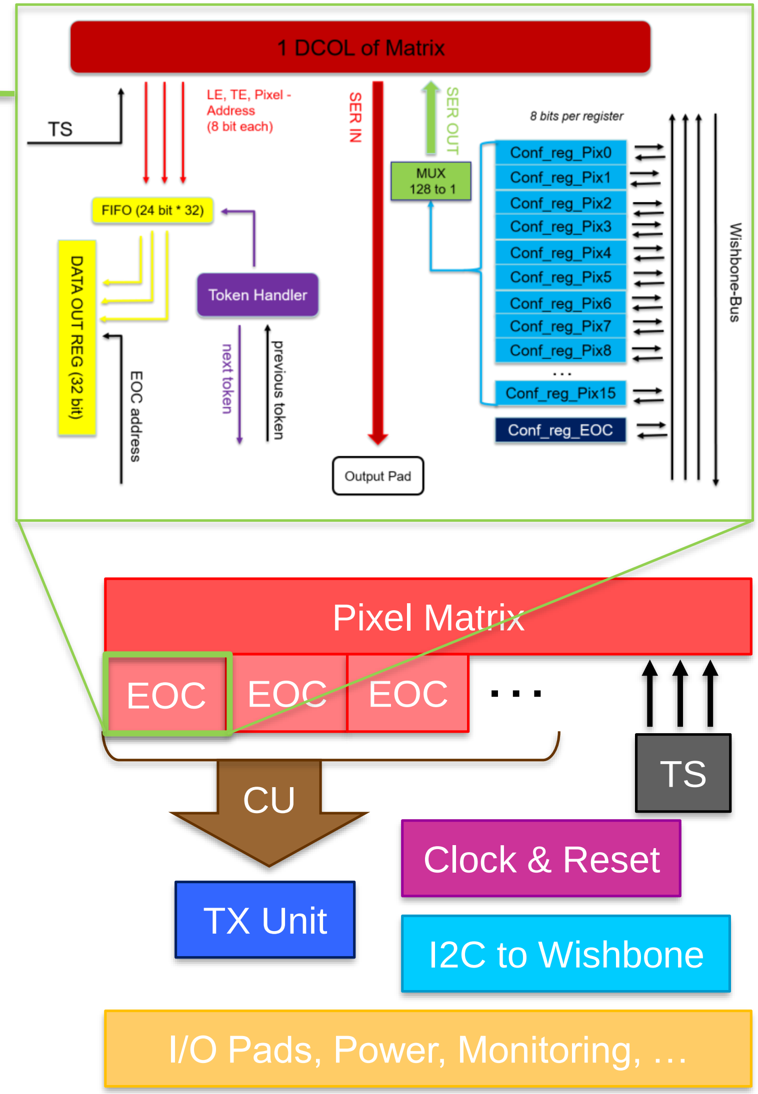


RD50

DIGITAL READOUT IMPLEMENTATION

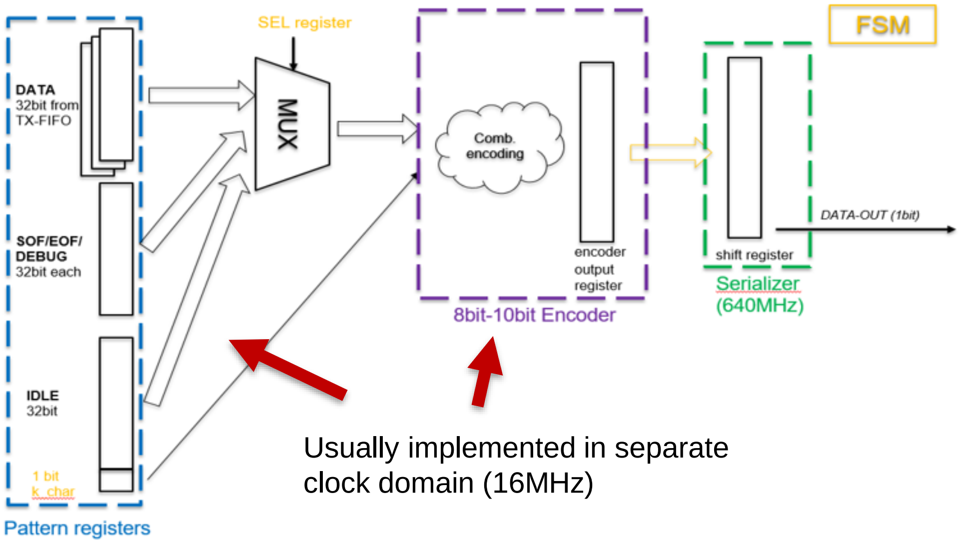
In-chip Electronics

- One End-Of-Column (EOC) per DCOL
  - Configuration of pixels
  - Pixel data readout + 32 words deep buffer
- Transmission Unit (TX Unit) for data transmission
  - 128 words deep buffer (FIFO)
  - Framing
  - Encoding (Aurora 8bit-10bit)
  - Serialization (Serial stream at 640MHz)
- Control Unit (CU) for reading out EOC buffers
  - Controls data propagation from EOCs to TX Unit
- Global Timestamp (TS) Generator
  - 8bit, running at 40MHz
  - Gray-encoded to minimize activity on bus
- Clock and Reset Generator
  - Dividing a fast (640MHz) clock into a 40MHz clock
  - Clock multiplexer for optional external 40MHz
  - Synchronizing the 2 external reset signals with both clock domains
- I2C to wishbone module
  - Converts external I2C signals to internal wishbone control signals



Features of RD50-MPW3

TX Unit



Clock Domain Crossing (CDC)

- Usually, internal clocks are generated using a PLL
    - Not available, complex to design
- Internal 40MHz used
    - generated by a divider from external 640MHz
- Special enable signal (EN, shown below) generated with 640MHz clock
    - 2 different cases, but always exactly 1 rising edge of 40MHz clock within high level of enable
    - Special attention to constraints and clock tree needed

Internal Buffers

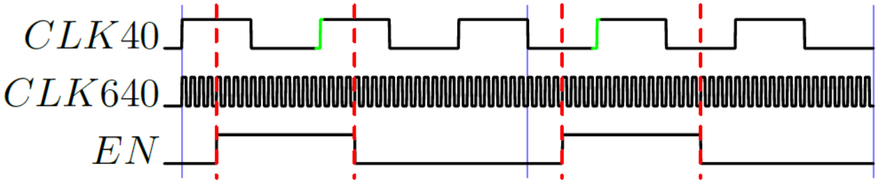
- 2 stage FIFO chain
    - 32 words deep in each DCOL
    - 128 words deep in TX Unit
    - Less high speed buffers in FPGA required

Monitoring

- 10 monitoring outputs for internal signals

External Control

- Parts of internal logic can be controlled with external signals for debugging



Timing of enable signal (EN)

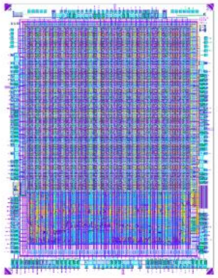
Paper submitted to NIM-A (accepted, not yet published)

Chip IO features

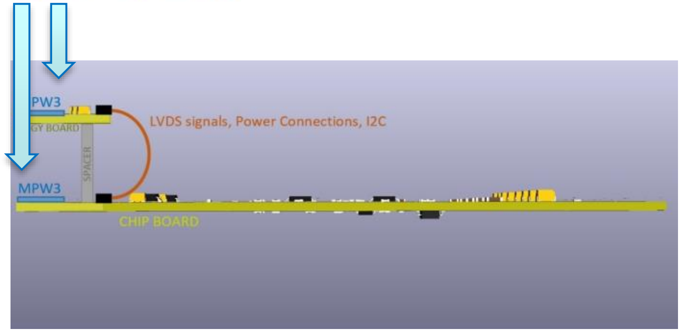
- Configuration: I2C
  - Mapped to internal, parallel bus (wishbone)
- Data: single 640MHz differential line
  - "unordered" in time due to internal 2 level FIFO stages and priority logic
    - Timestamp available (8bit, 40MHz)
    - Level of disorder depends on particle rate
  - Encoded (20% overhead)
- Synchronization: Fast, differential timestamp reset
- Analog: Analog MUX for most power lines, …
- "Trigger-output": HIT-OR
  - Digital OR and analog OR available
  - To be tested if useful as trigger

CONCEPTS RD50-MPW3 DAQ

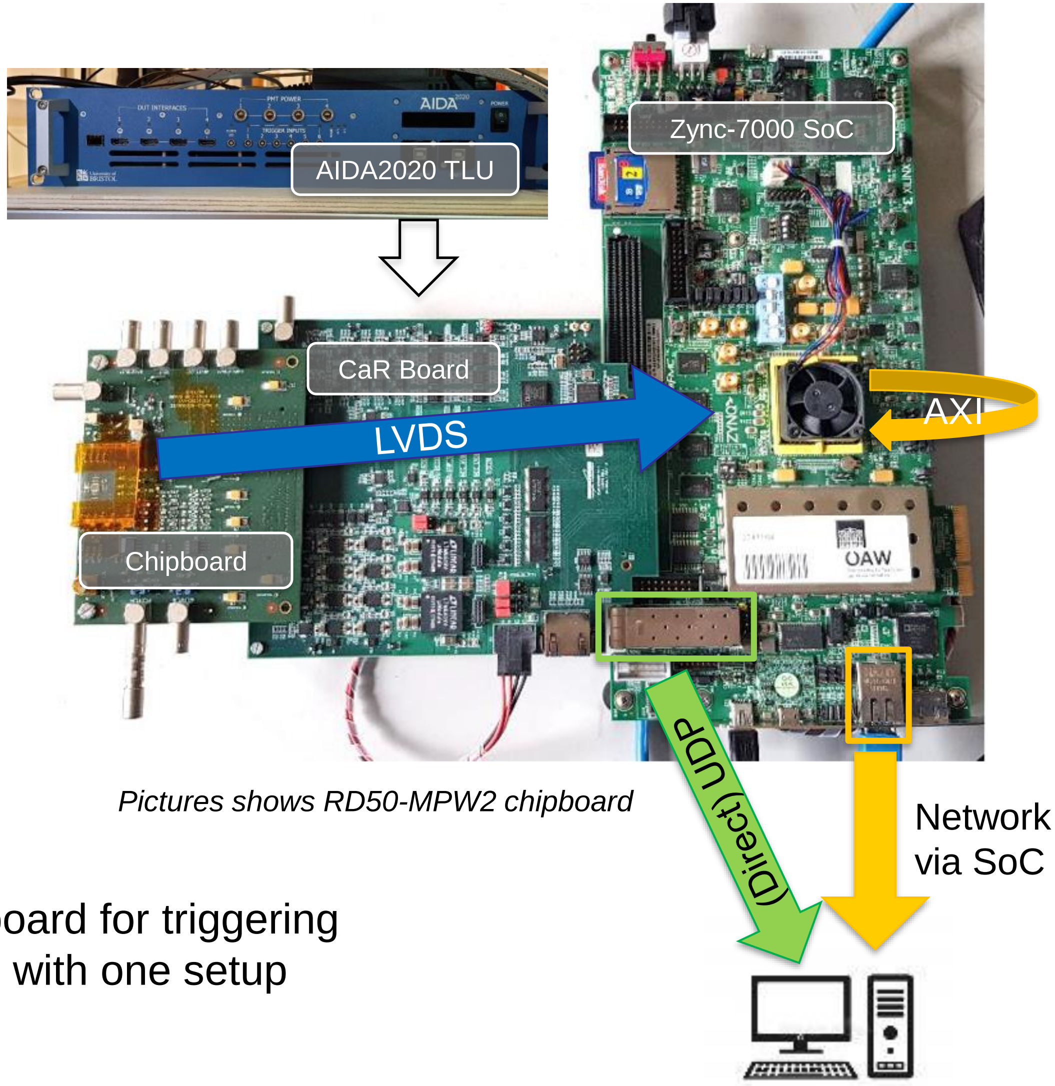
Hardware



- Incoming data stream (to FPGA)
- High speed data path
- Low speed data path (Monitoring)



Draft of RD50-MPW3 chipboard



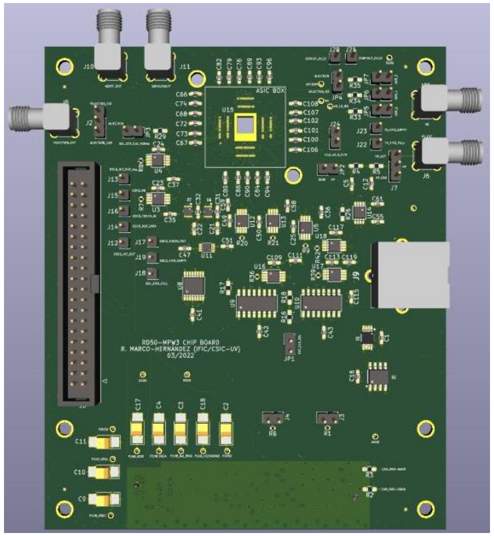
Pictures shows RD50-MPW2 chipboard

- Caribou used as DAQ
- AIDA2020 TLU connected to CaR-board for triggering
- 2-level chipboard to readout 2 chips with one setup
- 2 data paths

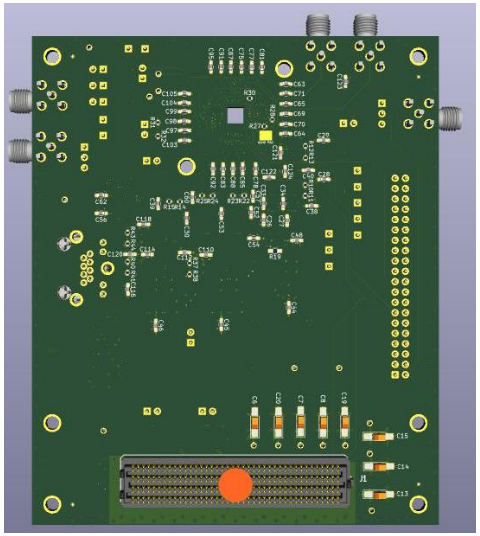
Chip board

IFIC
INSTITUT DE FÍSICA CORPUSCULAR

- Specific board to accomodate and fully test one RD50-MPW3 chip.
- Compatible with Caribou DAQ (CaR board).
- Size of 100 mm x 120 mm.
- 12 layer stack-up to implement controlled impedance tracks, power planes and planes.
- I2C thermometer, unique ID and 2k EEPROM.
- It can be connected to a Piggy board to read out 2 RD50-MPW3 chips with only one CaR board for test beam measurements.
- PCB layout finished.
- First batch of 15 boards fabricated and assembled.



Top view

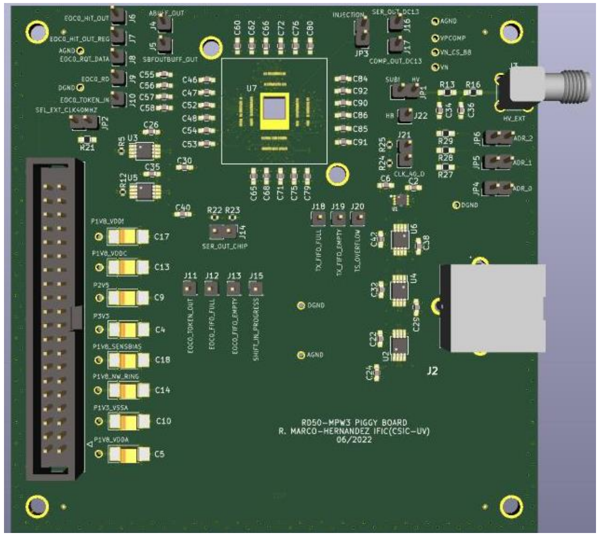


Bottom view

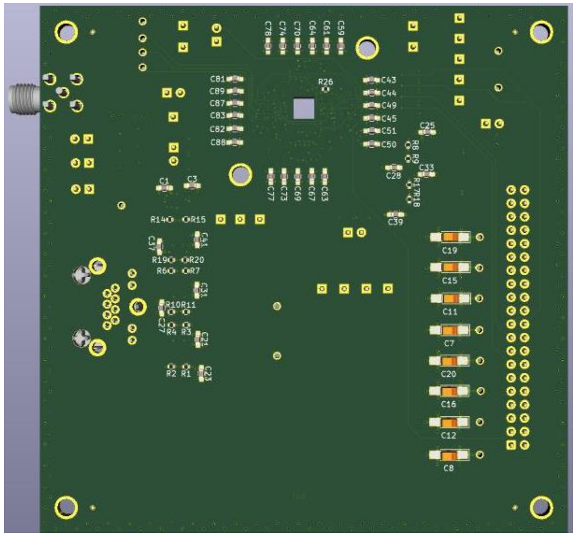
Piggy board

IFIC INSTITUT DE FÍSICA CORPUSCULAR

- Specific board to accomodate one RD50-MPW3 chip.
- Designed to be used connected to a chip board for test beam measurements.
  - IDC connector and RJ45 connector to chip board.
  - Only one CaR board required to read out 2 RD50-MPW3 chips.
- Size of 100 mm x 100 mm.
- 12 layer stack-up to implement controlled impedance tracks, power planes and planes.
- PCB layout finished.
- Production and assembly planned during July.

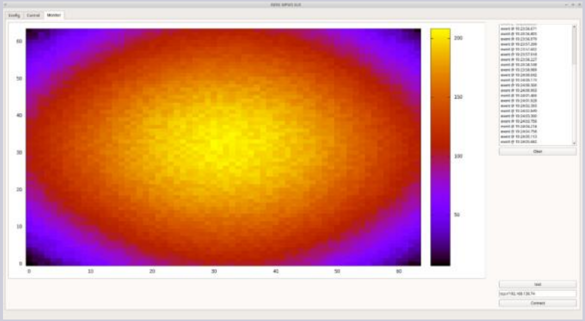


Top view



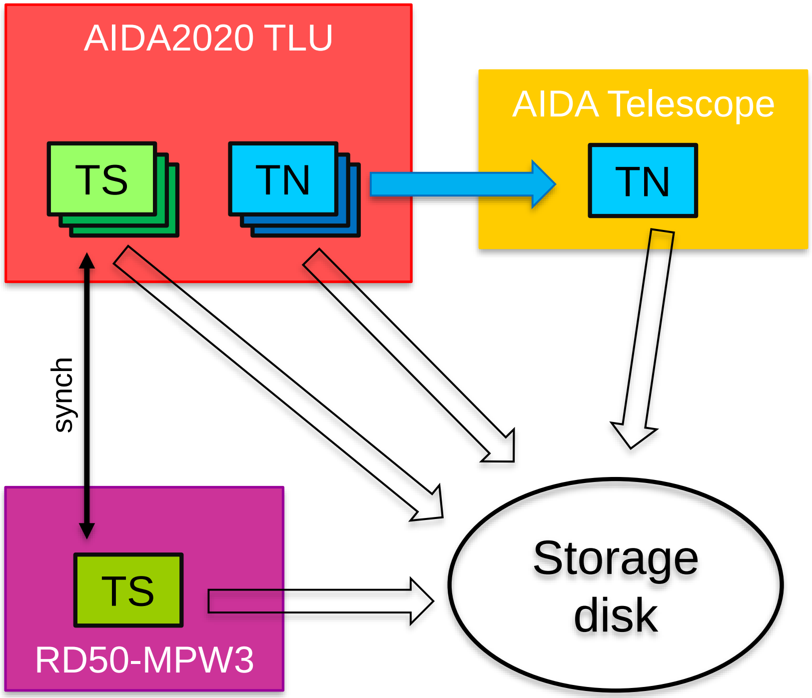
Bottom view

Data Flow and Software

	Fast data path	Slow data path
Purpose	Data taking	Monitoring, Spy Data (small percentage of data)
Data flow	SFP port + UDP (Jumbo frames) for fast, firmware-controlled readout	AXI Bus + Ethernet network for monitoring and slow control
Data storage	Integrated into EUDAQ (EUDAQ raw data files)	EUDAQ + custom data storage possible, Handling of slow control commands
Usage	• data transmission + storage only • easy integration to tracking framework Corryvreckan • Testbeam	• Slow control commands • Monitoring • Standalone tests at laboratory
Current development efforts (examples)	Loopback speed-test at 640MHz implemented • Dummy data generated in FPGA • Data sent to CaRboard, loop-back over FMC connector • Data read by FPGA + sent over UDP to PC (850Mbit/s data rate achieved)	Draft of online monitor: 

Synchronization

- Aiming to operate the chip in fall at CERN SPS together with AIDA telescope
- RD50-MPW3 read out synchronous
  - AIDA-Mode of AIDA2020TLU
  - Synchronization of timestamps (TS) from TLU + RD50-MPW3 at the beginning of each run
- Most telescopes read out asynchronous
  - No internal timestamp
  - Triggernumber (TN) from TLU stored
    - At least handshake needed (!)
- AIDA2020-TLU does matching
  - 2 internal FIFOs
  - Most likely the bottle neck
    - Can handle ~100kHz
    - Limiting factor: receiving CPU



Outlook & Summary

End 2020	End 2021	Begin 2022	July 2022	August 2022	October 2022
• Start Design RD50-MPW3	• Submission RD50-MPW3	• DAQ development • Chipboard design	• Expected Chip delivery	• First Laboratory test • **Test beam at MedAustron**	• **Test beam at CERN SPS**

Summary

- RD50-MPW2 very successful chip
  - Analog performance increased a lot compared to RD50-MPW1
- RD50-MPW3 submitted for fabrication in December 2021
  - Analog pixels electronics from RD50-MPW2
  - New digital periphery
- DAQ Design (Hardware, Firmware and Software) of RD50-MPW3 ongoing
  - <u>No show stoppers seen so far</u>
  - Ultimate goal is to build a small telescope demonstrator

Outlook/ToDo

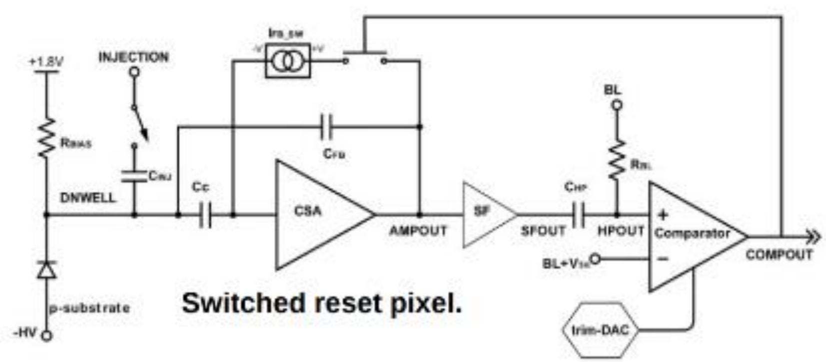
- Triggering/Synchronization with other detectors
  - No internal trigger in RD50-MPW3
  - Synchronous (AIDA-mode) readout with TLU
- "Time bin matching"
  - Order of hits depends a lot on the data rate
    - Due to fast internal readout scheme
  - Time matching tricky when internal timestamp has an overflow (8bit at 25ns -> every 6.4µs)
    - Might be old data in the FIFO chain of the chip
  - Design of a System Verilog based framework ongoing to provide data for different hit rates, occupancies, … for developing a software algorithm

This work has been partly performed in the framework of the CERN-RD50 collaboration. It has received funding from the Austrian Research Promotion Agency (FFG), grant number 878691 and from the European Union's Horizon 2020 Research and Innovation program under grant agreement 101004761 (AIDAinnova).

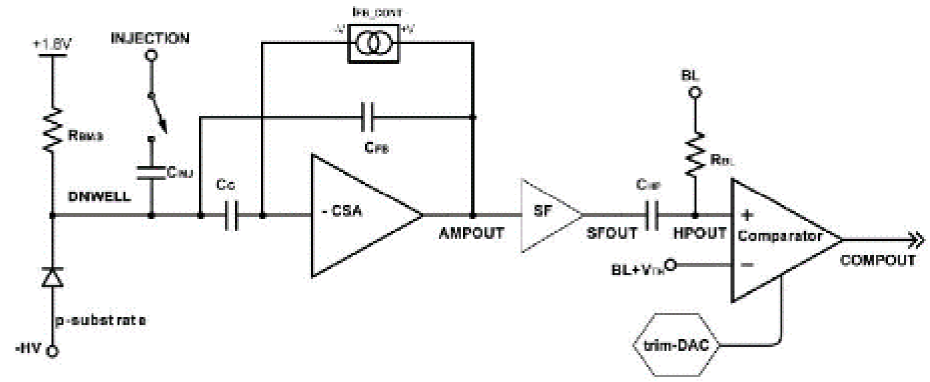
BACKUP

Pixel Flavors

Switched Reset Pixel

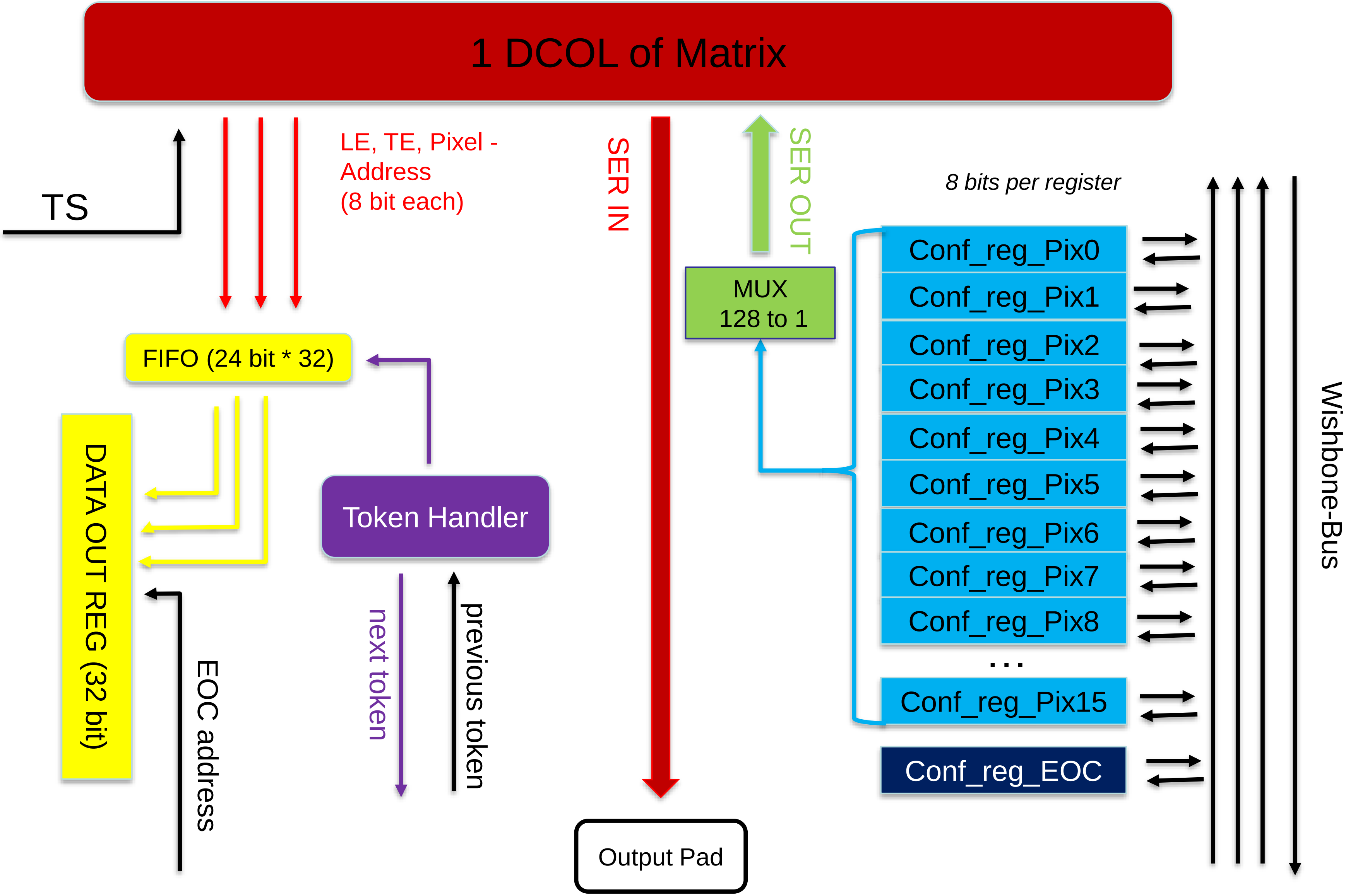


Continuous Reset Pixel



DIGITAL READOUT IMPLEMENTATION

Matrix Readout and Control – End Of Column (EOC)



TRIGGERING RD50-MPW3

AIDA TLU

AIDA-TLU with 2 possible DUT interfaces:

- EUDET Mode: Needed for Hephy-telescope and many other older telescope
  - Whenever no (fast or “synchronizable”) internal TS is available in the telescope
- AIDA Mode: Needed for RD50-MPW3 and newer telescope (probably at CERN)
  - Whenever internal TS-synchronizing is possible
  - Much faster than EUDET

Trigger/Busy Handshake With Trigger Number

This interface mode is an extension of the Trigger/Busy handshake.
After the DUT detects that the TLU has de-asserted the TRIGGER line it can cause the TLU to clock out the current trigger number by toggling the DUT clock line. The number is clocked Least Significant Bit (LSB) first.
Figure 4.2 shows the signal timing for this interface mode.

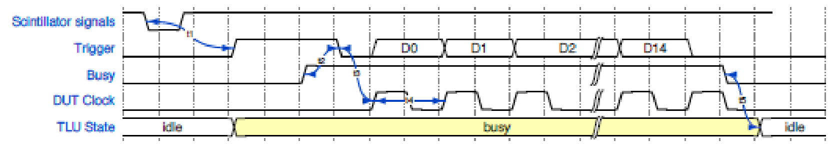


Figure 4.2: Trigger/Busy Interface Mode With Trigger Number

This mode of operations is enabled by setting the DUTMaskMode flag for the specific DUT to 0b00. See section 10.2 for details.

Synchronous (AIDA) Mode

In synchronous mode (also known as AIDA mode) the TLU sends a clock (by default 40MHz) to the DUT.
When the TLU produces a trigger, the trigger line from TLU to DUT is asserted for one cycle of the clock. In order to synchronize time-stamps between TLU to DUT a single cycle timestamp reset signal is issued at the start of each run.
The DUT can veto triggers at any point by asserting the BUSY line.
Figure 4.3 shows the signal timing for this interface mode.

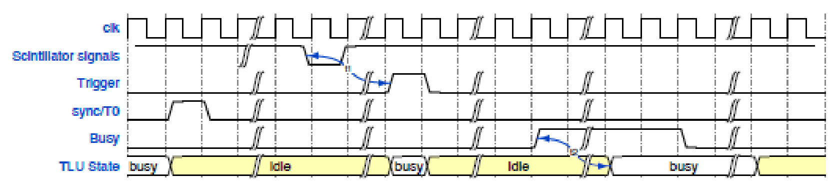


Figure 4.3: Synchronous (AIDA) Interface Mode

This mode of operations is enabled by setting the DUTMaskMode flag for the specific DUT to 0b11. See section 10.2 for details.

Trigger 2

- TLU has two internal, fast FIFOs
  - Trigger Number (TN), 15 bit
  - Fast timestamp (TS-T = TimeStamp-TLU), up to 160MHz, ~16 bit (coarse and fine(?))
- For the EUDET mode, the TN written on the DUT interface after every trigger
  - Trigger input from scintillators needed
- For AIDA mode, TS-C and TS-T are synchronized at the beginning of each run with a special signal on the DUT interface
  - TLU and RD50-MPW3 now have the same TS!
- **EUDAQ Producer available, which reads the two FIFOs of the TLU to match TN with a TS-T (and thus also TS-C)**
  - Event matching must be done offline
  - Data readout over the IPBus, up to **50MHz trigger rate** possible (otherwise, FIFO-overflow)
    - **This determines our max. particle rate we can handle (!)**