Science & Technology Facilities Council
Carleton University
Jožef Stefan Institute Ljubljana, Slovenia
中國科學院高能物理研究所
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University of Birmingham
University of Oxford

Radiation damage investigation of epitaxial p-type silicon using Schottky and pn-junction diodes

E. Giulio Villani, Christoph Klein, Thomas Koffas, Robert Vandusen, Garry Tarr, Angela McCormick, Philip Patrick Allport, Laura Gonella, Ioannis Kopsalis, Igor Mandic, Fergus Wilson, Yebo Chen, Matthew Kurth, Peilian Liu

40th RD50 Workshop, 21-24 June 2022

Project description and goals

- **What:**
  - fabricate Schottky and n^+p diodes on p-type epitaxial (50µm thick) silicon wafers
  - doping concentrations as they are normally found in CMOS MAPS devices

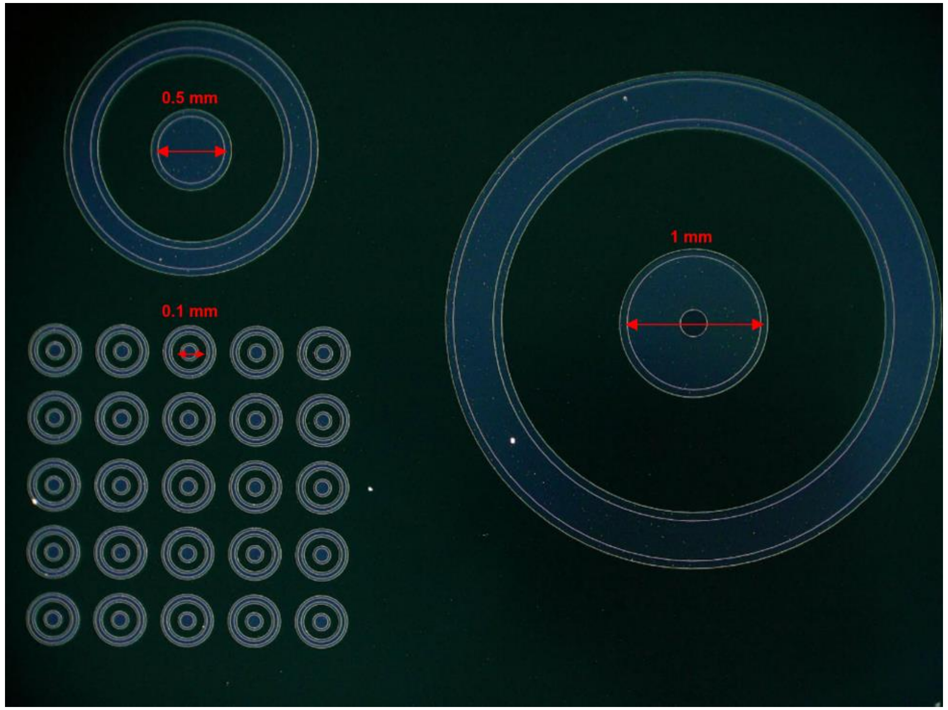
- **Why:**
  - investigate and gain a deeper understanding of radiation bulk damage in CMOS sensors
  - develop reliable damage models that can be implemented in TCAD device simulators

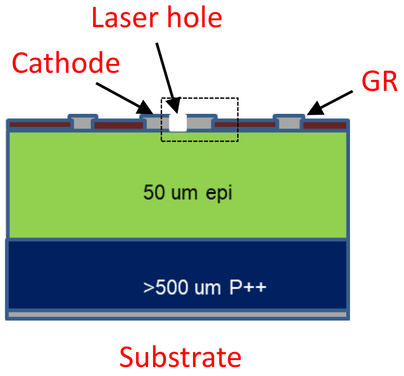
- **How:**
  - purchase of 6-inch wafers at five B-doped epitaxial levels (10^{13}, 10^{14}, 10^{15}, 10^{16} and 10^{17} cm^{-3}) 25x each, total **125 wafers**
  - fabrication process at ITAC (RAL) and Carleton University Microfabrication Facility (CUMFF)
  - measurements will be carried out at RAL, Carleton, Birmingham, JSI, IHEP

Design and layout of devices

5 type of devices proposed:

- #1: 2 mm Ø cathode with 0.4 mm Ø central hole, 10 x 10 mm^2 area
- #2: 1 mm Ø cathode, 0.2 mm Ø central hole, 5 x 5 mm^2
- #3: 0.5 mm Ø cathode, no central hole, 2.5 x 2.5 mm^2
- #4: 0.1 mm Ø cathode, no central hole, 0.5 x 0.5 mm^2
- ‘cell’ with the previous 3 flavors (2,3,4) grouped together, to exploit wafer uniformity on small area
- #5: 6 TLM points for contact and epi resistance
- 2 masks only (metal and oxide)
- detailed description during the 35th RD50 workshop
- different flavours of cathode/GR and option for p-stop in pn-junction diodes (see last RD50 workshop)





Fabrication details & comparison

RAL-ITAC

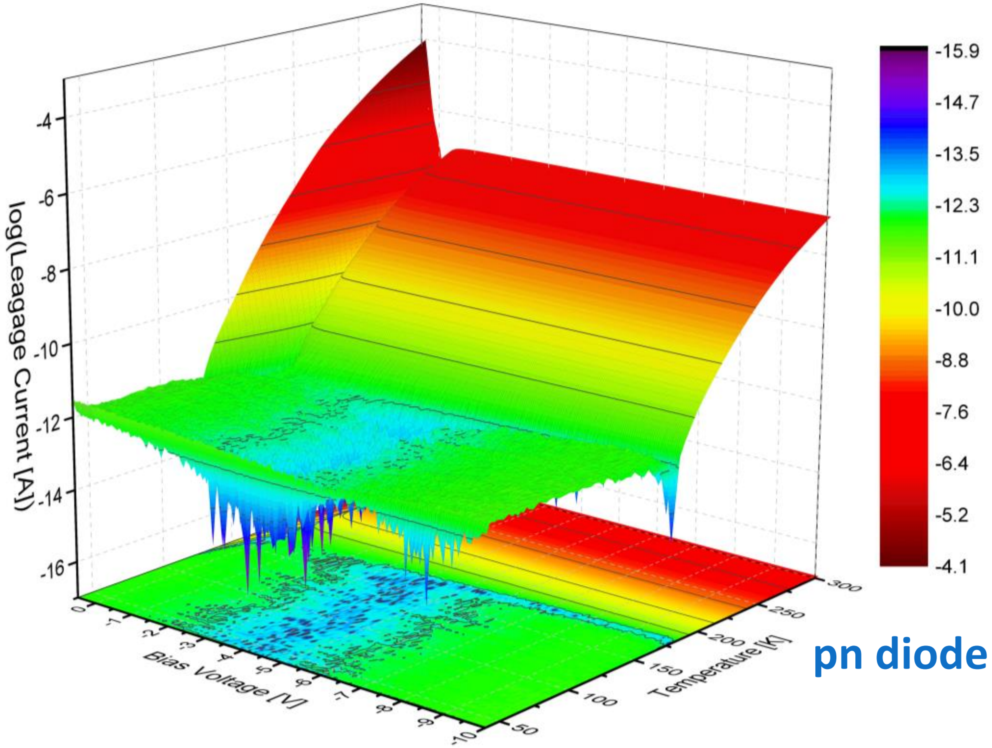
- Schottky fabrication process only, optimised on test wafers
- oxide deposition @150°C
- Al sputtering immediately after etching (no thin SiO2 layer)
- Al lift off in Acetone ultrasonic tank

CUMFF

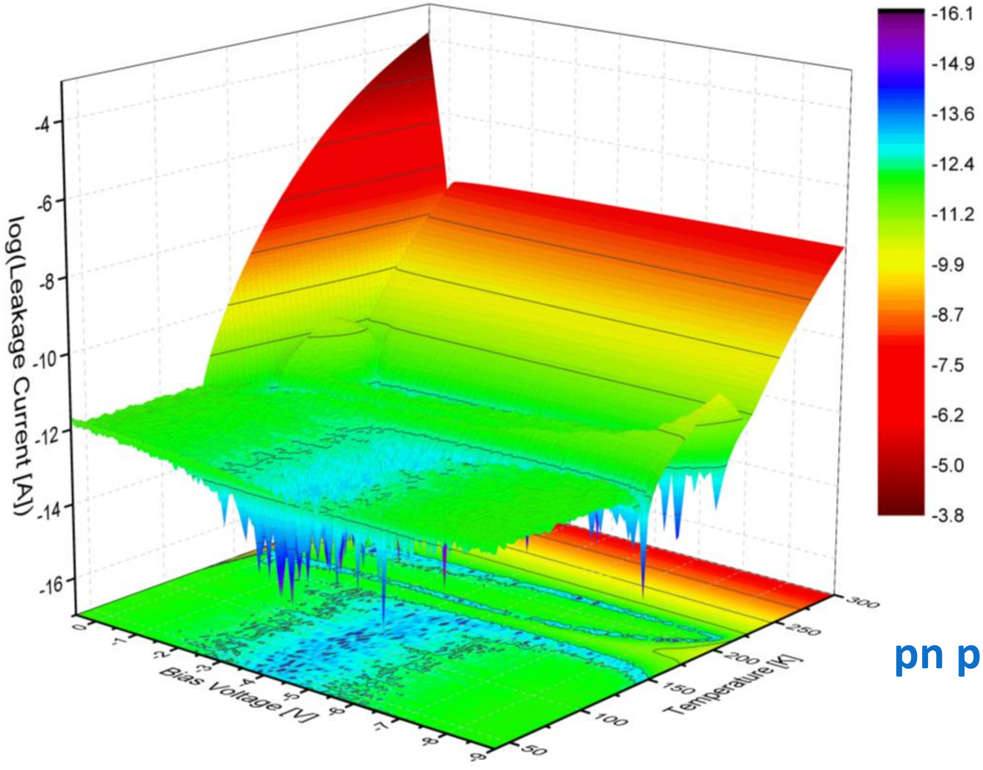
- pn-junction and Schottky processes, optimised on test wafers
- 6” substrate wafers laser cut into 4” or 6” wafer pieces
- high temperature thermal oxidation
- Al front metal thermal deposition, back Al via e-beam evaporation
- front metal patterning + etching

full details of fabrication processes in E.G. Villani’s talk from the 36th RD50 Workshop

IV vs. T measurements



pn diode

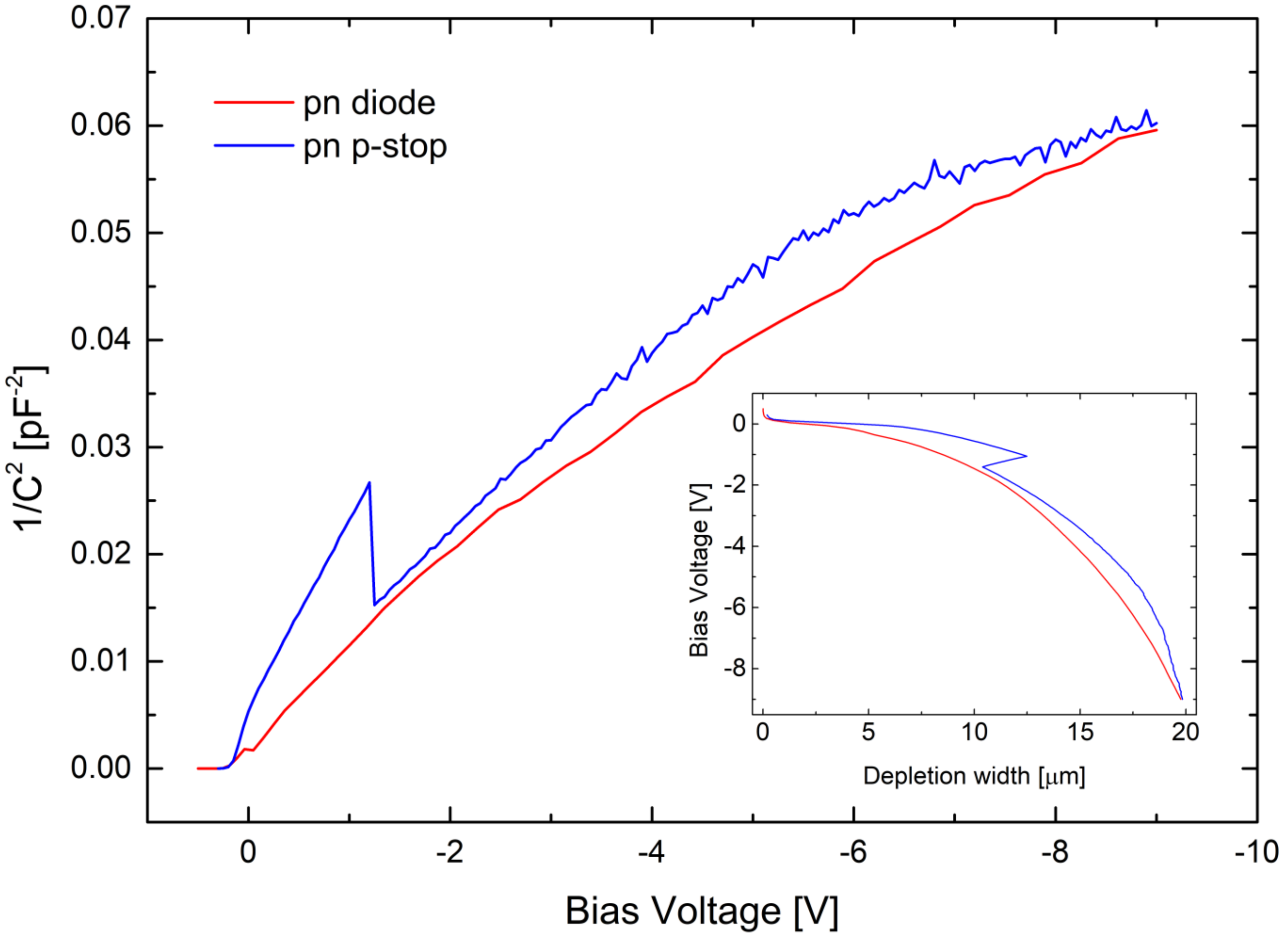


pn p-stop

- diode samples with 1mm cathode
- p-stop sample shows more than 1 polarity switch at some temperatures
- performing I-DLTS might be interesting

CV measurements

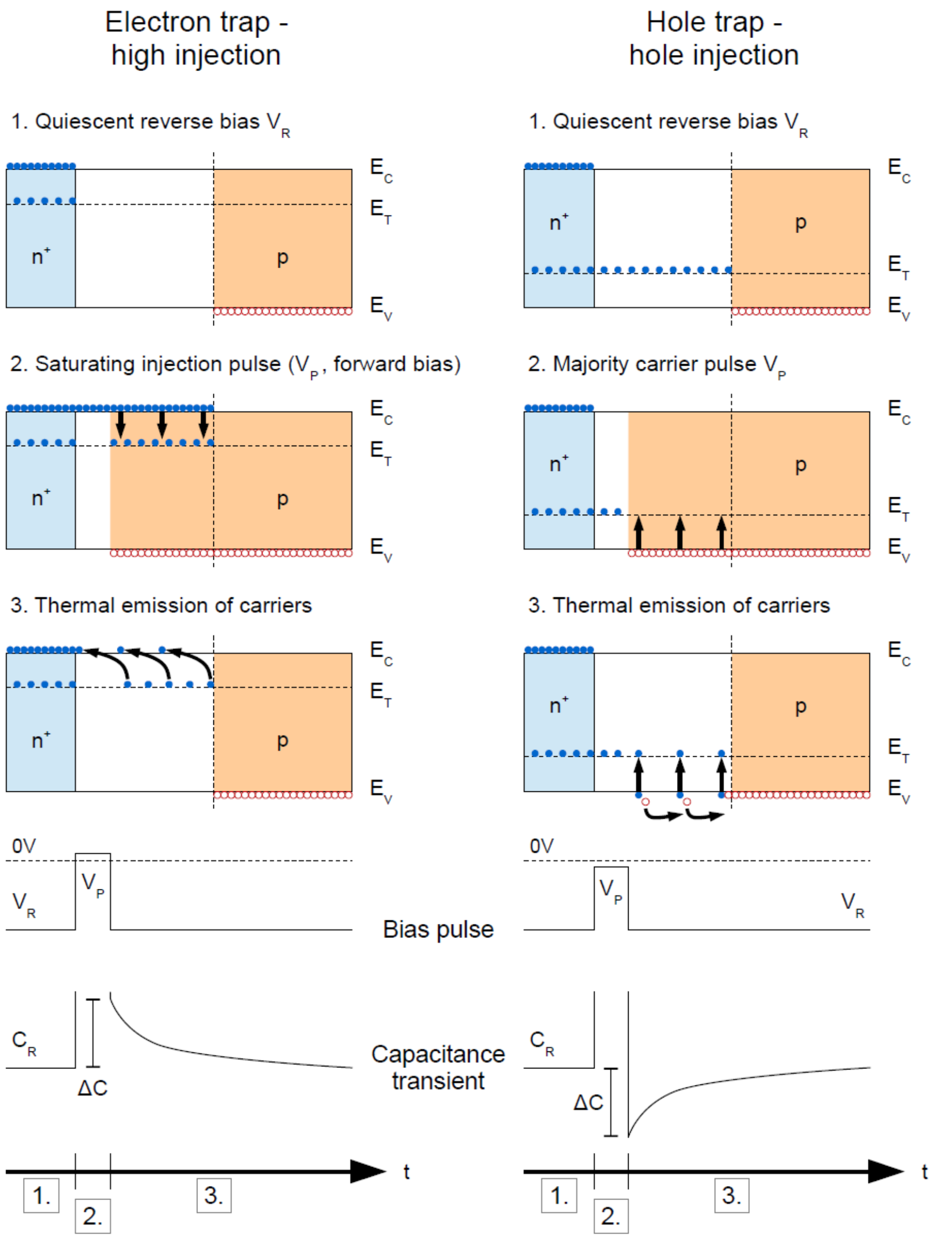
- CV measurements in cryostat setup prior to DLTS
- useful to determine depletion width
  ⇒ indicates bulk width that selected DLTS parameters are sensitive to
  - naïve assumption for lateral depletion = cathode area (1mm) shown in inset graphs
- 'jump' in data of pn-diode with p-stop also observed in other silicon devices with p-stop structures (e.g. ITk testchips)



DLTS: basics

1. DUT is under constant reverse bias
2. filling pulse with specific voltage V_P and duration is applied
    - ○ pulse settings need to be adjusted to trap states of interest
    - ○ V_P as reduced reverse bias → majority carrier traps (holes)
    - ○ V_P slight forward bias → minority carrier traps (electrons), if capture rate much larger than competing majority traps
3. bias back to prior level, measure capacitance transients

- usually average O(100) transients per temperature point to reduce noise
- plot $\Delta C = C(t_2) - C(t_1)$ vs. temperature for fixed times
- analyse peaks/valleys in spectrum by varying Rate Window $[t_1; t_2]$

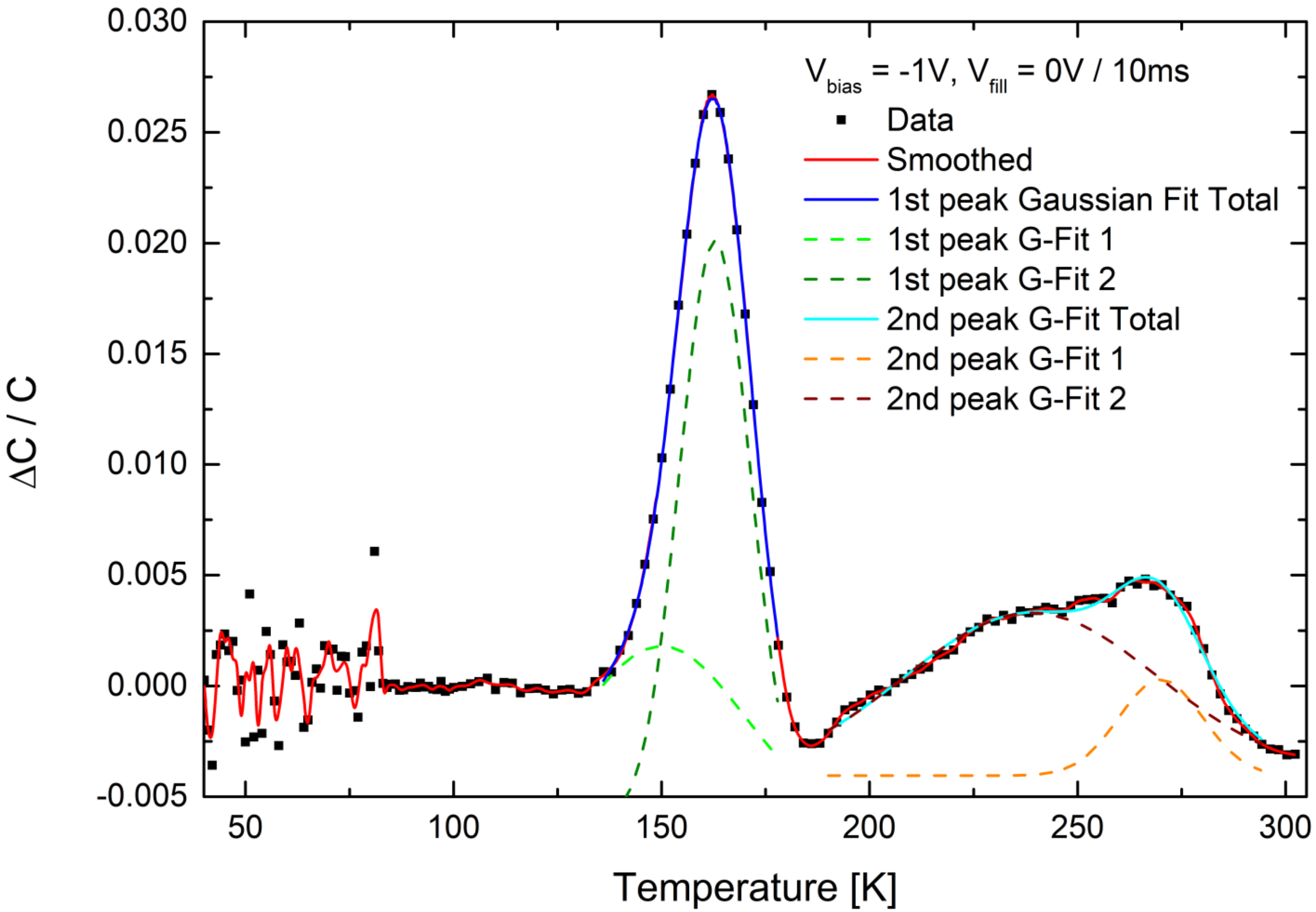


DLTS: Rate Window plots

- multiple DLTS measurements performed for diode sample with/without p-stop
  - different bias voltage + filling pulse settings used

<u>pn p-stop:</u>

- 2 peaks (≙ hole traps) with one clearly a convolution of 2 trap states
  - analysis of more narrow peak at ~165K also shows 2 trap states
  - example of RW analysis shown
- traps did not change much for different bias voltages used



pn diode, with p-stop

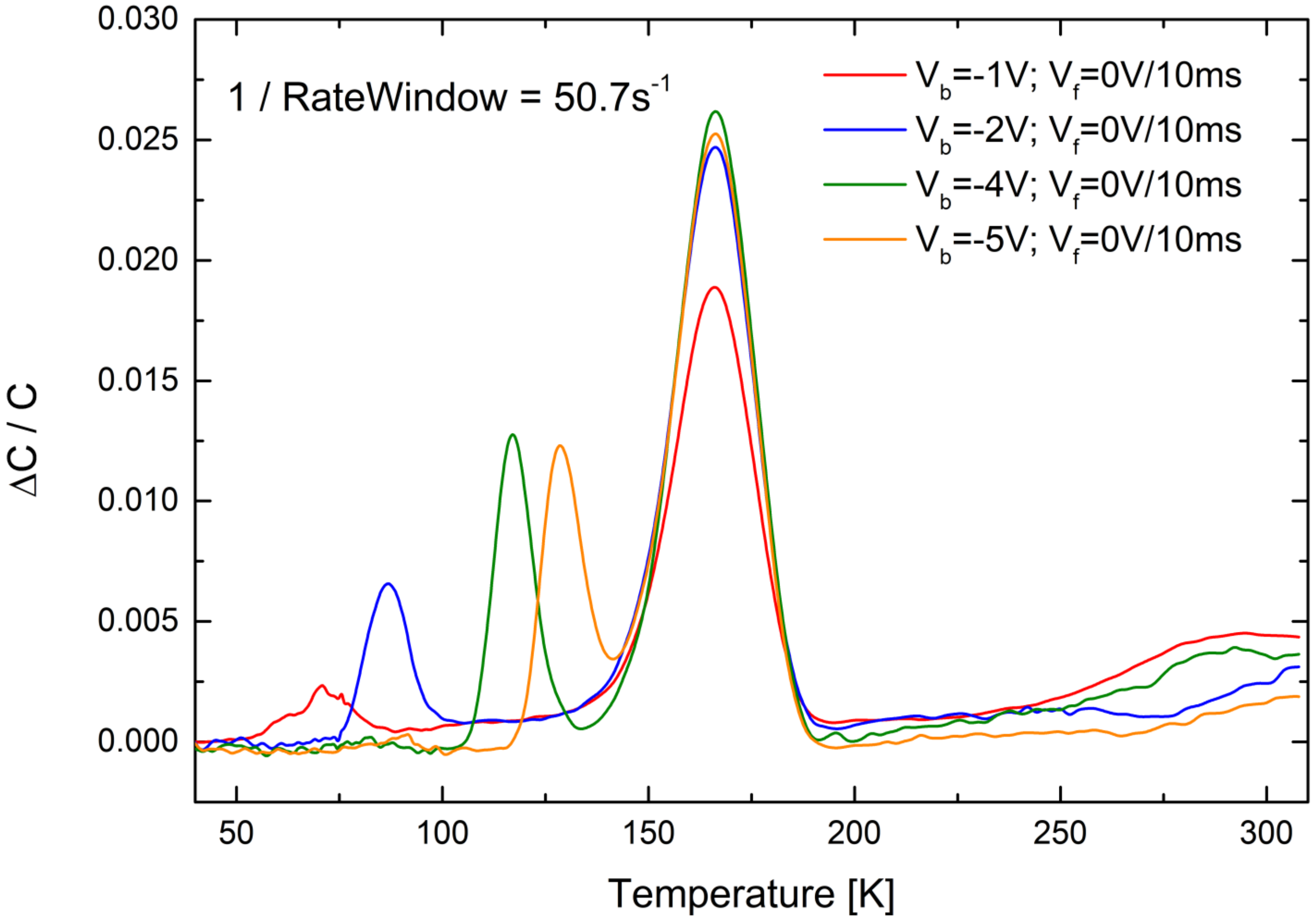
DLTS: Rate Window plots

- multiple DLTS measurements performed for diode sample with/without p-stop
  - different bias voltage + filling pulse settings used

<u>pn-diode:</u>

- Rate Window plots with same Rate Window parameters shown for different scans
- 2 peaks (≙ hole traps) at low T and onset of another peak at room temperature
  - low-T peak shifts for different bias voltage

⇒ **field dependence of trap energy**

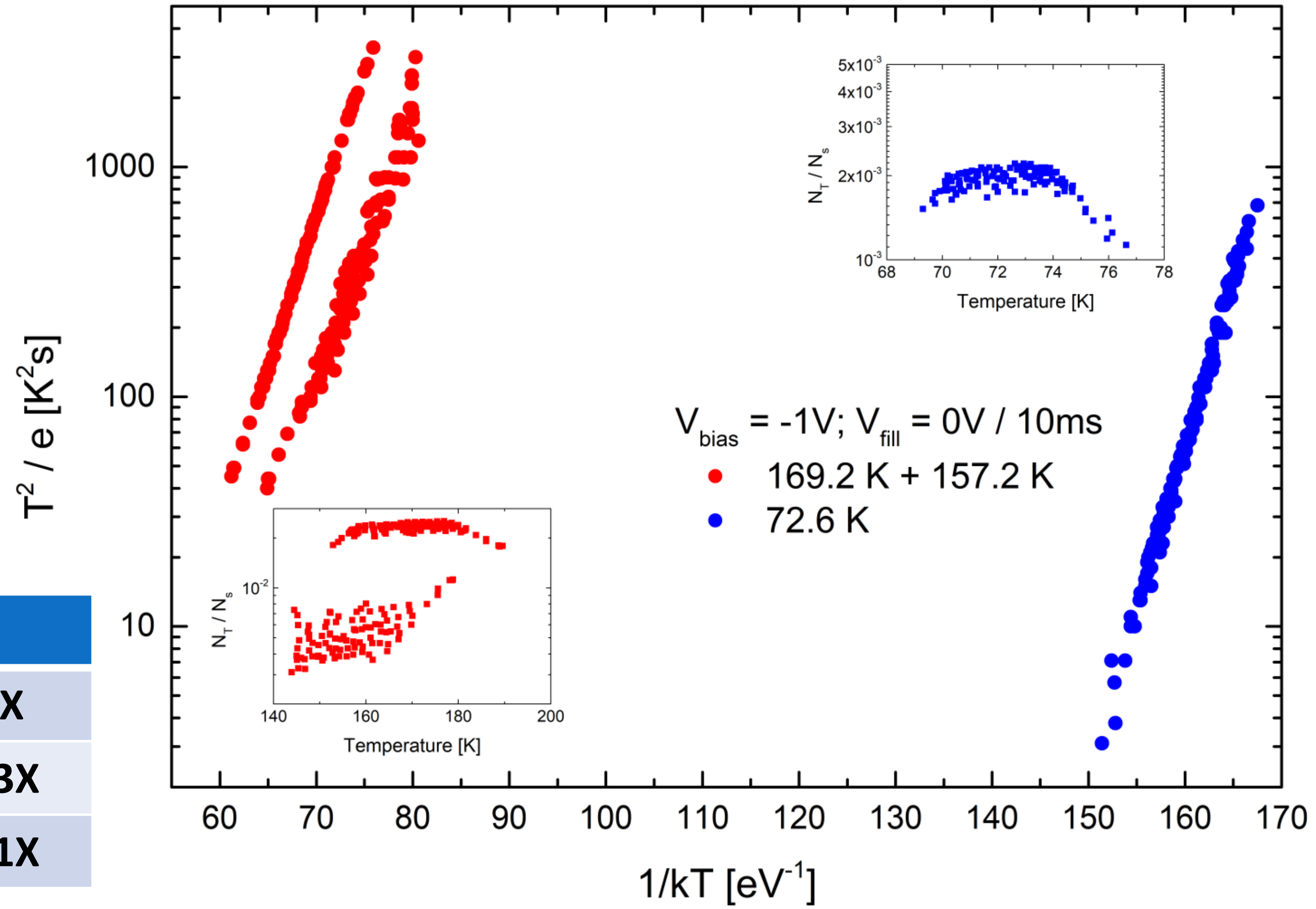


pn diode, no p-stop

DLTS: Arrhenius plots

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels
- more individual Arrhenius plots in backup slides

T_{median} [K]	E_{trap} [eV]	σ [cm^2]
72.6	0.330 ± 0.007	4.1x10^{-1} ± 3.1X
157.2	0.260 ± 0.011	1.9x10^{-16} ± 2.3X
169.2	0.298 ± 0.002	5.8x10^{-16} ± 1.1X

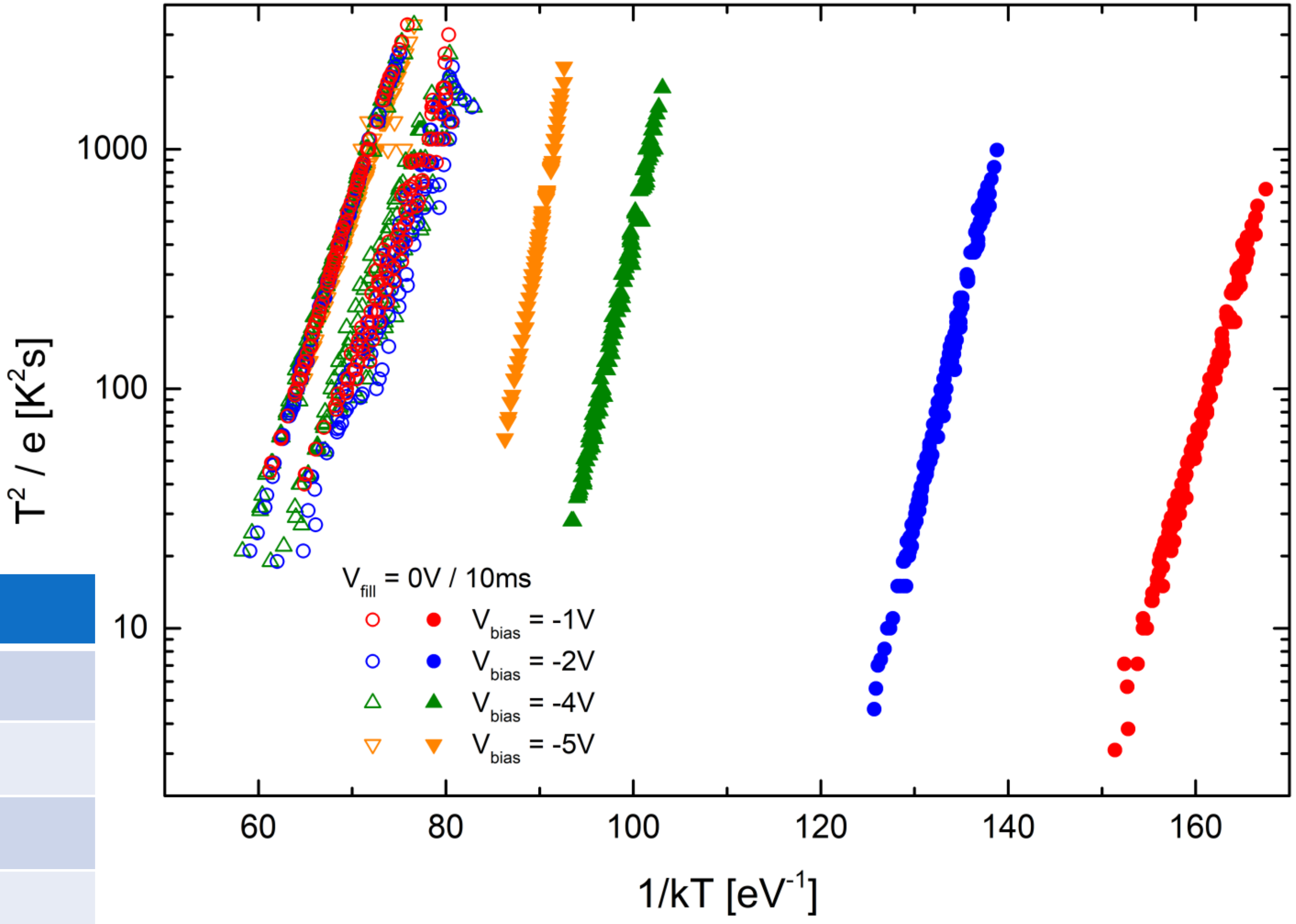


pn diode, no p-stop

DLTS: Arrhenius plots

- good agreement of common 165K peak
  ⇒ peak contains 2 traps each
- field dependence of low-T peak trap parameters

T_{median} [K]	E_{trap} [eV]	σ [cm^2]
72.6 (-1V)	0.330 ± 0.007	4.1×10^{-1} ± 3.1X
87.4 (-2V)	0.407 ± 0.005	9.4×10^{-1} ± 2.0X
118.6 (-4V)	0.442 ± 0.005	9.9×10^{-6} ± 1.6X
129.2 (-5V)	0.545 ± 0.007	1×10^{-3} ± 1.9X

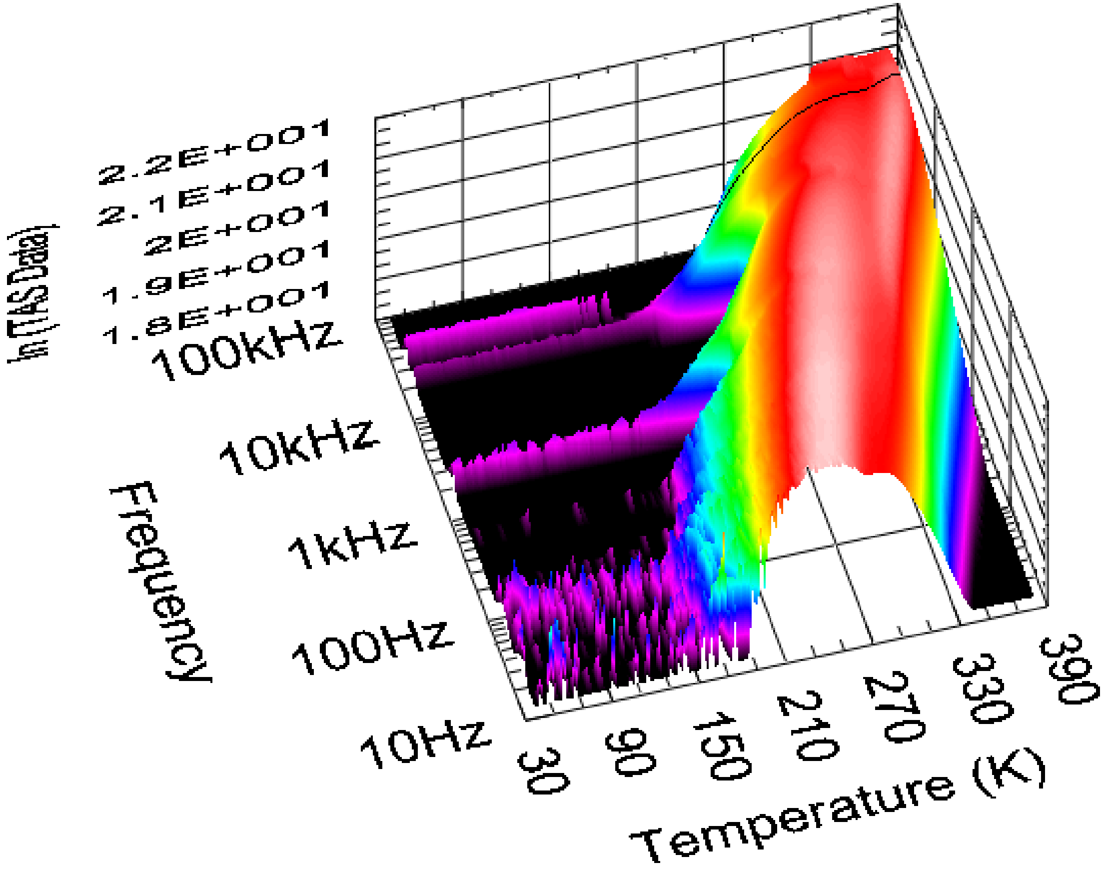


pn diode, no p-stop

Thermal Admittance Spectroscopy (TAS)

TAS:

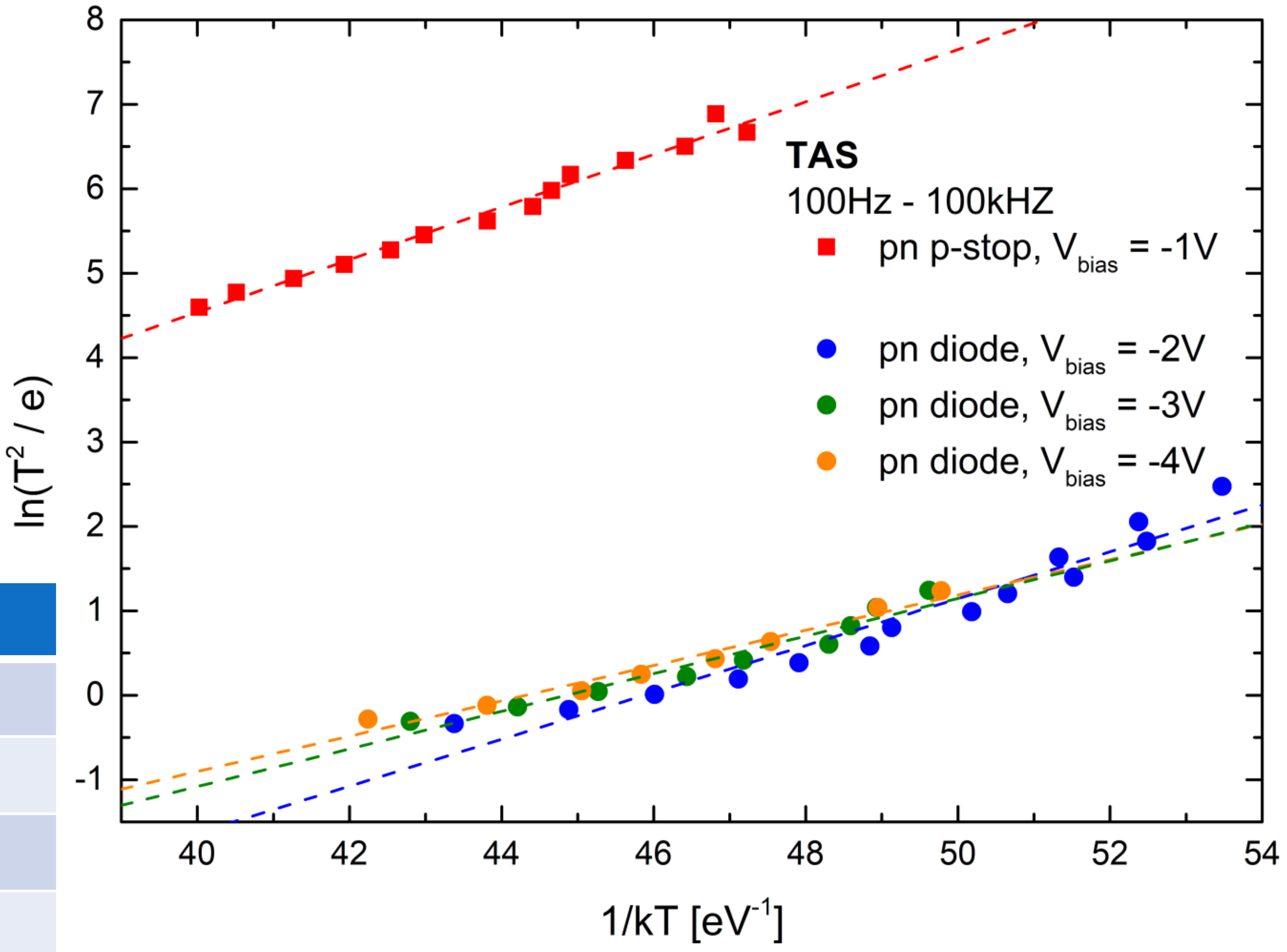
- measure capacitance C and conductance G as function of frequency and temperature
- defect contribution to C/G depending on test signal frequency and temperature
- steps in C or peak in G temperature dependence indicate thresholds for new traps contributing
- steady-state measurement
- applicable for low-doped or high-resistivity materials, complements DLTS



TAS: Arrhenius plots

- pn p-stop showed trap state similar to DLTS results
- standard pn-diode trap states differ from DLTS results
  - lower energy, lower cross-section

scan	E_{trap} [eV]	σ [cm²]
-1V pstop	0.311 ± 0.026	8.4×10^{-19} ± 3.1X
-2V pn	0.277 ± 0.043	1.0×10^{-16} ± 8.3X
-3V pn	0.168 ± 0.040	4.9×10^{-19} ± 6.2X
-4V pn	0.209 ± 0.037	3.3×10^{-18} ± 5.5X



Summary & Outlook

- DLTS and TAS measurements were successfully used to characterise traps in unirradiated diode samples
  - multiple trap states found
  - their trap levels + cross-section determined from Arrhenius plots
  - peak with 2 hole trap states common across all DLTS scans and samples
  - energy shift observed in ‘standard’ pn-diode, indication of field dependence of trap energy

Outlook:

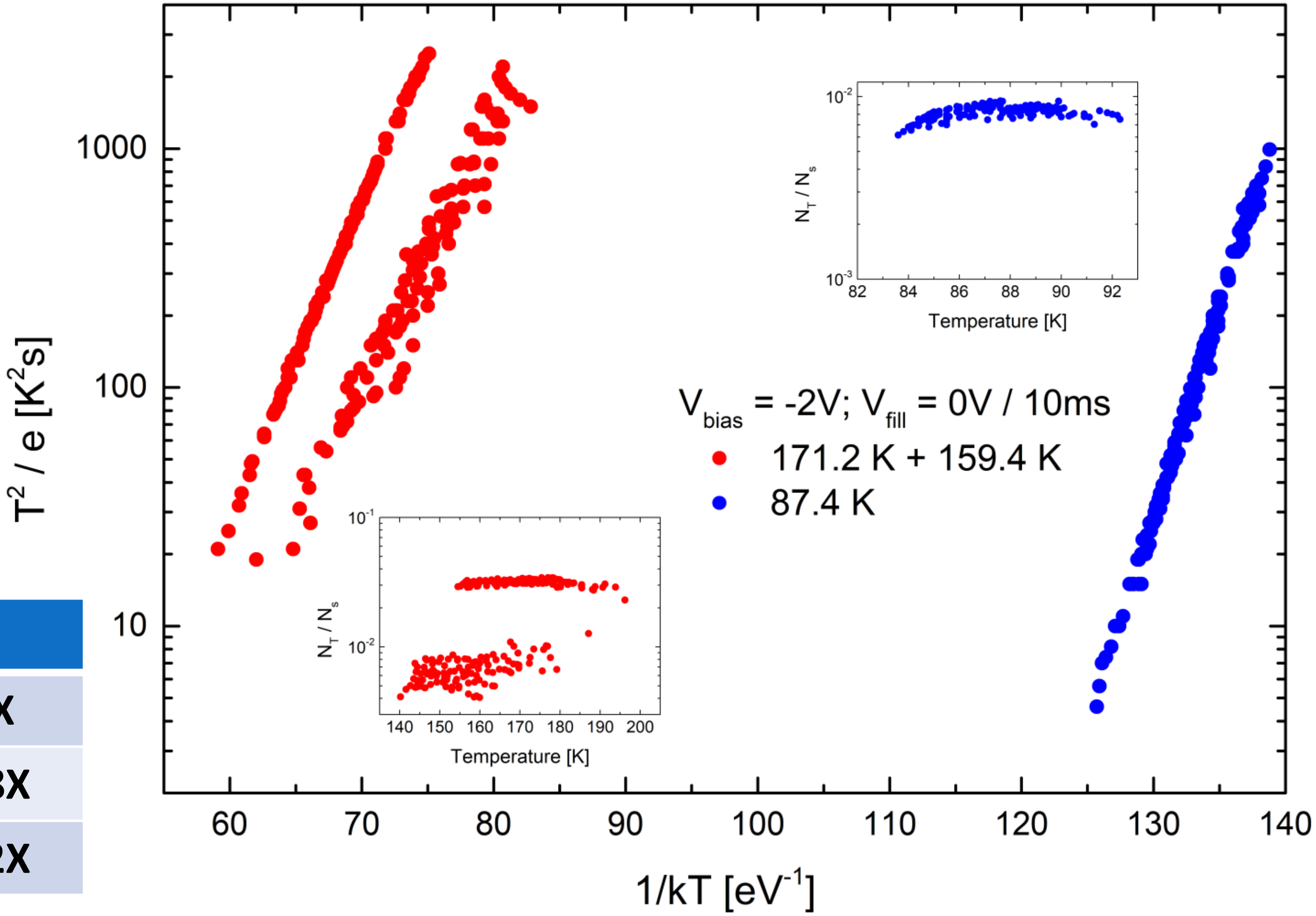
- further studies of observed traps for input in TCAD simulations
  - DDLTS for field dependent traps
  - filling pulse width dependence for capture kinetics
- DLTS measurements of Schottky diodes and irradiated samples

Backup

DLTS: Arrhenius plots

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels

T_{median} [K]	E_{trap} [eV]	σ [cm^2]
87.4	0.407 ± 0.005	9.4×10^{-1} ± 2.0X
159.4	0.255 ± 0.008	1.6×10^{-16} ± 1.8X
171.2	0.303 ± 0.003	8.4×10^{-16} ± 1.2X

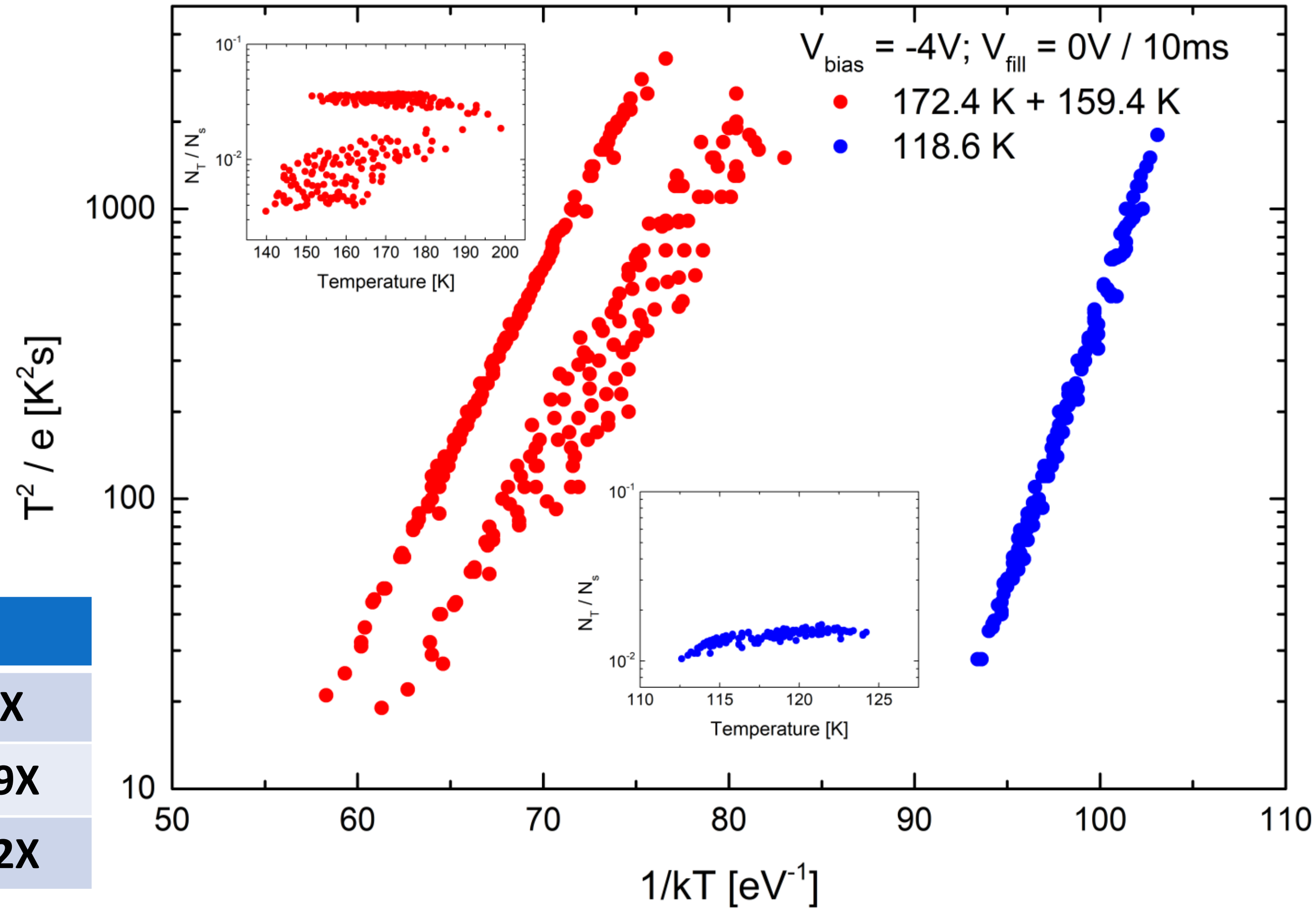


pn diode, no p-stop

DLTS: Arrhenius plots

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels

T_{median} [K]	E_{trap} [eV]	σ [cm²]
118.6	**0.442 ± 0.005**	**9.9×10^{-6} ± 1.6X**
159.4	**0.241 ± 0.009**	**4.7×10^{-17} ± 1.9X**
172.4	**0.296 ± 0.002**	**4.9×10^{-16} ± 1.2X**

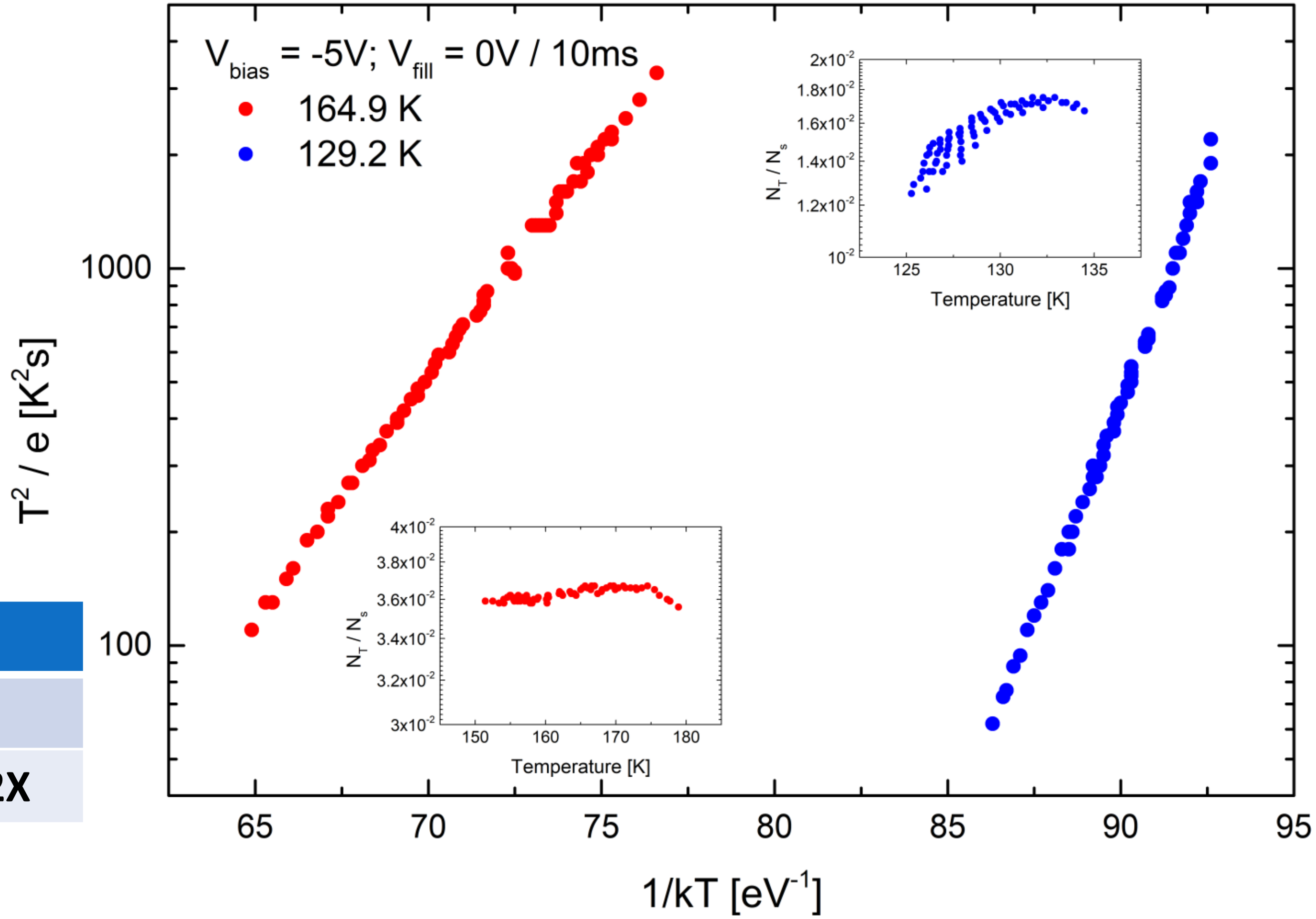


pn diode, no p-stop

DLTS: Arrhenius plots

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels
- low-T peak too close to 165K peak for good 2-Gaussian deconvolution

T_{median} [K]	E_{trap} [eV]	σ [cm^2]
129.2	**0.545 ± 0.007**	**$1x10^{-3}$ ± 1.9X**
164.9	**0.287 ± 0.003**	**$3.3x10^{-16}$ ± 1.2X**

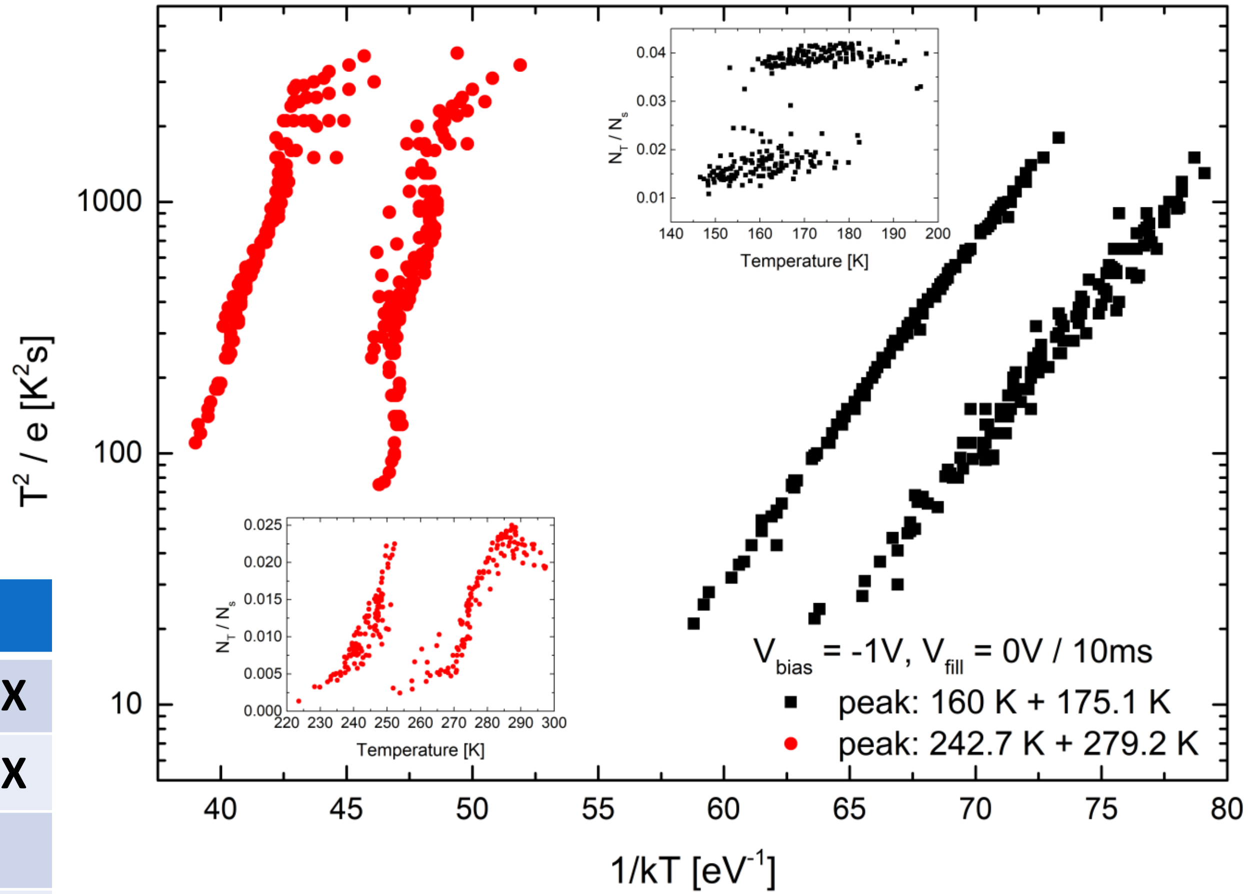


pn diode, no p-stop

DLTS: Arrhenius plots

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels
- filling pulse not yet optimised, fitting results not very precise

T_{median} [K]	E_{trap} [eV]	σ [cm^2]
160.0	**0.268 ± 0.014**	**3.0×10^{-16} ± 2.7X**
175.1	**0.309 ± 0.005**	**1.0×10^{-15} ± 1.4X**
242.7	**~0.999**	
276.2	**0.59 ± 0.04**	**2.4×10^{-14} ± 5.4X**

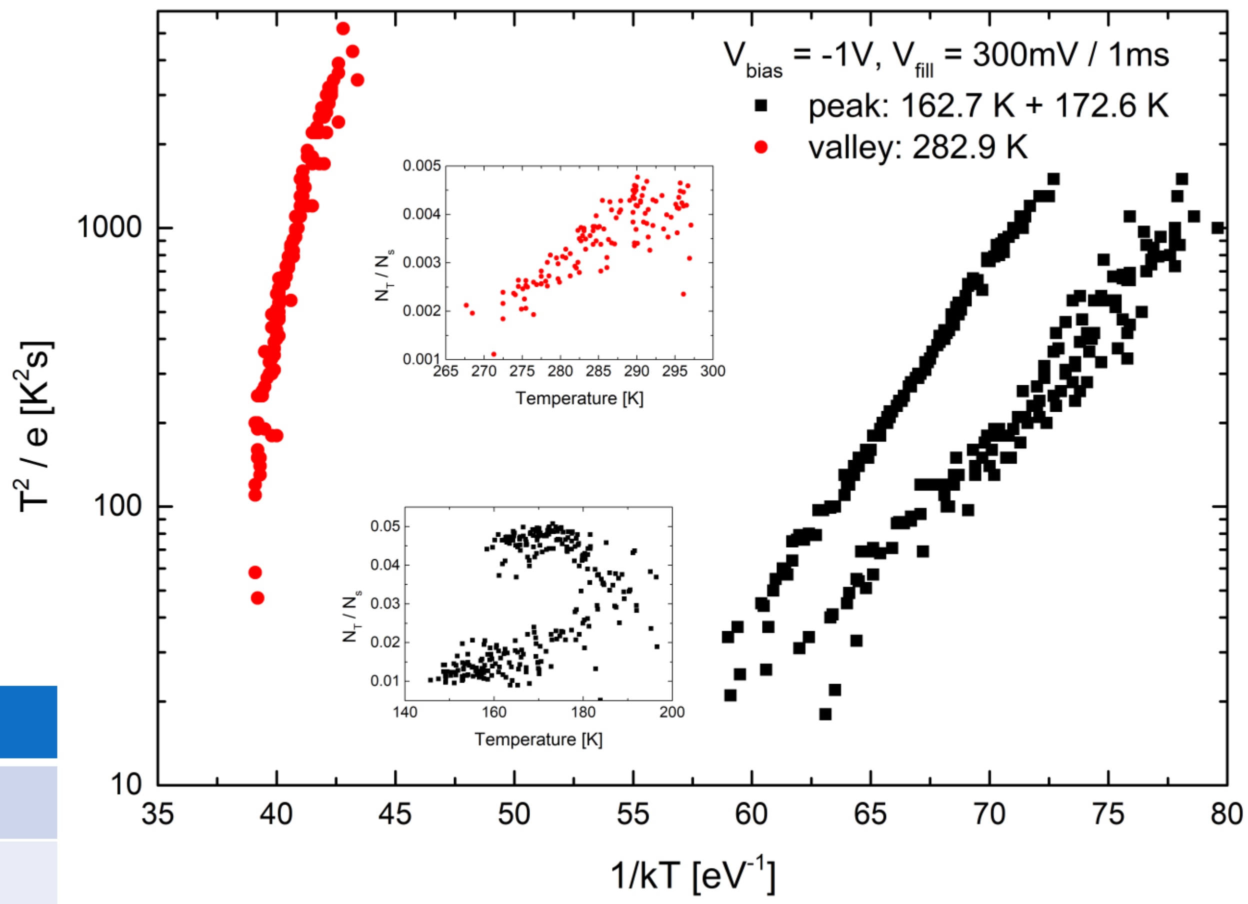


pn diode, with p-stop

DLTS: Arrhenius plots

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels
- filling pulse not yet optimised, fitting results not very precise
- forward bias filling pulse yields electron trap (‘negative‘ trap energy)

T_{median} [K]	E_{trap} [eV]	σ [cm²]
162.7	**0.217 ± 0.007**	**7.2×10^{-18} ± 1.3X**
172.6	**0.287 ± 0.004**	**2.2×10^{-16} ± 1.7X**
282.9	**-0.832 ± 0.037**	**1.8×10^{-10} ± 4.5X**

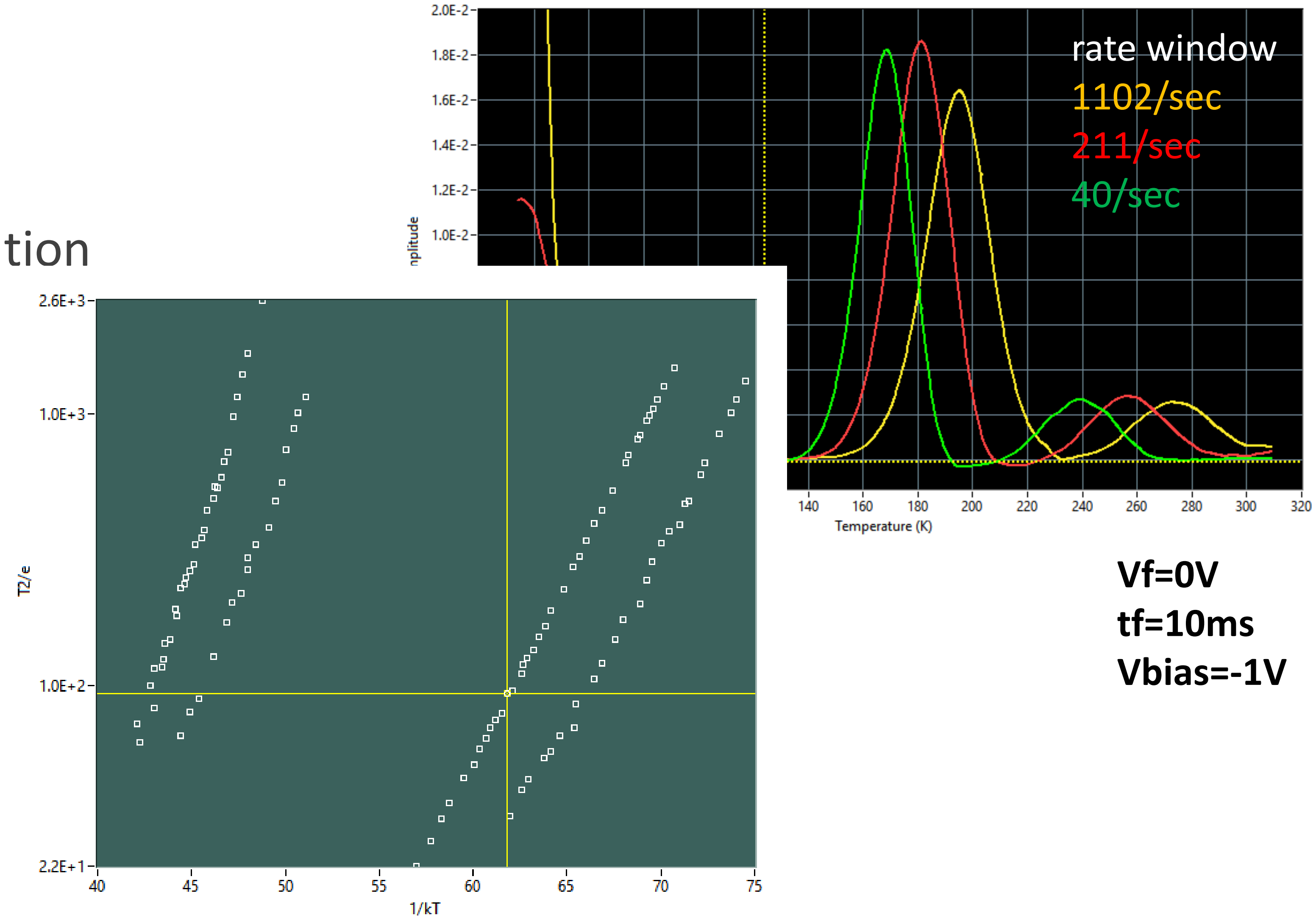


pn diode, with p-stop

DLTS: pn-junction diode @Semetrol 2020

DLTS spectrum:

- 2 maxima
- analysis with Gaussian deconvolution
  ⇒ peaks contain 2 traps each



Vf=0V
tf=10ms
Vbias=-1V

trap params from Arrhenius plot:

Midpoint temp (K)	E_t (eV)	Sigma (cm^2)	N_t/N_s
170.6	0.293	7.6E-16	9.7E-3
182.8	0.310	7.0E-16	2.1E-2
241.8	0.430	1.0E-15	7.6E-4
258.5	0.536	3.2E-14	3.5E-3

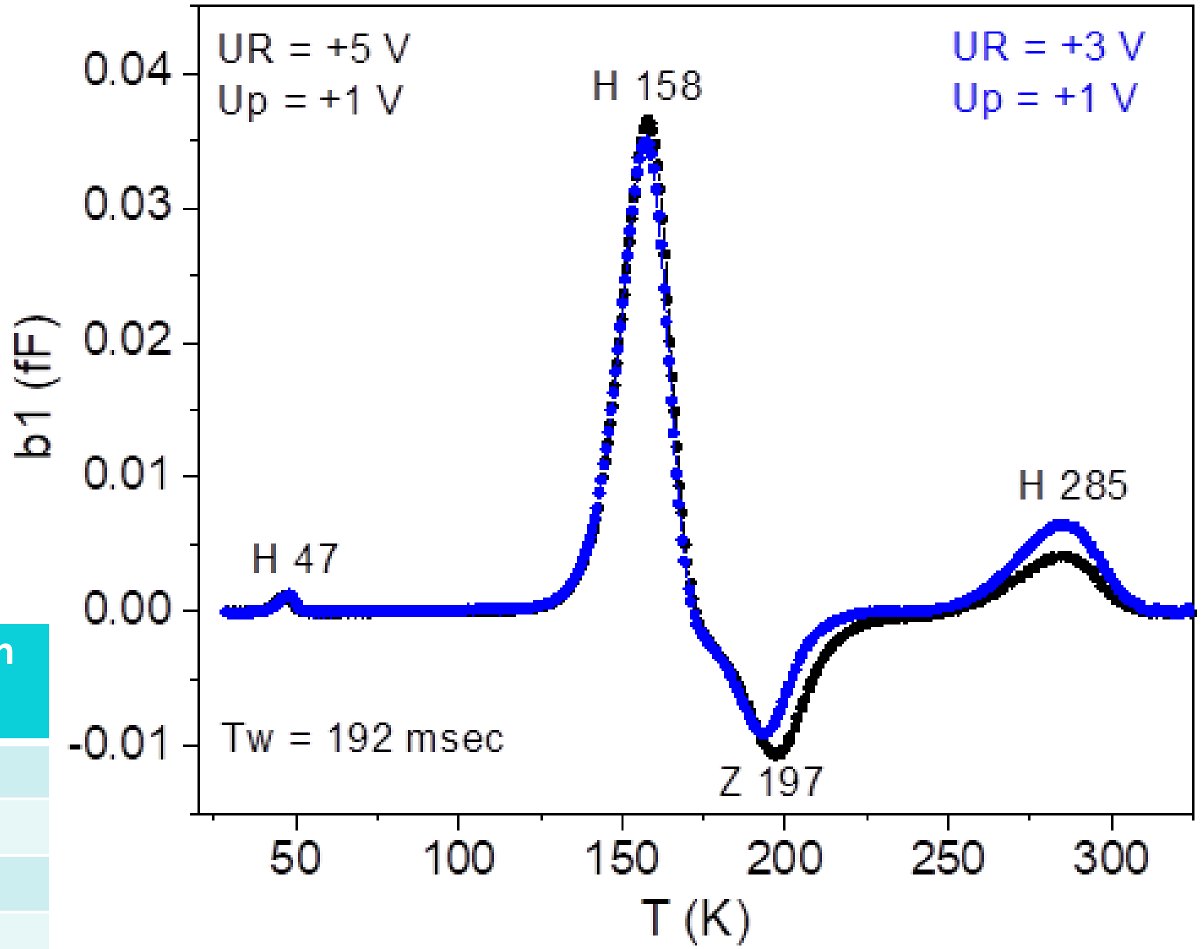
DLTS: Schottky diode @Bucharest 2020

DLTS spectrum:

- 3 maxima from hole traps
- 1 minimum, most likely from surface/interface states

trap parameters (Vbias=+5V; Vf=+1V):

Defect	Temp (K)	Ea (eV)	Sigma (cm2)	Defect concentration (cm-3)
H47	47	0.069	6.87E-17	2.49E10
H158	158	0.294	4.35E-16	9.32E11
Z197	197	0.439	1.85E-14	2.90E11
H285	285	0.611	3.76E-15	1.32E11

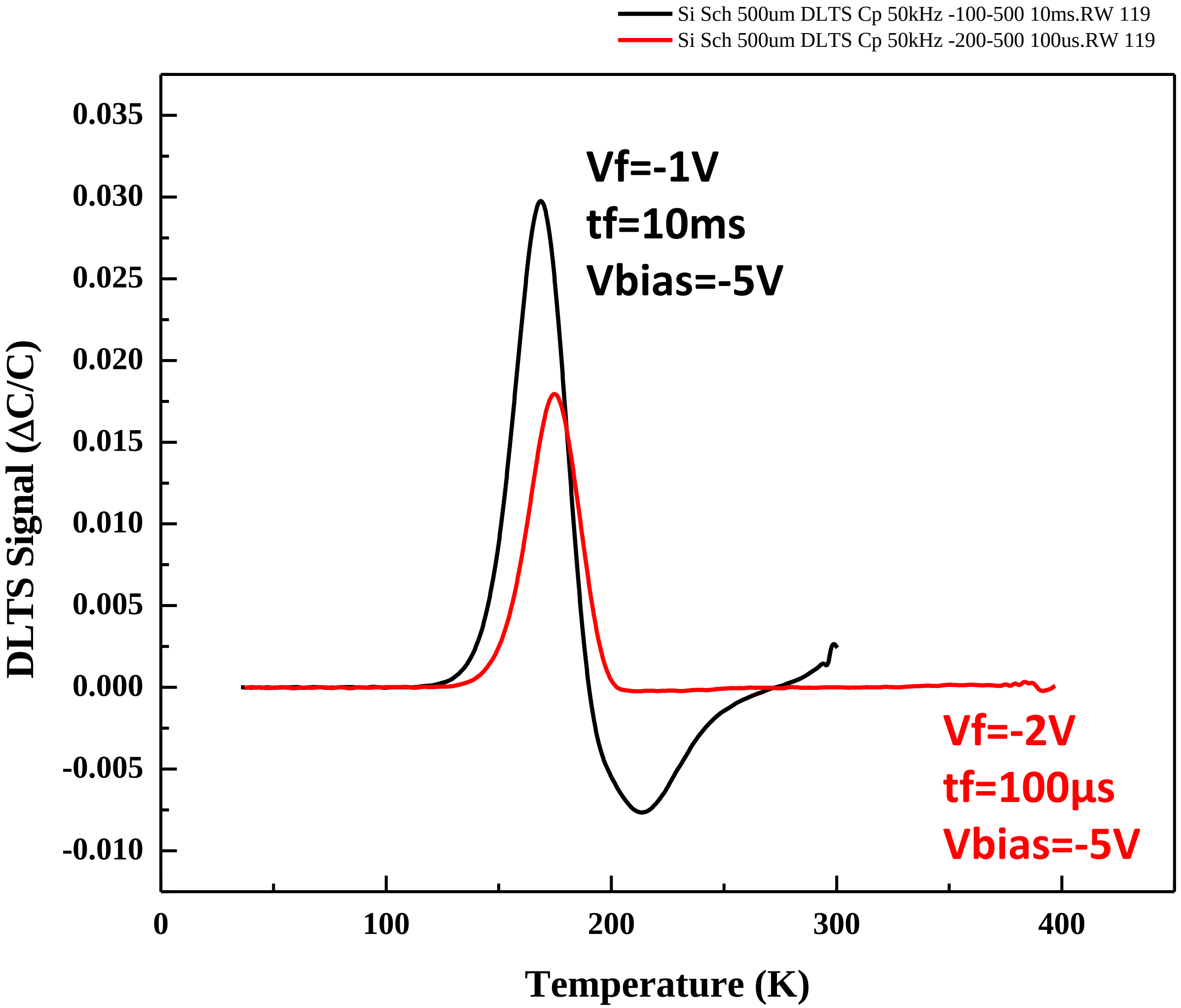


DLTS: Schottky diode @Semetrol 2020

DLTS spectrum:

- peak with 2 majority carrier traps
- ‘minority’ carrier trap
  ⇒ vanishes for reduced + shorter filling pulse
  ⇒ surface/interface states likely
- large majority carrier trap for larger filling pulses at room temperature

Midpoint temp (K)	E_t (eV)	Sigma (cm^2)	N_t/N_s
170	0.312	5.5E-15	7.8E-3
180	0.294	3.3E-16	2.2E-2



TAS @Semetrol 2020

TAS analysis:

- higher trap energy in Schottky for similar peak
- second Schottky trap near mid-gap
- energy shift at different test voltages
  - field dependence of trap energy
  - might explain difference between Schottky and pn-junction (higher E-fields in pn diode)

Sample	V_{bias}	E_t (eV)	σ (cm^2)
PN	-1V	0.384	1.1E-16
Schottky	-1V	0.498	1.6E-14
Schottky	-2V	0.467	3.0E-15
Schottky	-1V	0.664	3.5E-13
Schottky	-2V	0.614	3.7E-14