Tilman Rohe for the PSI-LTP-HEP-group

DMAPS-activities of the PSI HEP group

RD50-Meeting 24.06.2022

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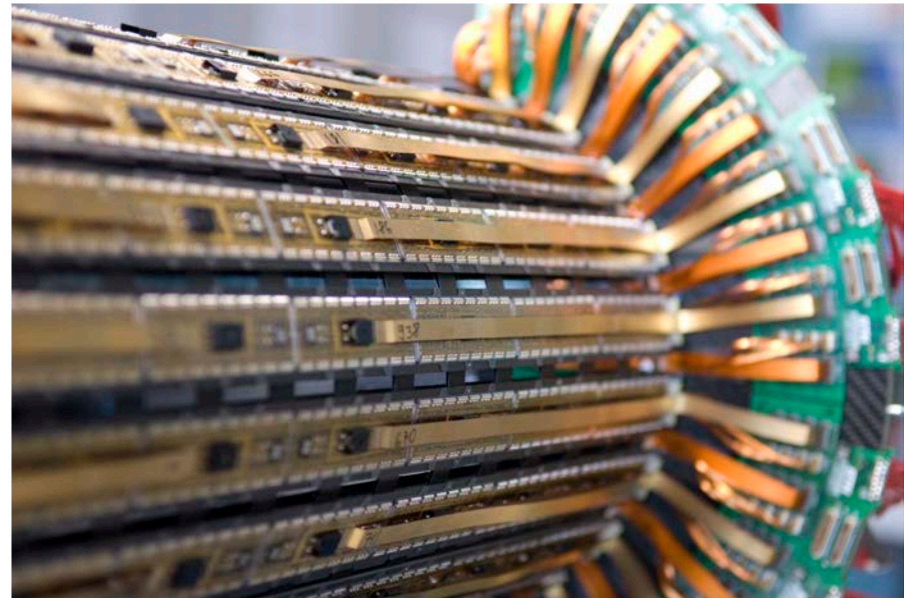
HEP group of the PSI-lab for particle physics

- HEP group is one out of 7 groups of the Lab for Particle Physics (other activities are theory, experiments at the PSI-accelerator (MEG, mu3e, ….), experiments with UCN (nEDM), detector development)
- Head of the group since 10/2020 is Lea Caminada (who leads in addition a group at UZH)
- Present staff: 5 scientists, 1 Postdoc, 2 PhD students (1 ETHZ, 1 UZH) + 1 technician
- Close collaboration with UZH (groups of Ben Kilminster and Florencia Canelli) and ETHZ (group of Rainer Wallny)
- Record
  - Development and construction of hybrid pixel detectors
    - CMS pixel barrel P0
    - Lead institute in the construction of pixel barrel P1
    - Replacement of L1 (2021)
    - Building Tpix modules for Phase2
- Competences
  - Chip design
  - In house bump bonding
  - Sensor design
  - Integration
  - System architecture (readout systems, testing, …)

  → Most of them are also useful for development of monolithic pixels



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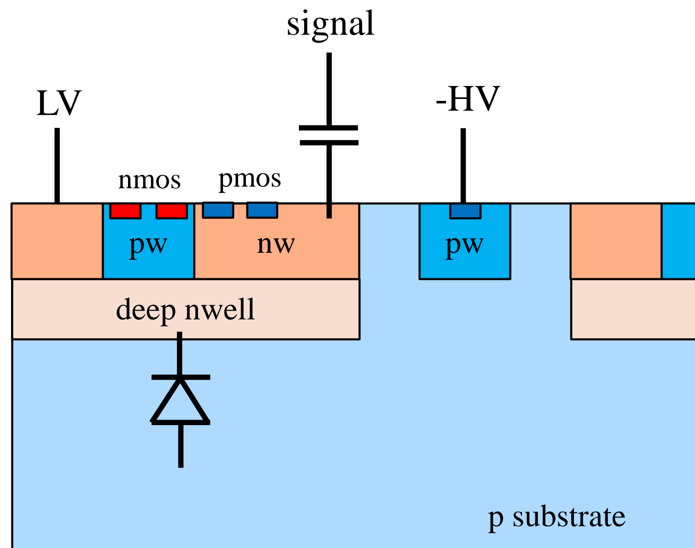
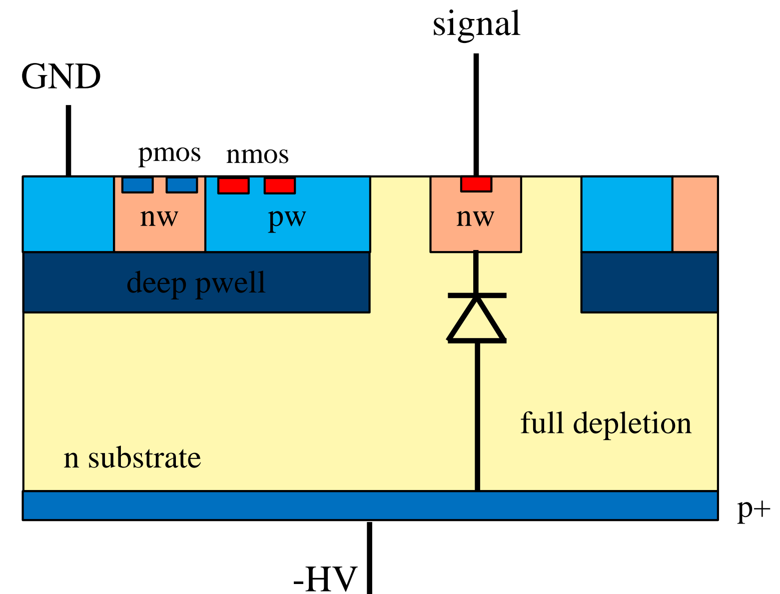
DMAPS activities

- Started work on DMAPS in 2018
  - Evaluated several technologies. Now following 2 with own chip submissions.
- Short/medium term aims
  - Gain experience with DMAPS
  - Gain experience with ToA measurements (in close collaboration with UZH)
    - Possible development of a (hybrid) timing chip for use in CMS (Phase > 2)
  - Combine the two above
- Possible projects
  - PSI experiments with moderate timing requirements (roughly 0.1-1ns)
    - Data rate low
    - Basically no radiation hardness required
  - Check the radiation harness of the used processes (in case there is funding)
    - Is in principle already done by others
    - No mid term DMAPS project in CMS
    - Can be considered as RD50 activity by potential funding agencies
    - Chips might be used as beam monitors at secondary beam lines at PSI

Technologies





Large fill factor (area of collection electrode)

- Large sensor capacitance
  - higher noise, power needs
  - slower signals → - for timing
- Shorter drift paths, homogeneous electric field → +for timing, + rad hardness
- X-talk issues from electronics into collection node (improved by an isolated n-well)

TSI (180nm), AMS, LFoundry 150

TSI → Share submissions with KIT (I. Peric)

Small fill factor

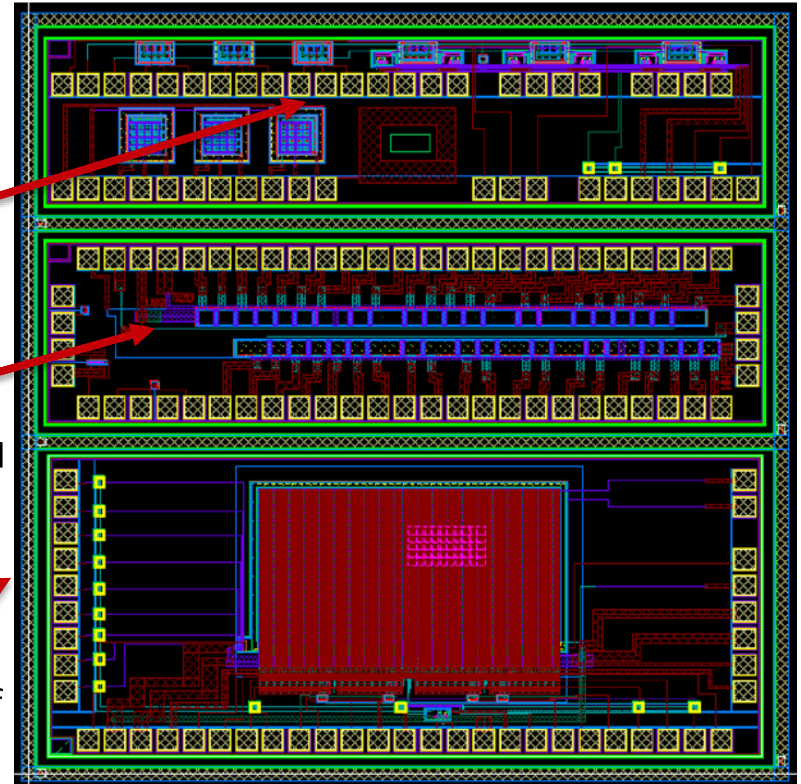
- Small sensor capacitance
- less noise, power needs
- Fast and larger signals → ++ for timing
- Longer drift paths and low field regions → -for timing, - rad hardness
- Need to find new ways to form fields

LFoundry 110, ESPROS, TowerJazz

LF110 → Collaboration with Arcardia, INFN Torino

TSI

- 180nm HV (includes devices up to 120V) derived from former IBM/AMS process
- Fab located in California
- «Convenient»: Regular MPWs, relatively cheap, turn around < 3 month, **extraordinary good communication**, willing to respond to special wishes (**accept high resistivity wafers**, discuss process modification like **isolated n-well**).
- 1st 5 x 5 mm^2 **MPW** test chip (on standard substrate) received in May 2020
  - Sensor test structure
  - Transistor test structures for characterization of enclosed transistors and measuring of radiation hardness
    - Some structures irradiated at RBI up to 45Mrad
    - Measurements ongoing
  - Small MAPS chip ("R4S-like") with 20x40 pixels with several options for preamp
    - Cal-injections used to choose to final version of the preamp
    - Actually see betas from Sr-source

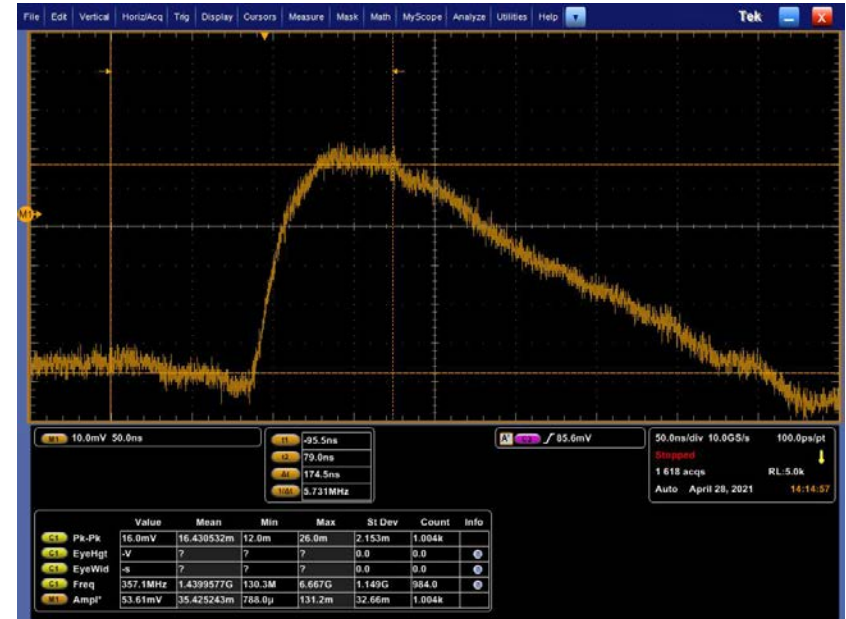


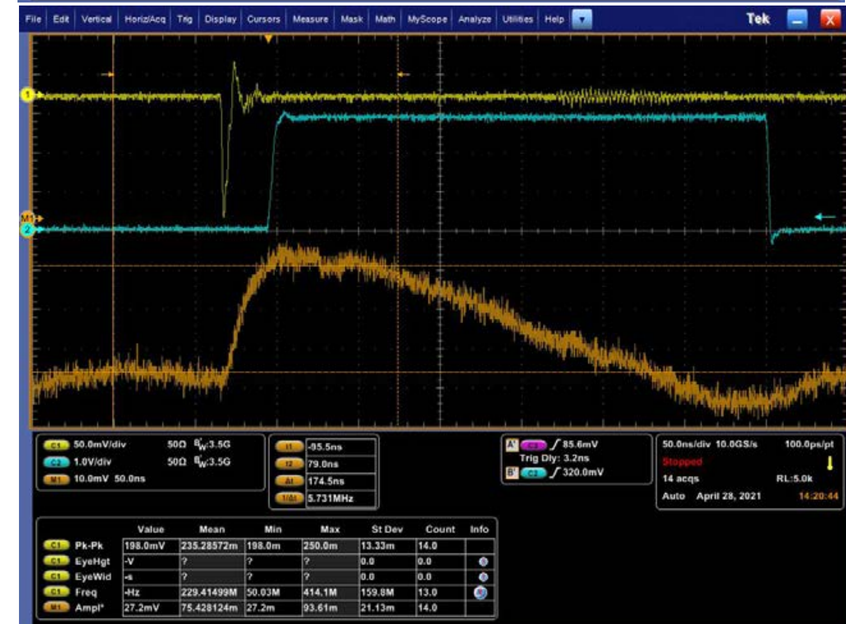
Signals from Sr-90 source

- Set R4S in «transparent» mode
  - Special dtb firmware with «hold» signal always released
- Program 1 pixel
  - Very small sensitive area (50 x 50)
  - More not possible as base lines would add
- Send analogue R4S output through the dtb to a scope
- Trigger with scope

Results

- Very small rate (1Hz)
- If in addition a signal in the scintillator is required → rate goes down to some events per minute
- Signal does not depend on bias voltage
- Conclusion
  - By far most pulses come from low energetic beta particles
  - Signal from «high» energetic particles are usually too small



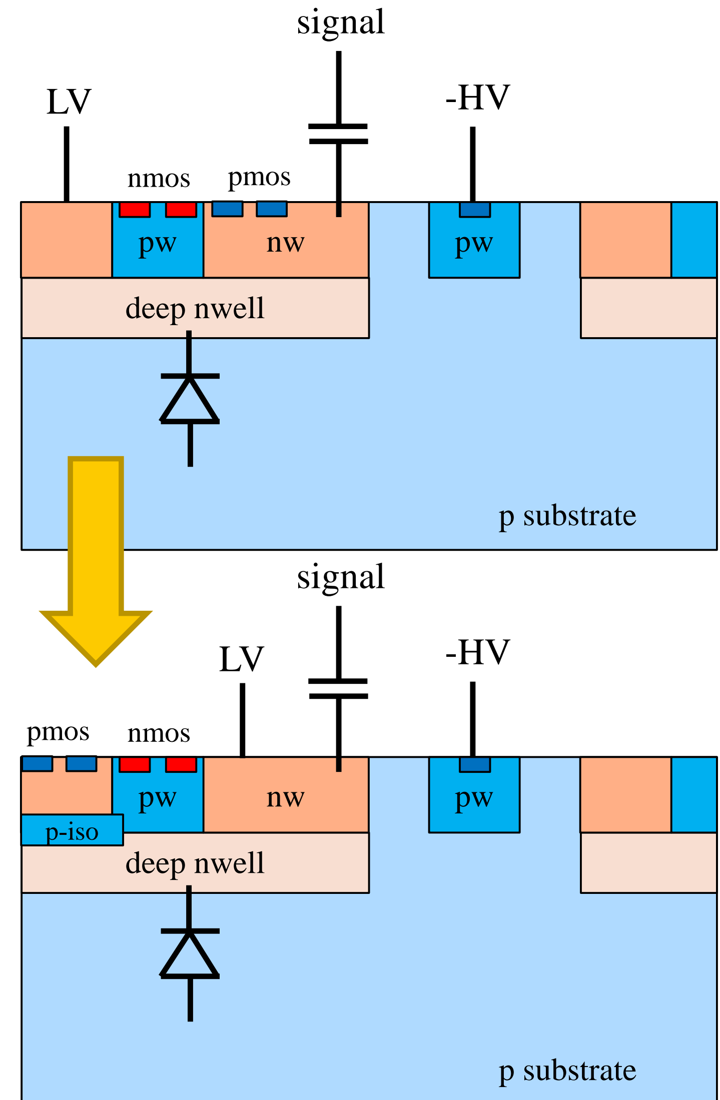


Prototyp run: technology options

- Prototype run shared with KIT submitted 11.06.21
- Standard plus 2 types of high resistivity p-type silicon

Res [Ωcm]	10V	50V	120V
20	5 um	10 um	16 um
200	15 um	33 um	50 um
5000	75 um	160 um	250 um

- Extra implant to create «isolated n-wells» (process modification)
- pMOS transistors in pixel cell possible
- Higher capacitance
- Different “experimental” (design rule violating) HV structures



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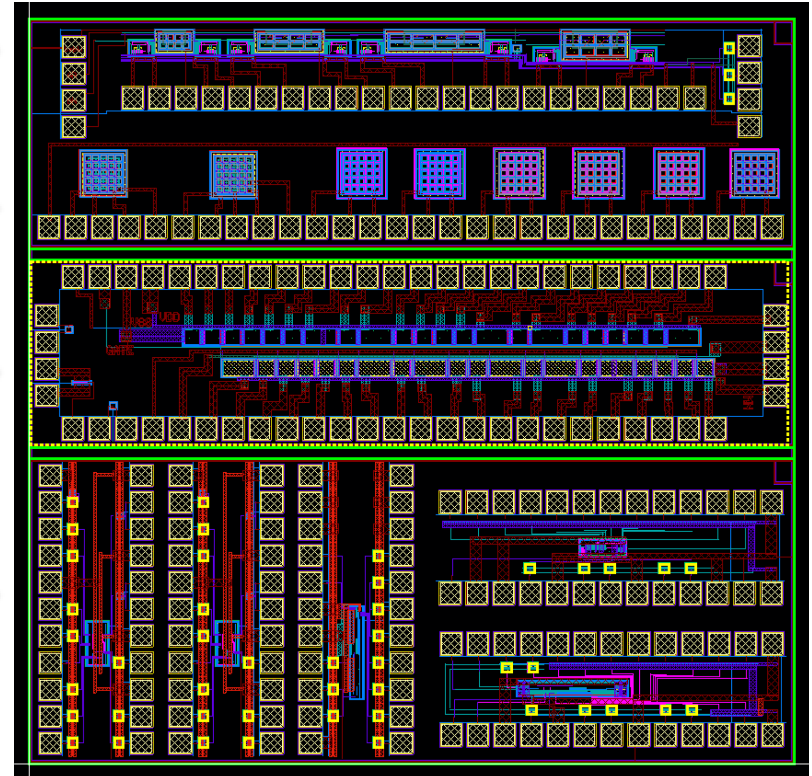
Prototype run: test structures

- Sensor structures with amplifiers (laser and source measurements, edge TCT)
- Small pixel matrices with experimental (DRC violating) edge termination
- Transistors (PMOS in isolated n-well)
- PLLs, I2C, ADC, DAC



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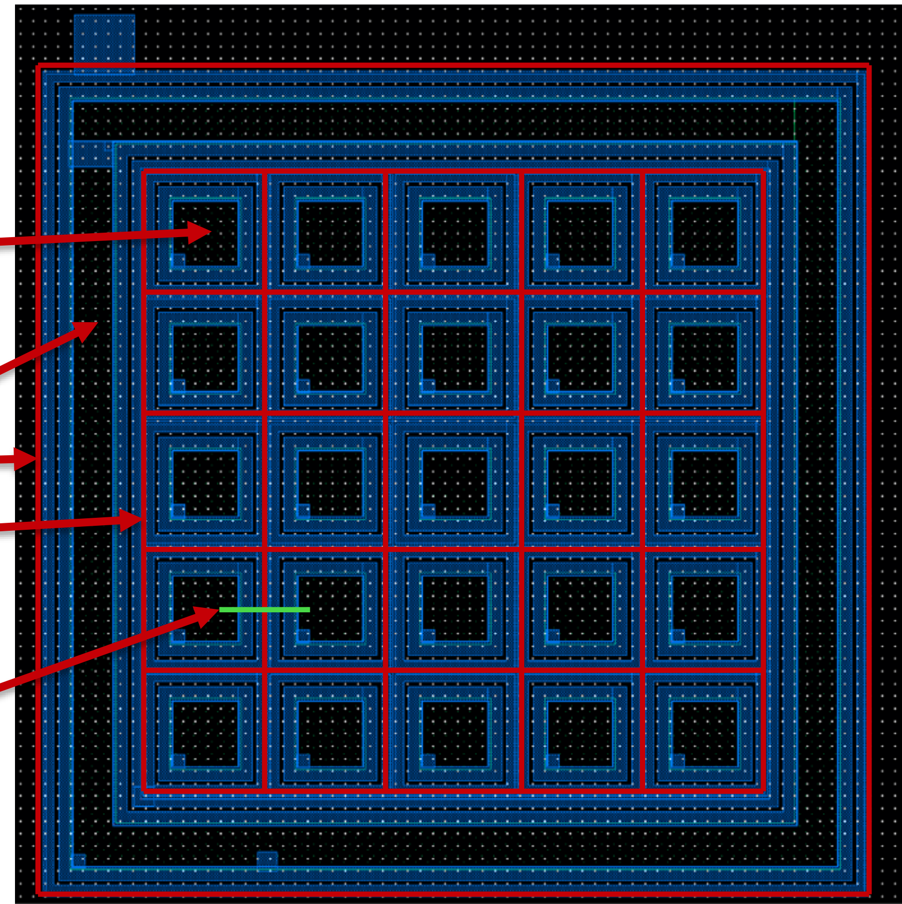
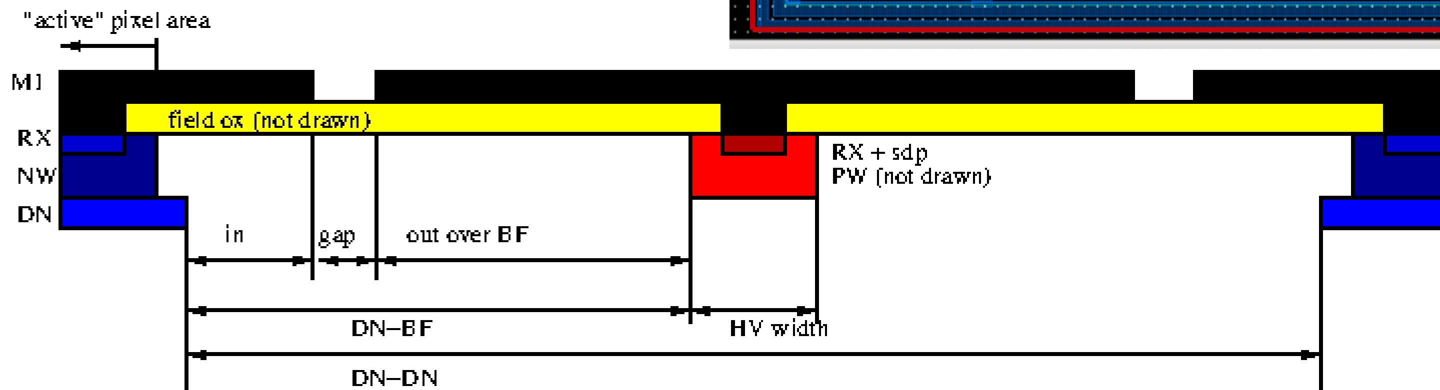
Pseudomatrices

- 5 × 5 pixels
  - Shorted (DP)
  - No circuits inside
- Closed DP-well surrounding all pixels (GR)
- HV-connection
- “inner” HV connection (extra pad)
- Layouts 1-8 differing mainly in the HV termination (No 3+4 have a larger Gap DN-DN)

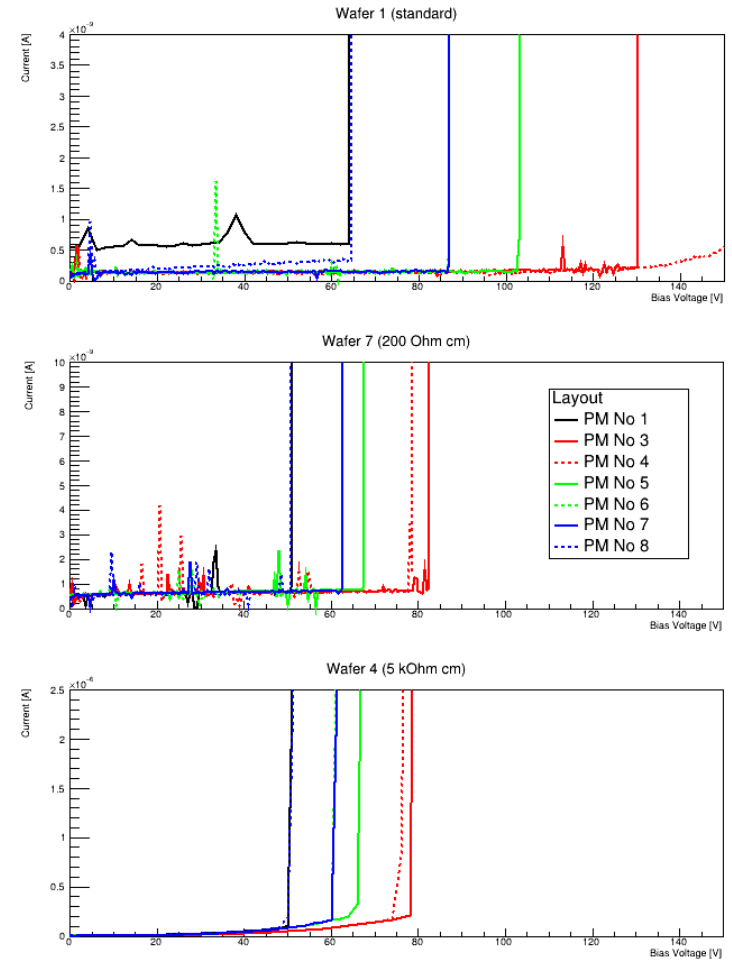




IV measurement – both HV pads connected

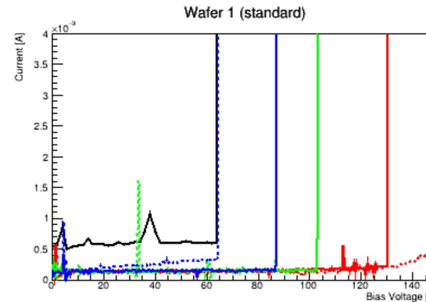
This configuration tests the HV capability of the inter pixel region

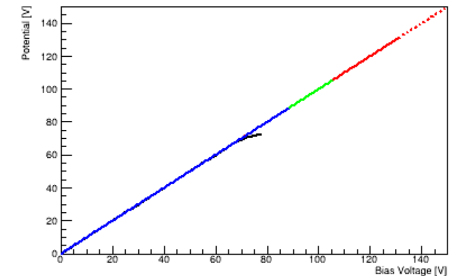
- Designs 3+4 are always best due to the larger gap
- In the standard substrate #4 is the best due to large field plates directed outwards combined with the low depletion depth
- All «experimental» designs (>1) are better than «standard» (1) due to the larger gap (DN-BF)
- When the region between HV and DN is depleted at al low voltage, the space charge has little impact ($V_{breackdown}$ is the same for 200 and 5000 Ohm cm)
- Fieldplates mainly directed outwards seem not of advantage anymore (3 and 5 are only slightly better than 4 resp. 7)

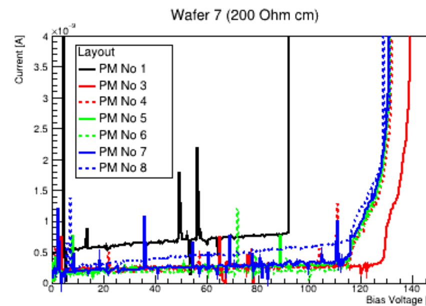


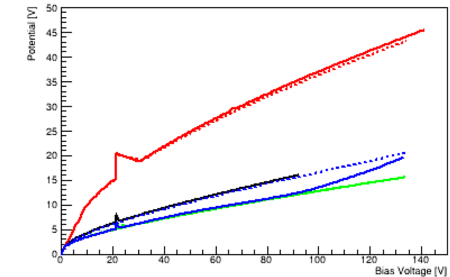
IV measurement – inner HV floating

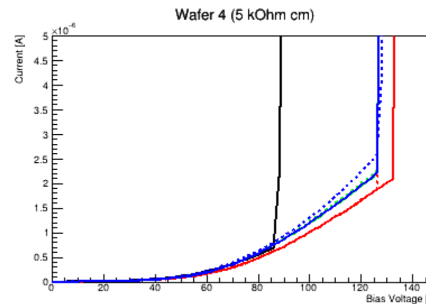
- Standard substrate: curve identical due to ohmic path through the substrate, inner HV follows outer perfectly
- High ohmic substrates:
    - Inner HV is pinched off
        - #3+4 have larger gap
    - Breakdown is determined by outer structure (identical for all but PM 1)
- Adjustment of «inner» HV:
    - "inner" HV can be connected and ramped to higher voltages → charge collection
    - Max value as shown on p10

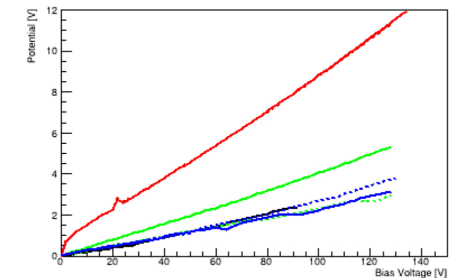


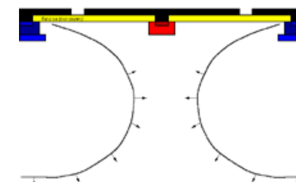












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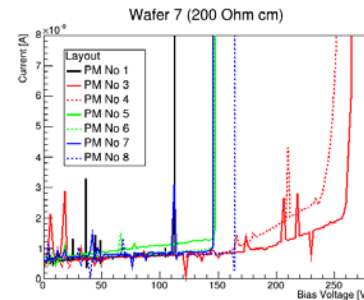
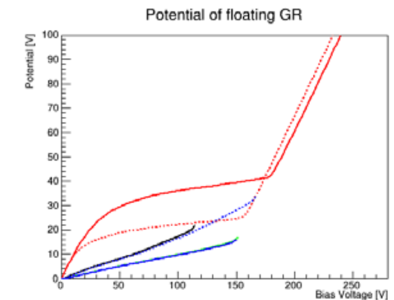
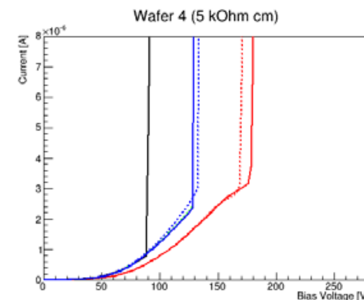
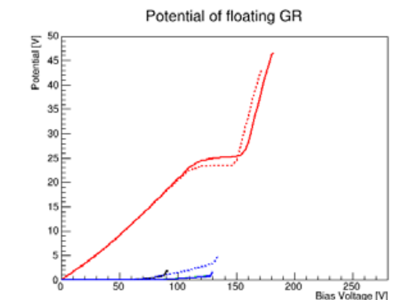
IV measurement – inner HV + GR floating

- Not practical in real device as GR cannot be filled with electroics.
- Standard substrate: measurement makes no sense
- High ohmic substrates:
    - Vbd shifted by ~ 2 × GR voltage
    - Designs 3+4 with large gaps have the strongest effect







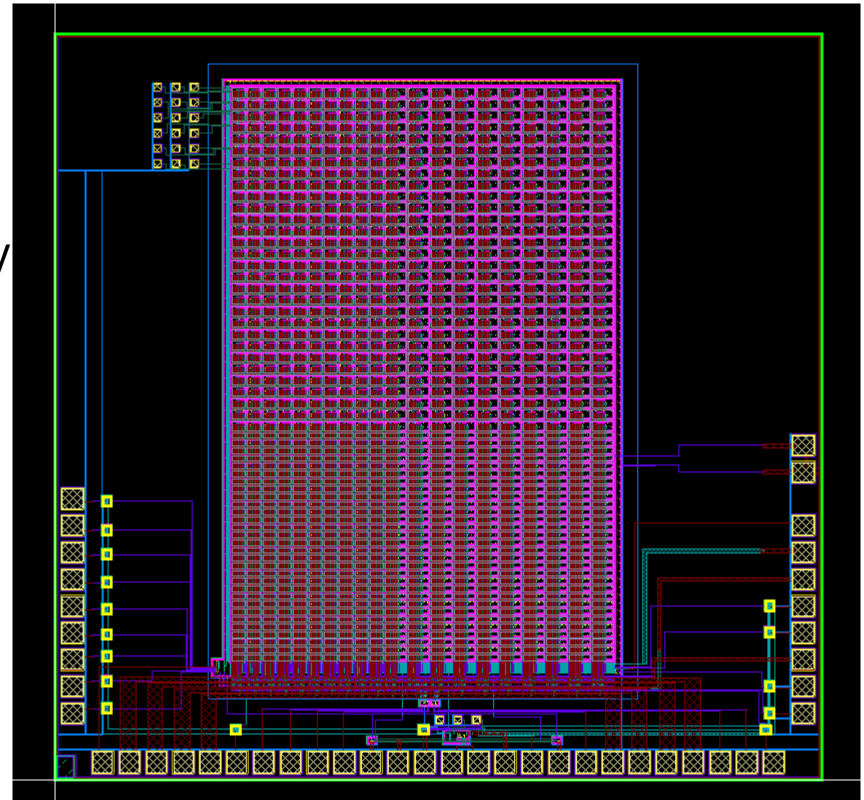


Conclusions

- High ohmic substrates need adapted HV terminating strategies
- A closed ring around the chip is of great advantage (but might be forbidden by DRs)
- Focus on HV stability of the outermost edge (like in a “normal” pixel sensor)

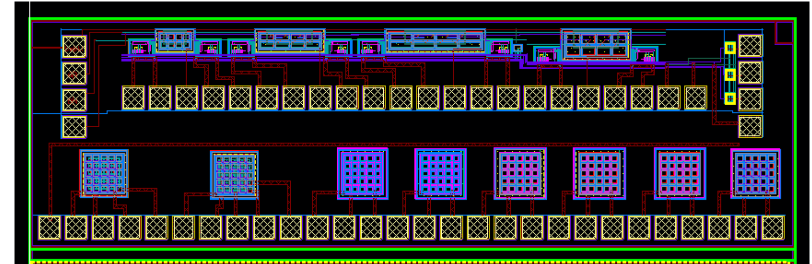
Prototype run: pixel chip

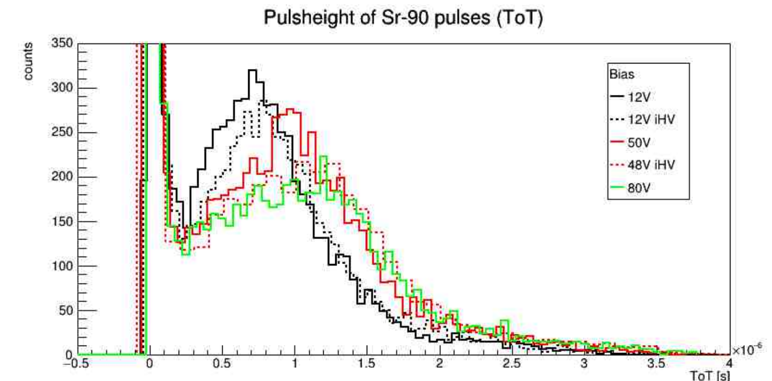
- One pre-amp option chosen
- 4 different pixel sizes (50x100, 50x150, 75x100, 75x150)
- Discriminator in each pixel with 3 trim bits (in isolated n-well)
- Internal hold with programmable delay
- External hold possible (R4S-like operation)
- Trigger output (pixel-OR)
- Chip works fine but does not detect particles due to a trivial bug
- Smaller version with pixel sizes of 50x100 and 50x150 resubmitted parasitic in a run of KIT (I. Peric)
- Testbeam at DESY planned for late Nov. 2022

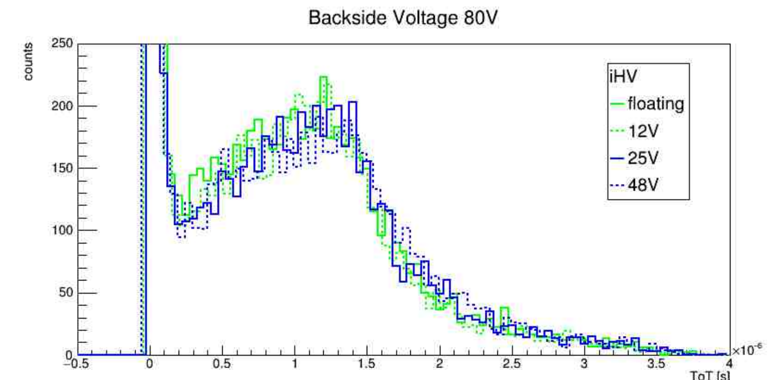


Measurements with “TCT” structures

- 2 Pixels per array have a strong and fast amplifier
  - Can directly be read out with a scope
  - Only “standard” HV-connection limiting bias
- Sr-90
  - Little bias dependence of signal height
  - Charge collection not too much influenced by “inner HV” (in case of time critical measurements this might change)
- Laser measurements with set-up at UZH are planned soon







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Modified LF110

LF110 process modified by INFN-Torino

- Back side implant (diode)
- Diode edge termination with multi guard rings (for 100 and 300 µm wafers)
- Special n-type substrate
- Thinned wafers (300, 100, 50 µm)
- Charge collection node designed by Arcadia collaboration (Lucio Pancheri, Coralie Neubüser, Trento)

First submission as MPW in LF110 (without modifications). Chips received mid 2020

- Transistors (enclosed and linear)
- 2 types of TDCs
- PLLs
- DACs
- Different types of ring oscillators and inverter chains

LF110 - Motic

Monolithic **ti**ming **c**hip

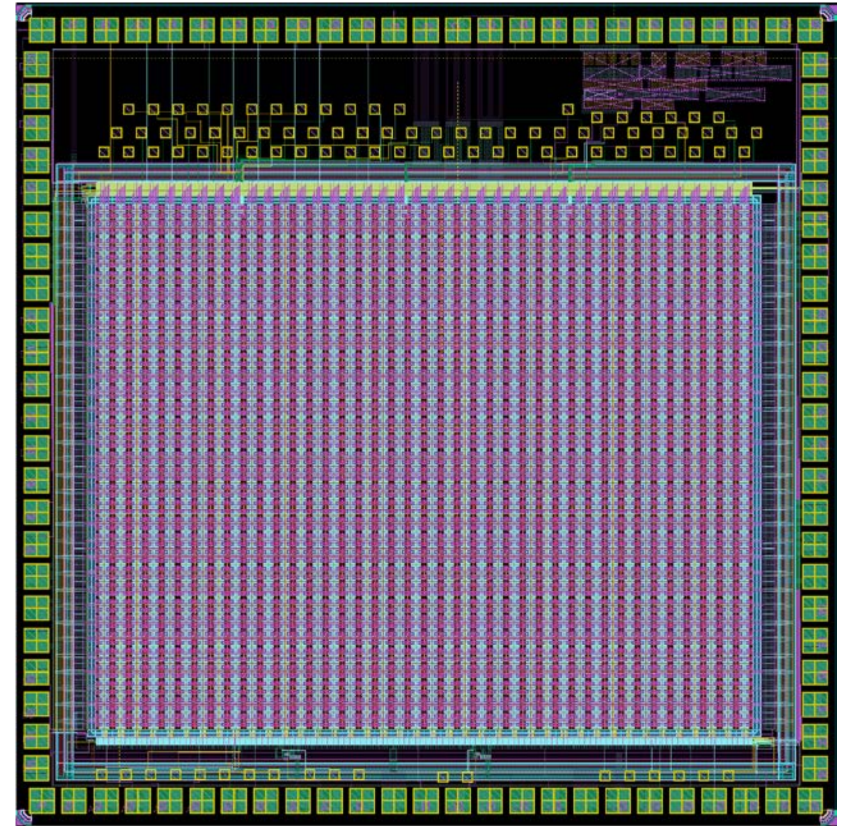
- Pulse height and **time of arrival** is measured
- Two chips of 5 x 5 mm^2: MoTiC A (with varying preamplifiers) and MoTiC B (with collecting electrode variations including 1 AC coupled option).

Additional test structures:

- TCT for all sensor flavours
- Bricked TCT pixel with and w/o comparator
- AC bias diode
- TDC oscillator

Status

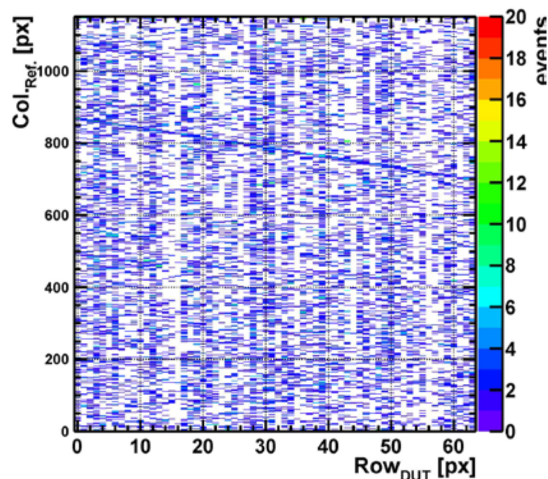
- Parts delivered Autumn 2021
- 1st test beam at DESY April 2022



Motic A

Test beam at DESY

- Very first test beam with new chip AND new test system
- Learned a lot
  – Chip features
  – Test system/Software
- Detected tracks on very last day …
- Data analysis is ongoing
- Next beam time in July 2022
- Chip resubmitted with features understood corrected (June 2022)



Conclusions

Experience from development and construction of hybrid pixel detectors is useful for MAPS development

Two technologies with different flavours (large/small fill factor) are presently followed

First pixel chips in both flavours are available and first results presented

Test beam campaigns at DESY planned in July (LF110) and November (tsi180) this year

Applications within PSI envisaged

No experiment for our group recognised, yet, requiring radiation harness and high data rate apart from beam instrumentation