Discussion
Defect Characterization

Defect and Material Characterization

- **Collaboration on "acceptor removal"** in p-type Si: Bucharest, CERN, Minsk, Hamburg, CiS formed (TSC, DLTS, HRTEM, PL)
- **project**: *Schottky diodes on Epitaxial Silicon for Radiation Damage Characterization of CMOS MAPS* : (RAL, Giulio Villani)

Defect and Material Characterization

- Main activities
  - Detection and microscopic characterization of standard and material engineered silicon via dedicated techniques (DLTS, TSC, TDRC, SIMS, ICP-MS, PITS, FTIR, TCT, EPR, HRTEM, PL, fluorescent centers)
  - Identification of electrically active defects induced by irradiation responsible for trapping, leakage current, change of Neff , change of E-Field
  - Studying possible application for radiation hardening
  - Deliver input for device simulations (e.g. TCAD) to predict detector performance under various conditions
- Milestones [2018-2022]
  - WP 1.1 Electrically active defects in p-type silicon [7 MS]
  - WP 1.2 Microstructural Investigations on extended and clustered defects [4 MS]
  - WP 1.3 Theory of defects and defect kinetics modeling [5 MS]

- finished
- started
- not yet started

WP 1.1. Electrically active defects in p-type silicon

M2: Determine defect annealing behaviour in STFZ and engineered silicon. Correlation with device performances (**Q4/2019**)

M3: Determine defect transformations and kinetics in STFZ and engineered silicon after treatments at high temperatures (between 150 °C and 350 °C). Correlation with the device performance (**Q3/2020**)

M4: Identify the role of impurities in the formation of defects impacting on device performance **(Q1/2021)**

M5: Detection/characterization of radiation induced defects in LGAD and HV-CMOS (test structures fabricated through the RD50-2021-04 common project) via sensors based on STFZ and defect engineered p-type silicon, establish the annealing behavior (annealing at 80°C), correlation with electrical performance of the devices **(Q3/2021)**

M6: Validity tests on optimized material engineered sensors (pads, LGADs and HV CMOSs). Comparison between prediction and experiments (Q1/2022)

M7: Validity tests on finally optimized material engineered sensors (pads, LGADs and HV CMOSs) (Q3/2023)

WP 1.1. Electrically active defects in p-type silicon

- finished
- started
- not yet started

Status: As irradiated – several type of diodes (FZ, CZ, EPI), several type of irradiations (e, n, p)

- High fluences (CV, IV, TSC and HRTEM):
  - STFZ, EPI and CZ PiN diodes, different resistivities, CERN, Hamburg and Bucharest
  - HRTEM on highly neutron irradiated samples ($10^{17}cm^{-2}$ and 10^{19}) (done in Bucharest)
  - LGADs – by TSC (still ongoing)
- Low fluences (CV/IV and DLTS):
  - electron irradiated EPI PiN diodes (Minsk, CERN and Hamburg) (ongoing)
  - neutron and proton irradiated EPI, CZ and FZ PiN diodes (CERN, Hamburg and Bucharest)
  - **DLTS on LGADs not work – PiN samples mimicking the gain layer might be a good solution for characterizing the gain layer**

Annealing studies (DLTS, TSC, HRTEM)

- at 60 / 80^0 C – TSC, partly done for hadron irradiation (EPI 50 ohmcm at Hamburg), DLTS (Bucharest and CERN); at T > 150 C – done on electron irradiated samples (DLTS, Minsk), on proton and neutron irradiated PiN samples in Bucharest (DLTS) and at Hamburg and CERN (TSC) , still ongoing.
- HRTEM on highly neutron irradiated PiN samples (in Bucharest)

- finished
- started
- not yet started

WP 1.2. Microstructural Investigations on extended and clustered defects

M1: Microstructural characterization of the radiation induced clustered defects (fluences between 10^{15} and 10^{17} n_{eq} cm^{-2}) and monitoring of the evolution of clusters at 80 °C **(Q3/2019)**

M2: In situ- annealing studies at 5 temperatures (between 150 °C and 350 °C) in order to determine the structural transformations of the extended and clustered defects (Q3/2020)

M3: Microstructural characterization of the oxide semiconductor interface in irradiated LGADs and HV CMOS devices, time evolution at 80 °C **(Q3/2021)**

M4: Microstructural characterization of the oxide semiconductor interface in irradiated optimized LGADs and HV CMOS devices **(Q3/2022)**

Status:

- HRTEM on STFZ PiN diodes and LGADs (CNM), fluence 10^{15} n/cm^2, and annealing up to 240 C, in Bucharest (2019)
- HRTEM on LGADs (fluence ~$10^{19}$$cm^{-2}$) in Bucharest

- finished
- started
- not yet started

WP 1.3 Theory of defects and defect kinetics modelling

M1: Modelling of the detected defect generation/kinetics and of the impact on the device performance corresponding to annealing treatments at 80 °C (Q3/2020)

M2 : Modelling of the detected defect generation/kinetics and of the impact on the device performance corresponding to annealing at temperatures between 150 °C and 350 °C and final assessment of the role of the intentional added impurities **(Q1/2021)**

M3 : Identification of the optimal impurity concentrations for pads, LGADs and HV CMOSs as input for production. **(Q3/2021)**

M4 : Improvements of the developed models according to validity test foreseen at WP.1.1 - M6 and provide new optimization solutions for WP.1.1-M7 **(Q3/2022)**

M5 : Validity test for the developed theoretical models based on the results obtained on WP.1.1 - M7 optimized sensors **(Q3/2023)**

Status:

– ongoing with the BiOi generation rate “puzzle”, A&B configurations, B, P and C content

Thoughts

- **Acceptor removal**
  - Need to parametrize, if possible, the multiple reasons for the strong variations of gBiOi or gB_sSi_i – donors containing Boron. Combine the "macroscopic" acceptor removal models (i.e. parameterization of the c parameter) with the formation of defects (i.e. BiOi or B_sSi_i introduction rates)
    - $g_B=2g^A+g^B$, where g^B is unkown yet!
  - Need to know the impurity content by SIMS in the samples
  - Need DLTS/TSC on CMOS sensors and DLTS for characterizing the gain layer in LGADs
  - Need to link observations (acceptor removal) on LGADs, CMOS and p-type pad sensors with the defect formation (TSC, DLTS,..) measurements

Thoughts

- **RD50 new project proposal: Defect engineering in PAD diodes mimicking the gain layer in LGADs**
  - **SIMS for impurity content**
  - **Different levels of Carbon implantations**
  - **Allows microscopic investigations (DLTS)**

Valentine Sola:

To increase radiation tolerance of the LGAD gain layer we concurrently implant p^+ and n^+ dopants in the gain layer volume

→ Use the interplay between acceptor and donor removal to keep a constant gain layer active doping concentration