

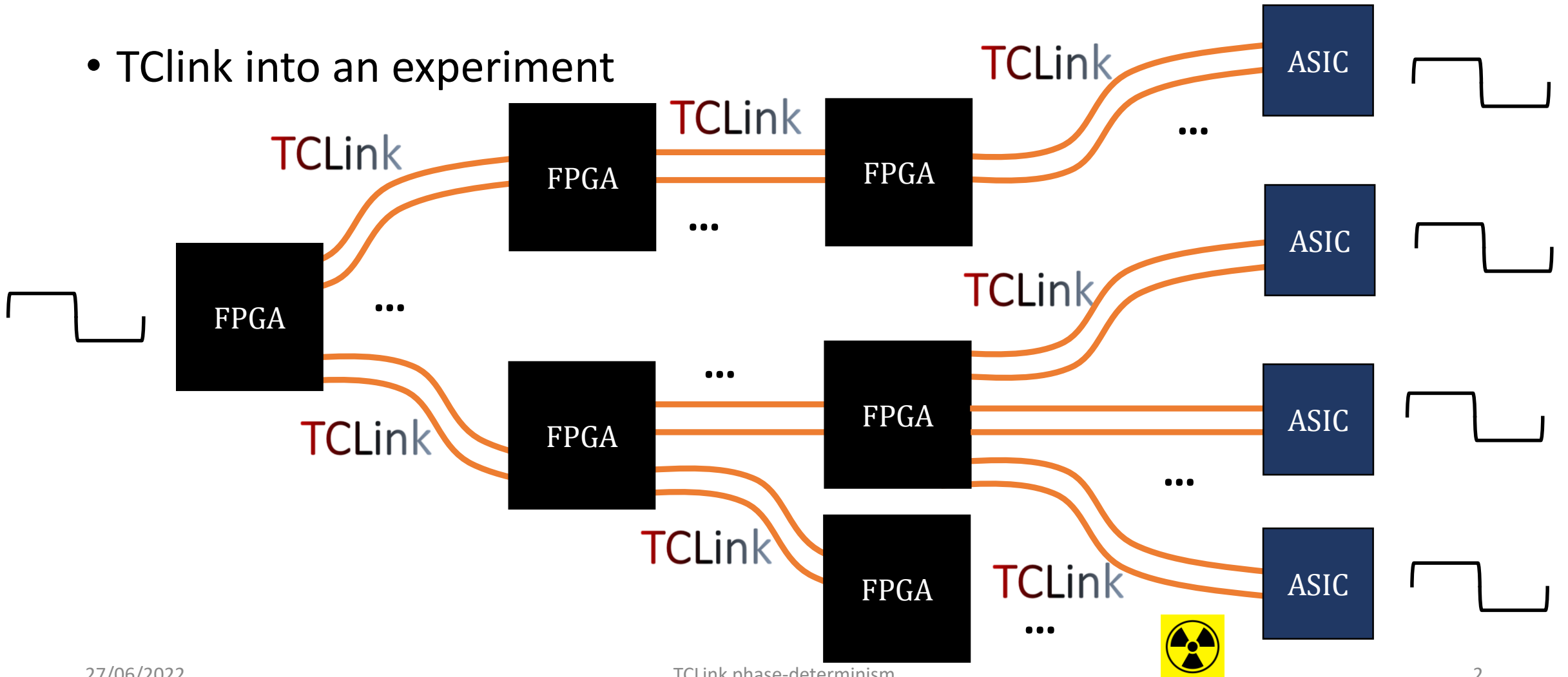
# TCLink

## Discussion on phase-determinism tests

Sophie B. / Eduardo M. – 27/06/2022

# Introduction

- TClk into an experiment

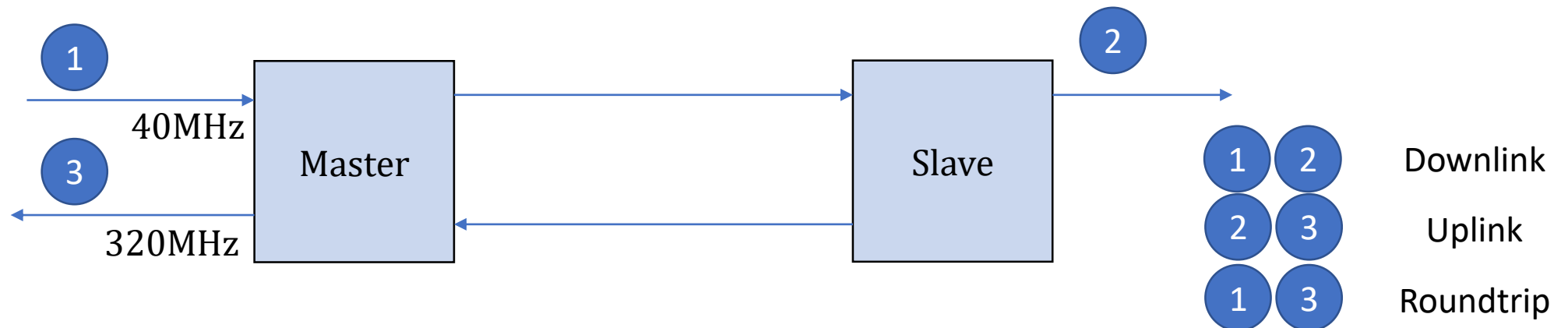
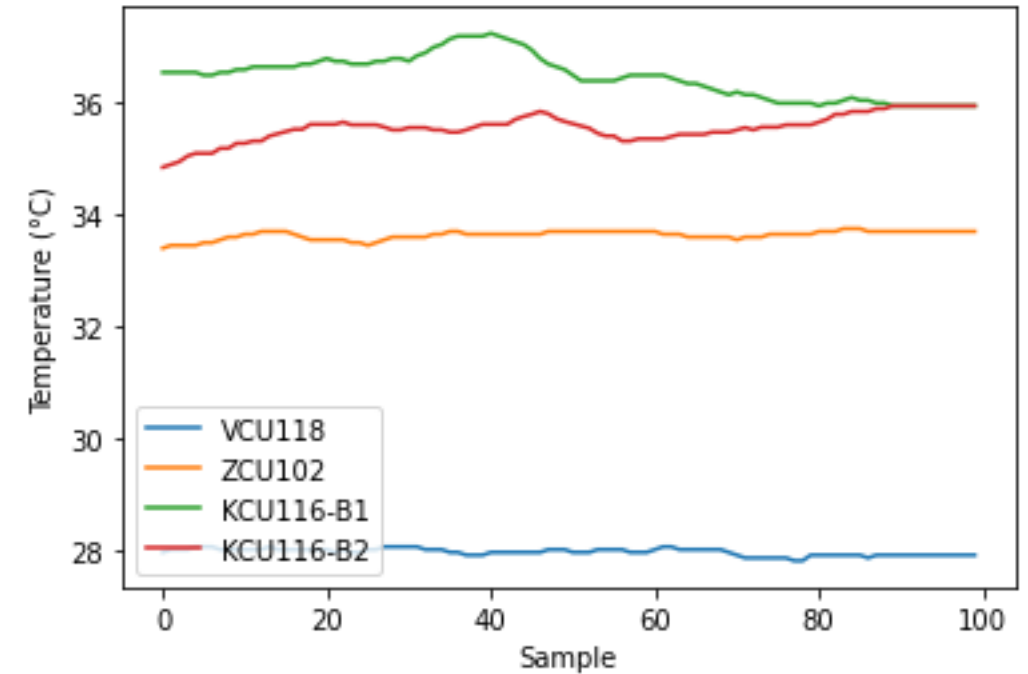


# Overview

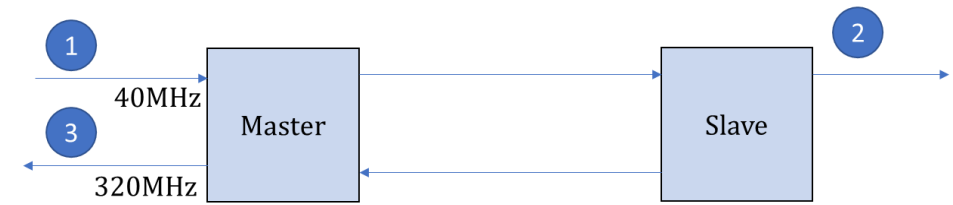
- Preliminary studies
- New Rx architectures

# Example design

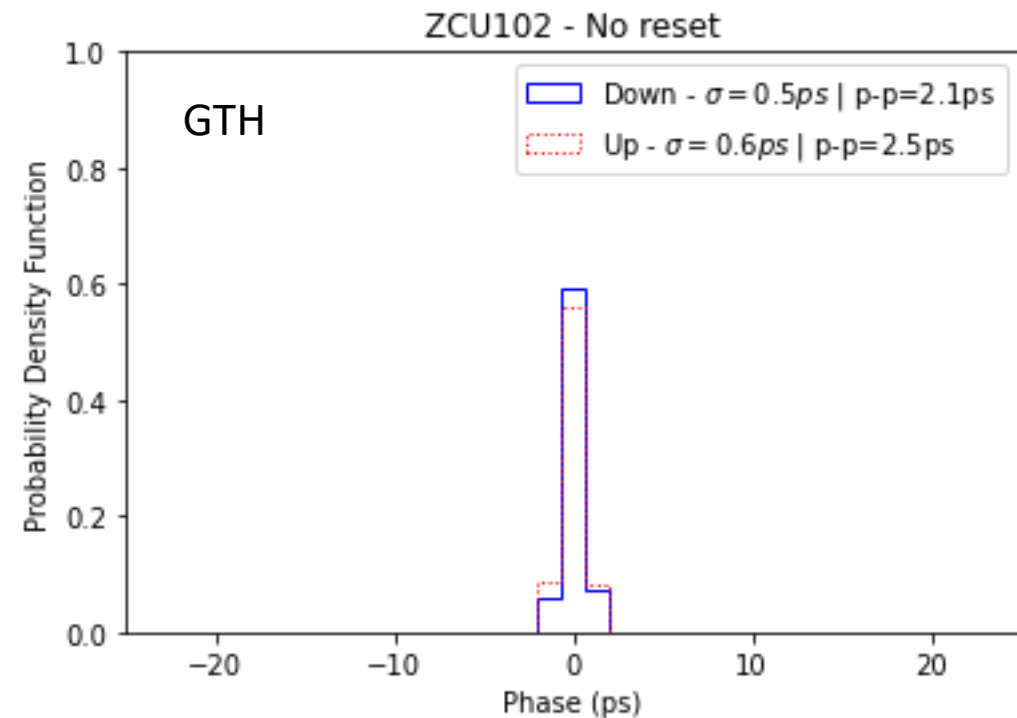
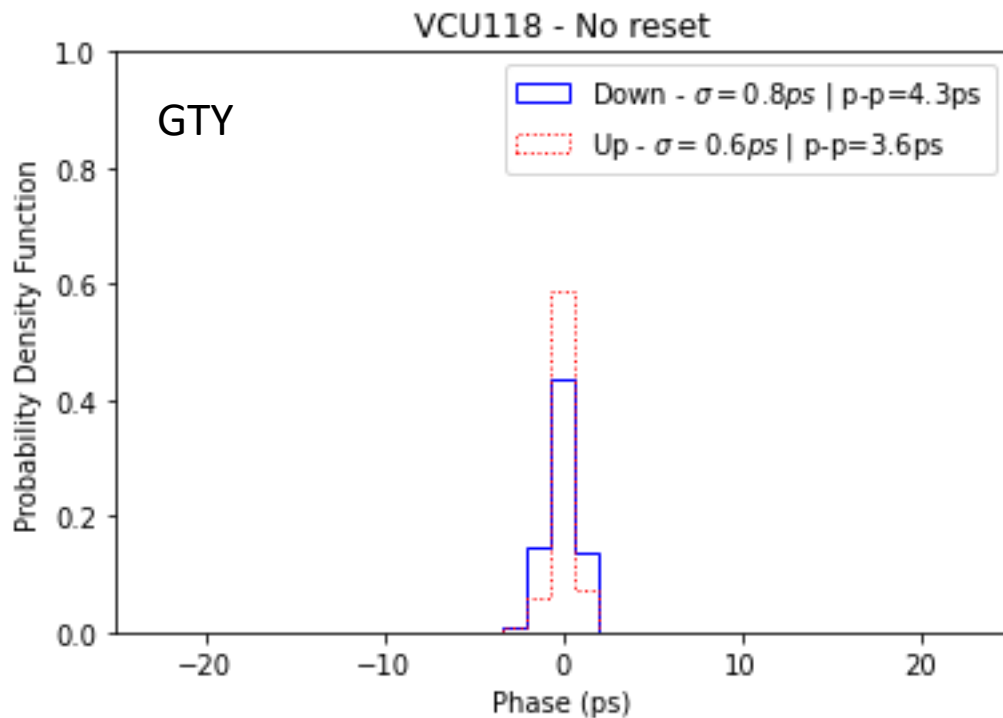
- Master/slave share same FPGA
  - ZCU102 –Ultrascale+ GTH
  - VCU118 – Ultrascale+ GTY
  - KCU116 – Ultrascale+ GTY (2 boards)
- Master Rx uses rxslide PCS: up mod UI
- Low temperature variation



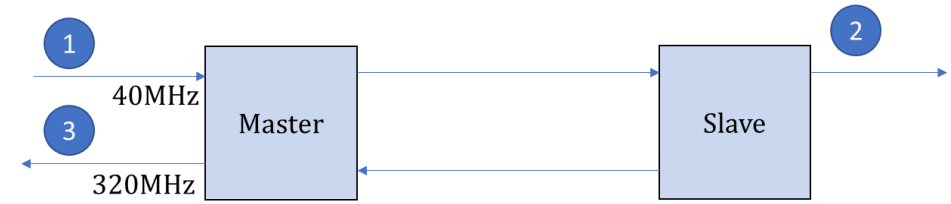
# Meas. Control (no reset)



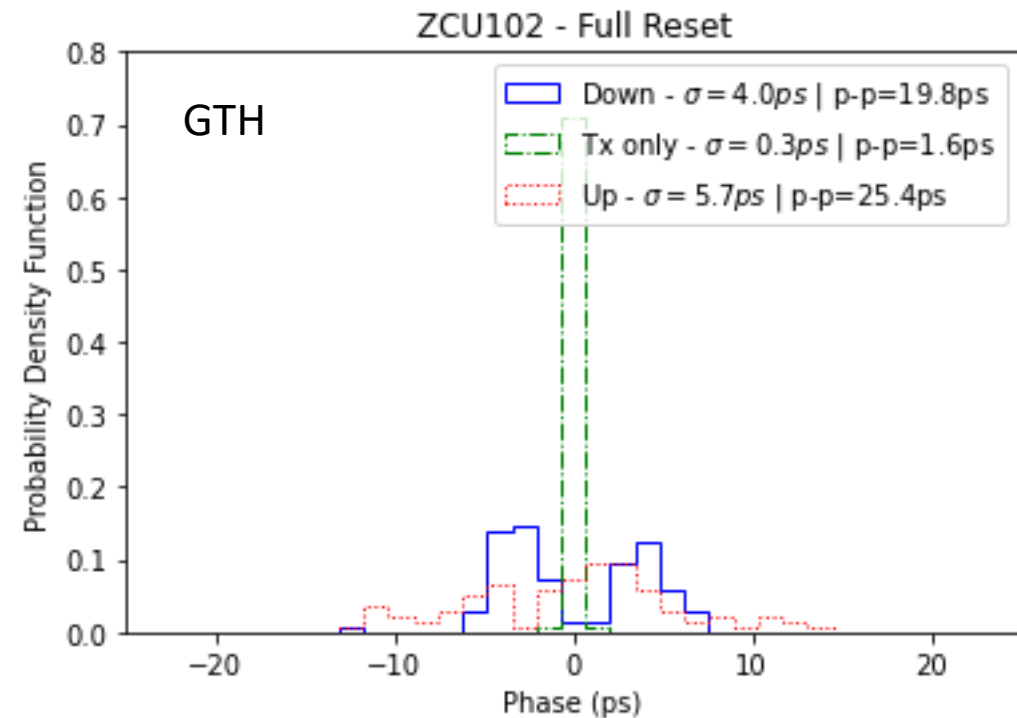
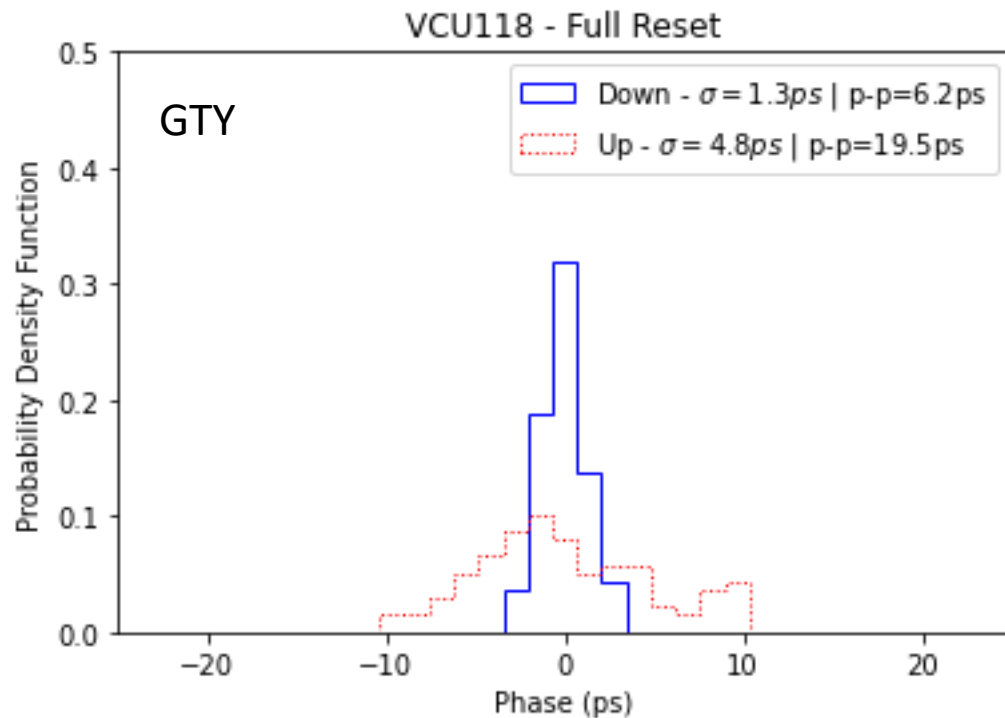
- Very little phase variation for both tests
- Our measurement methodology is good



# Full reset

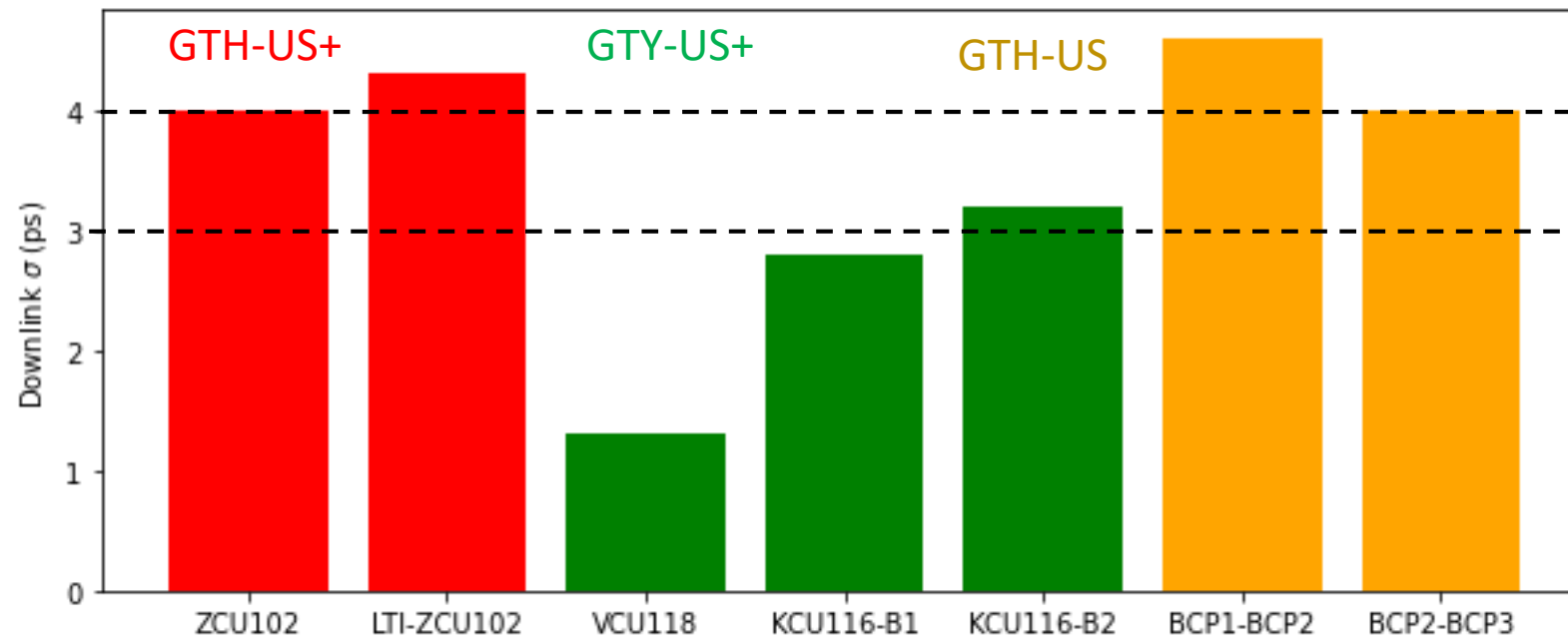


- Phase variation seems to come from Rx (see ZCU102 Tx only)
- Are GTY better than GTH?



# Summary so far...

- Around 4ps rms for GTH and 3ps rms for GTY
- Is there a true difference on GTY vs. GTH?



# New architectures

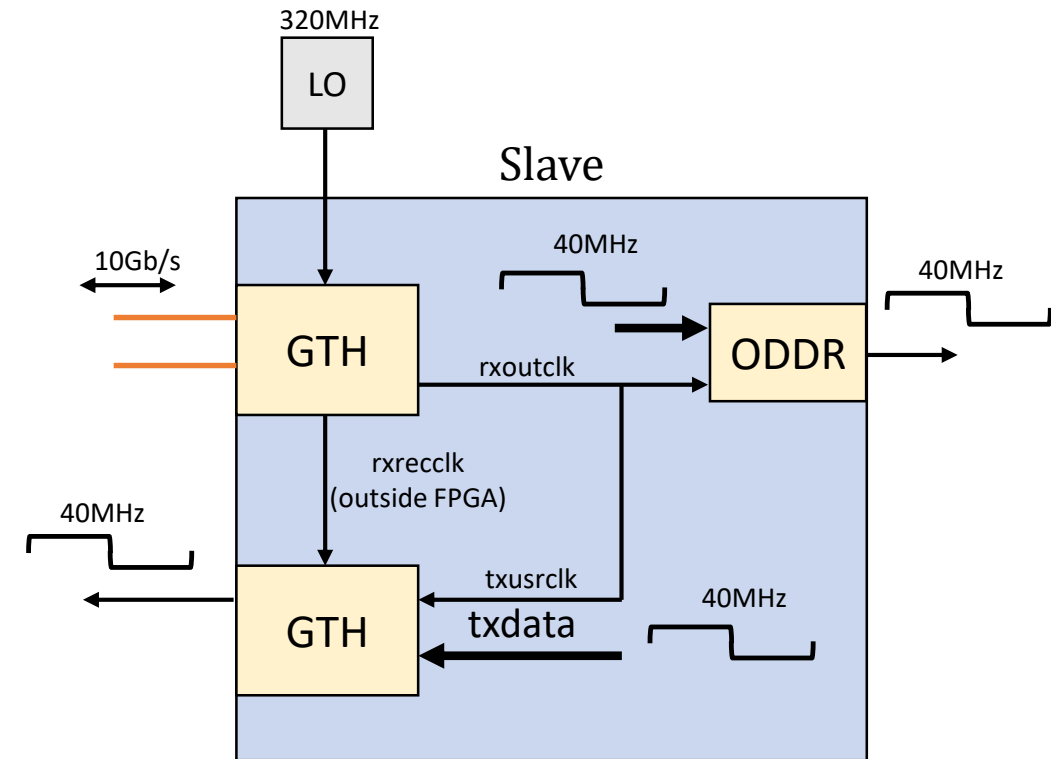
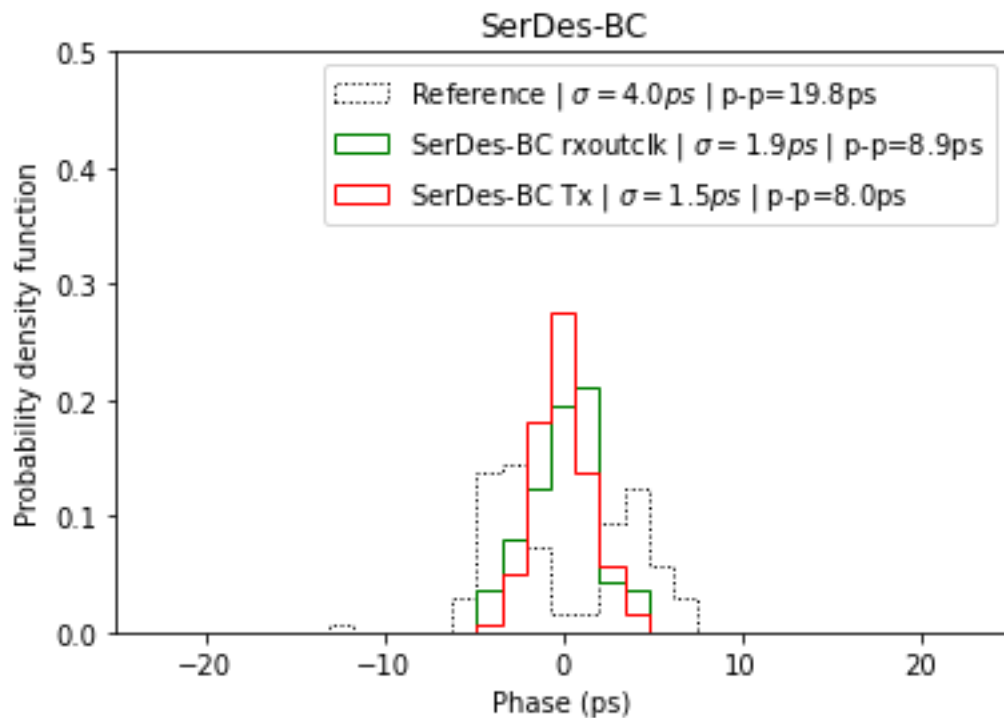
## More advanced studies with ZCU102

- SerDes-BC
- RxoutclkPCS
- Roulette
- Roulette FIFO



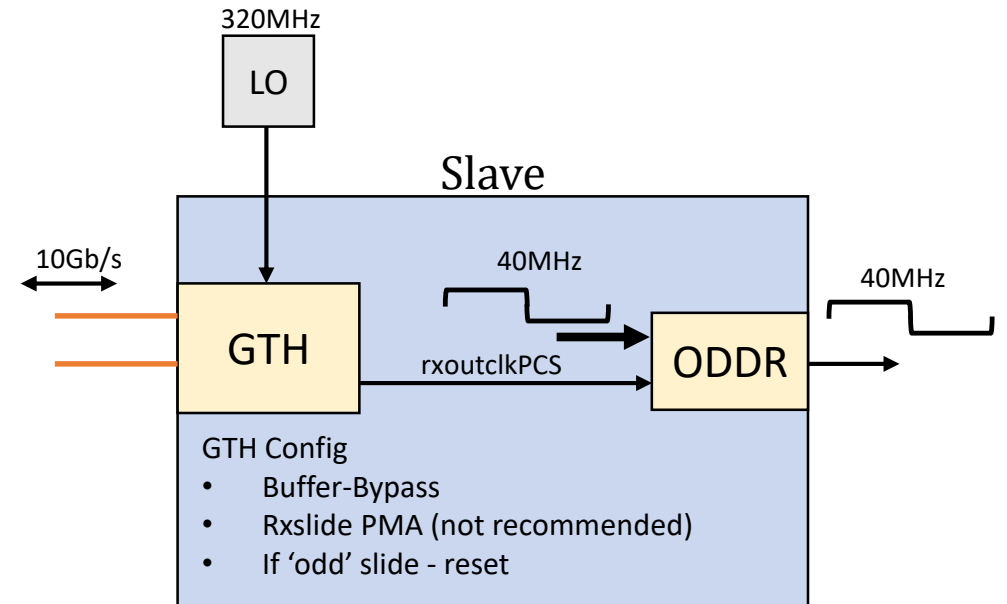
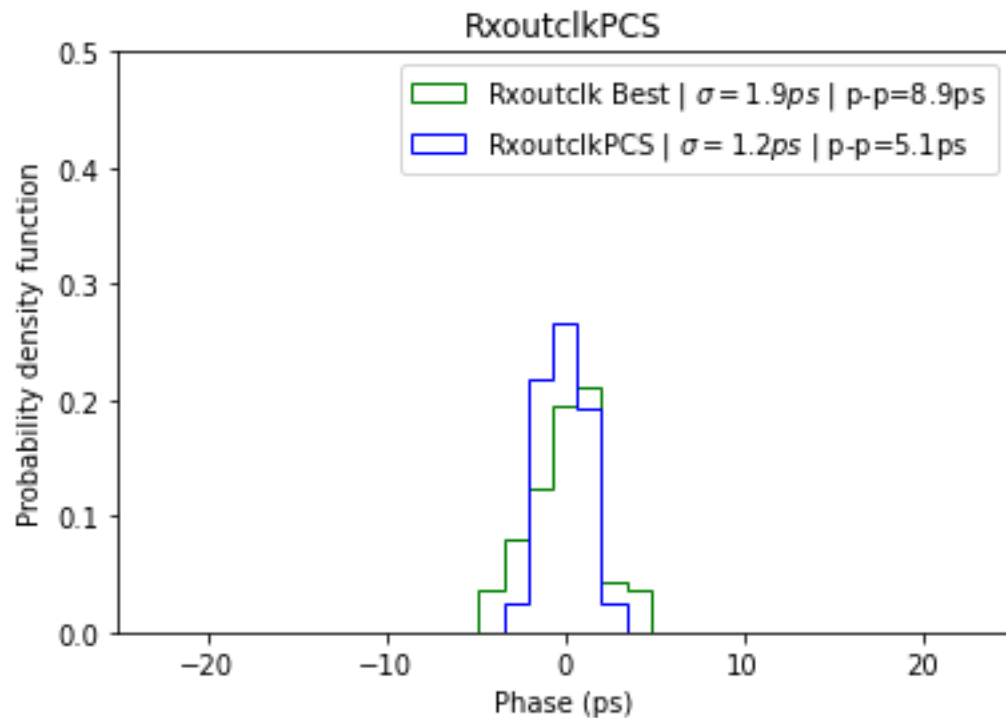
# New architecture: SerDes-BC

- Sacrifice two reference clock pins and one SerDes
- Good results but... rxoutclk also significantly improved (?)



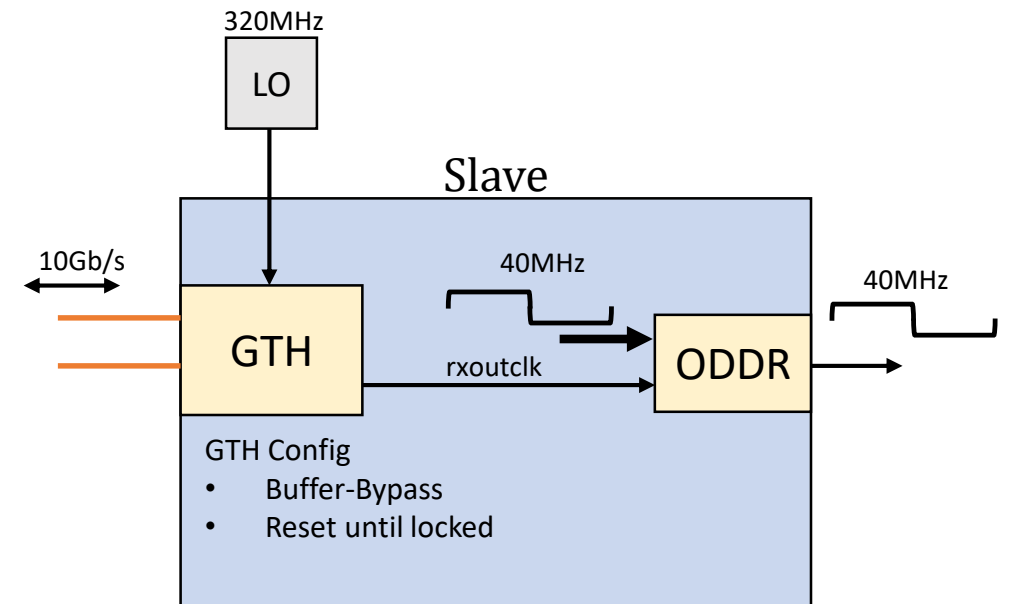
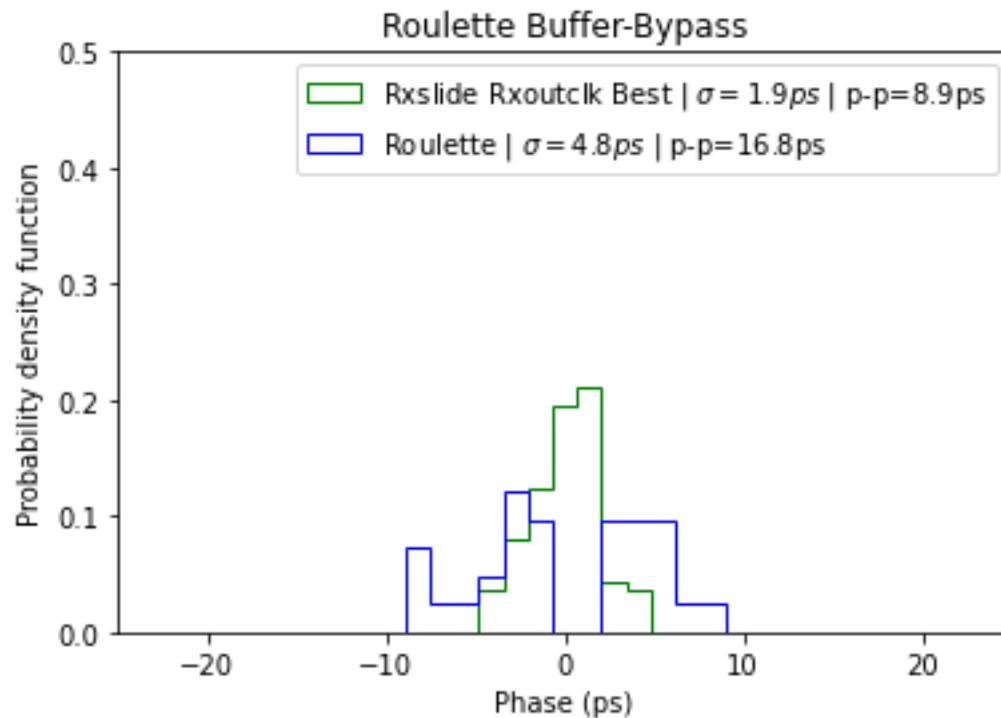
# New architecture: RxoutclkPCS

- Use dedicated RxoutclkPCS pin - same overall architecture
- **Higher temperature variability** as studied by Nikitas-CMS



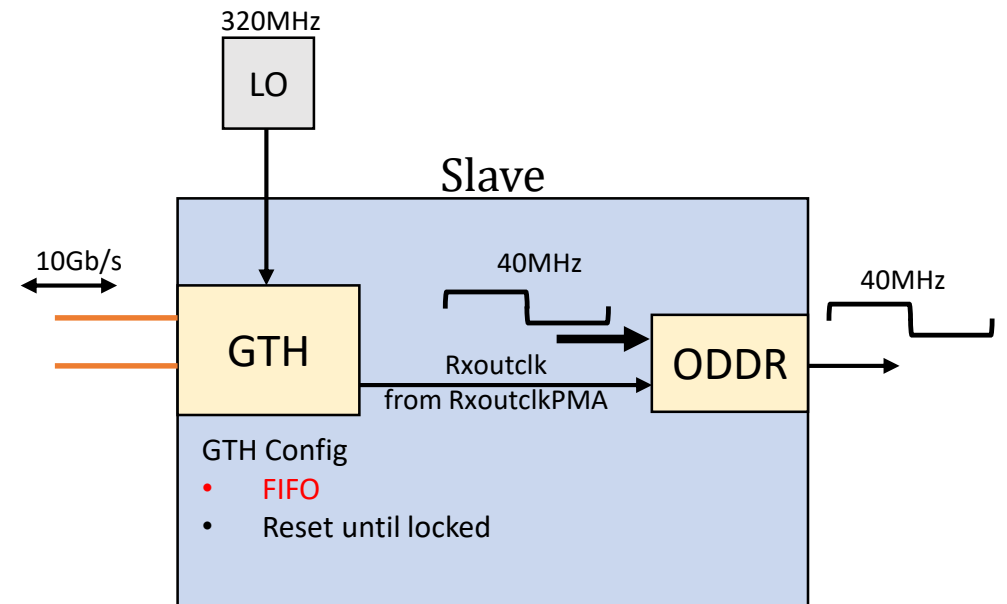
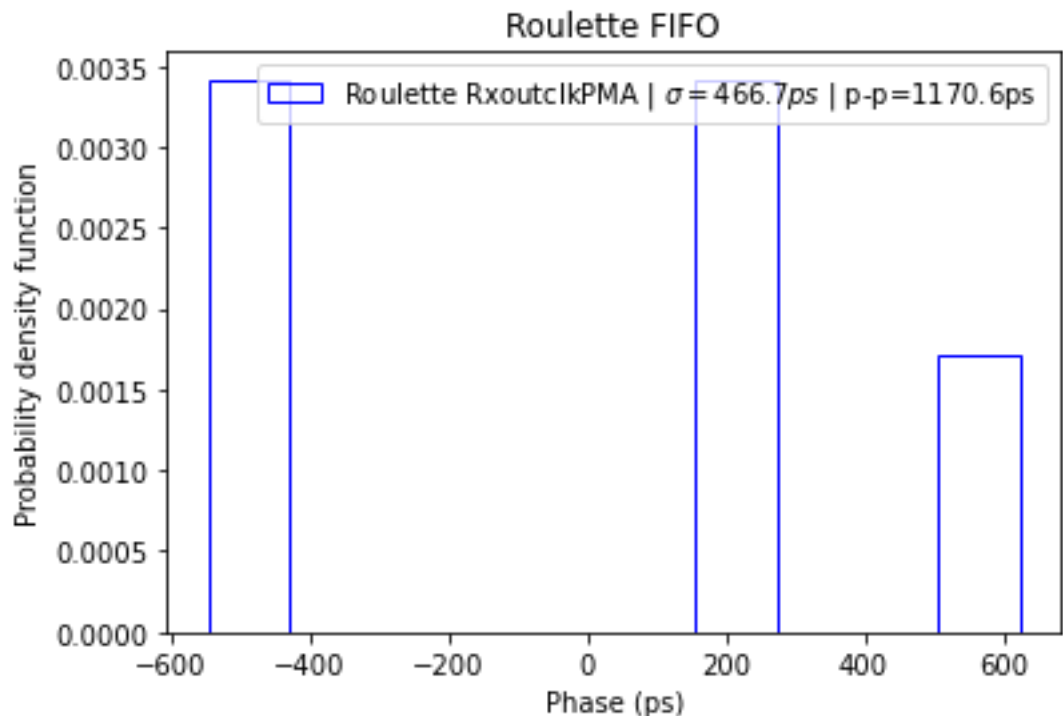
# New architecture: Roulette

- Roulette (reset until locked) in buffer-bypass mode is not better...
- What about if FIFO is enabled?



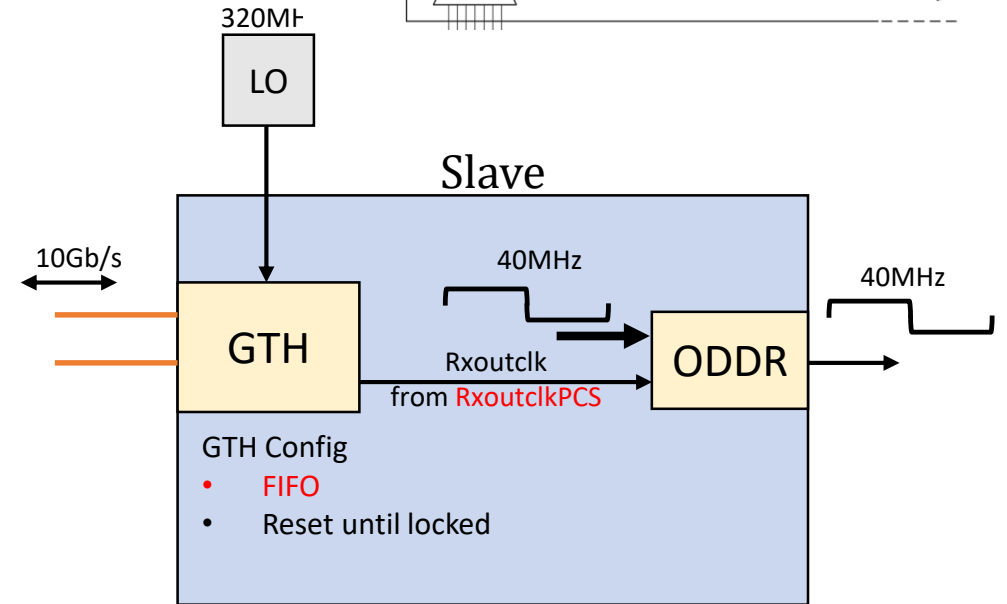
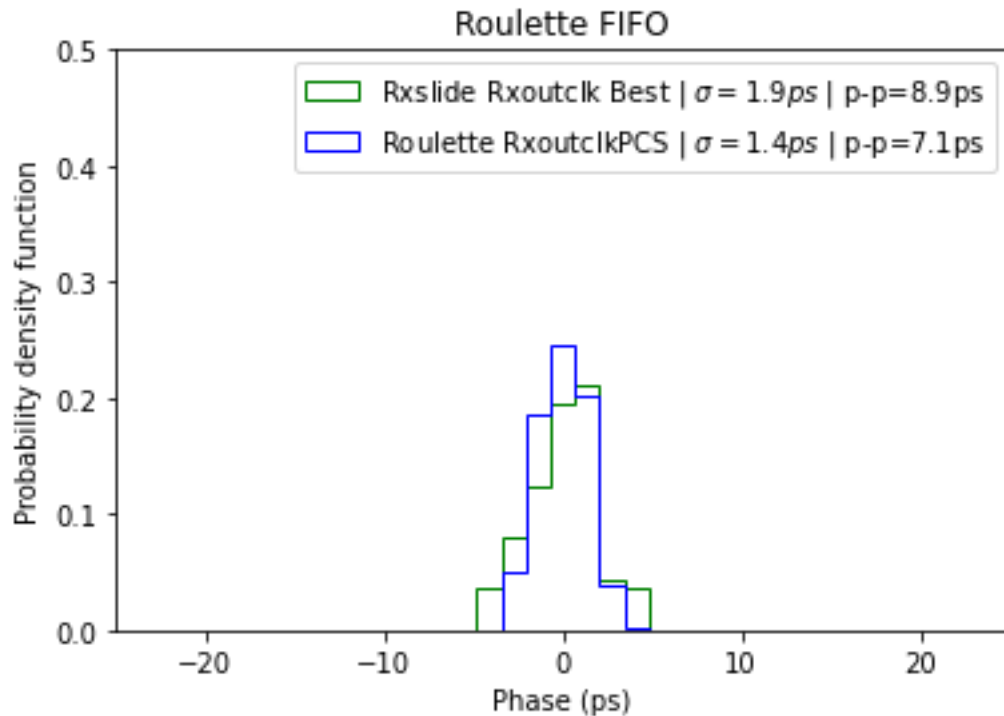
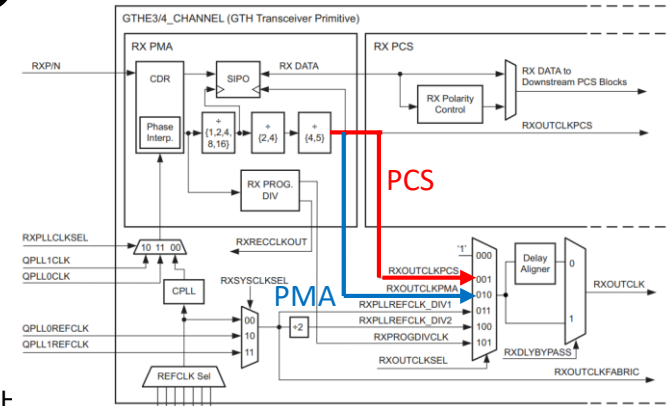
# New architecture: Roulette FIFO

- When rxoutclk comes from rxoutclkPMA: phase is not fixed
- UI jumps (just ran a few points here)



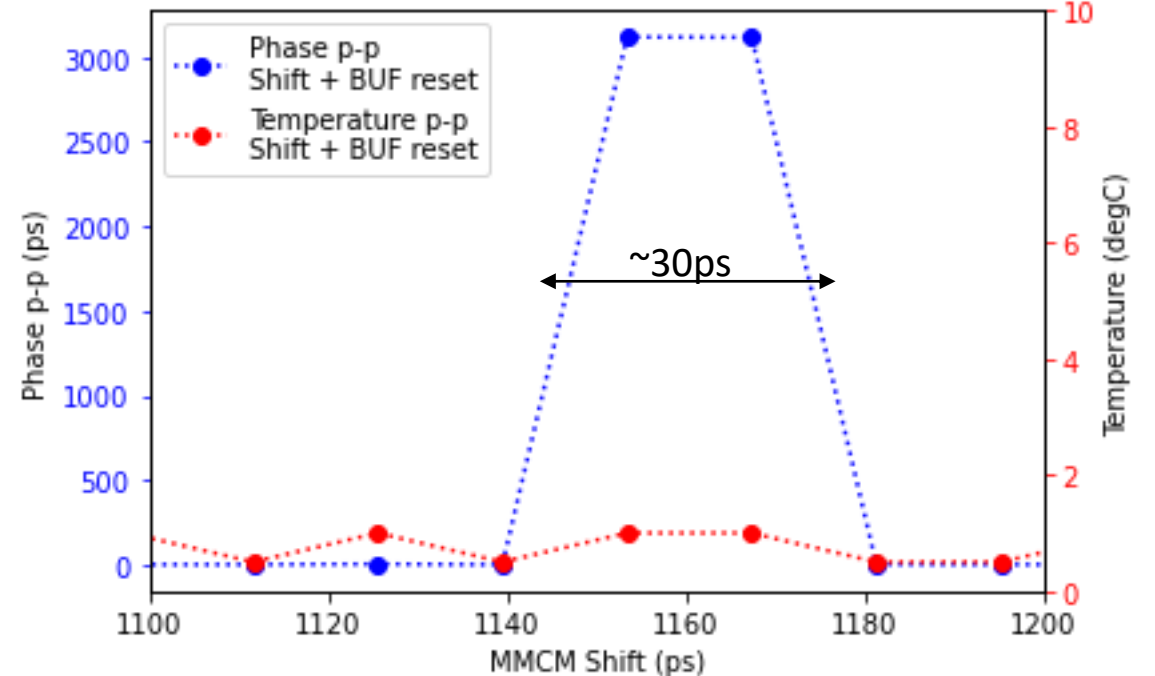
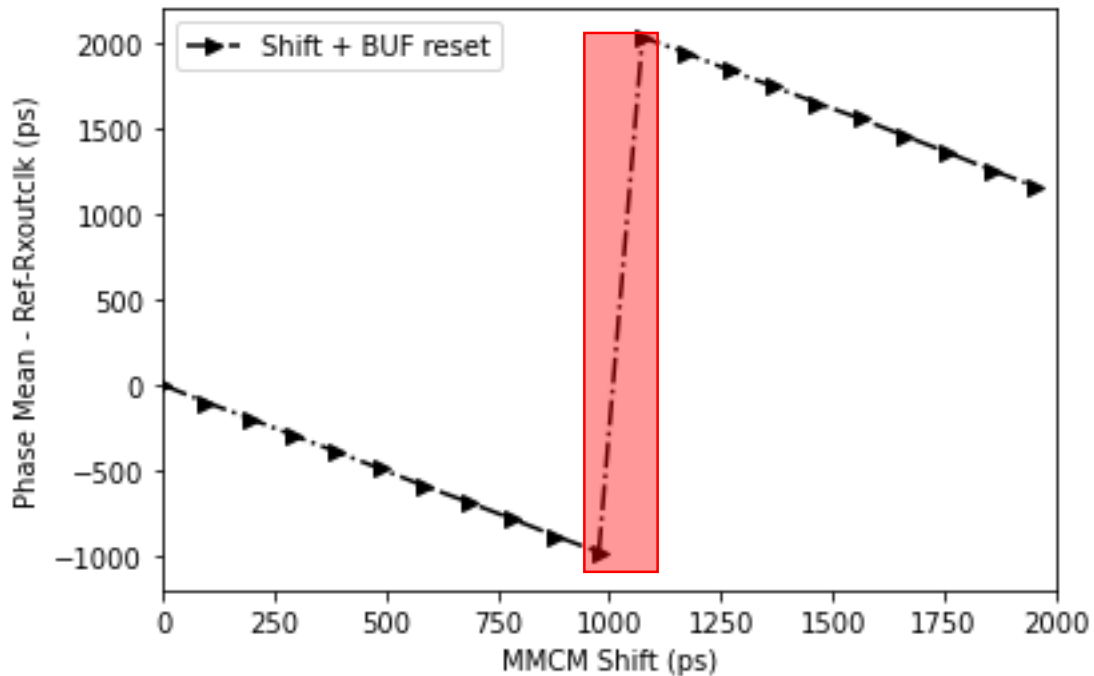
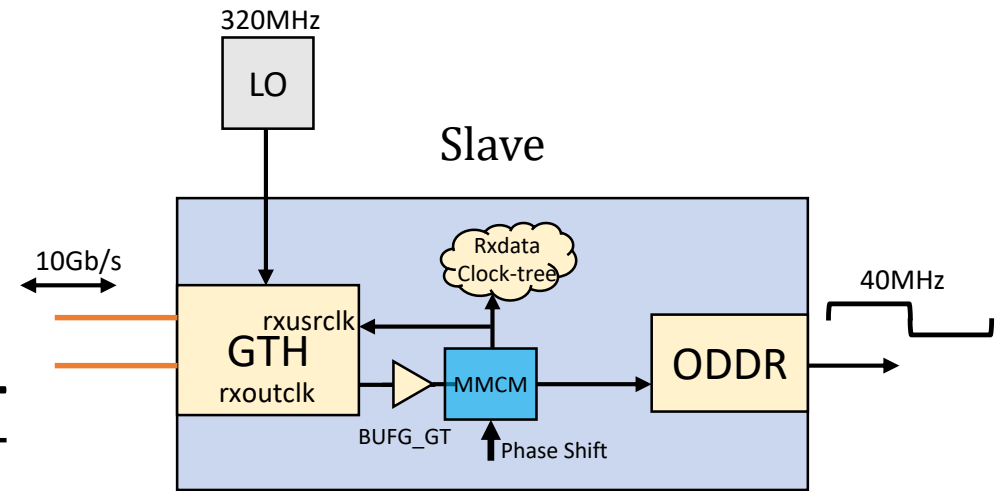
# New architecture: Roulette FIFO

- Fixed phase (why is it different: PMA/PCS?)
- But this represents a risk...



# Roulette FIFO: the risk

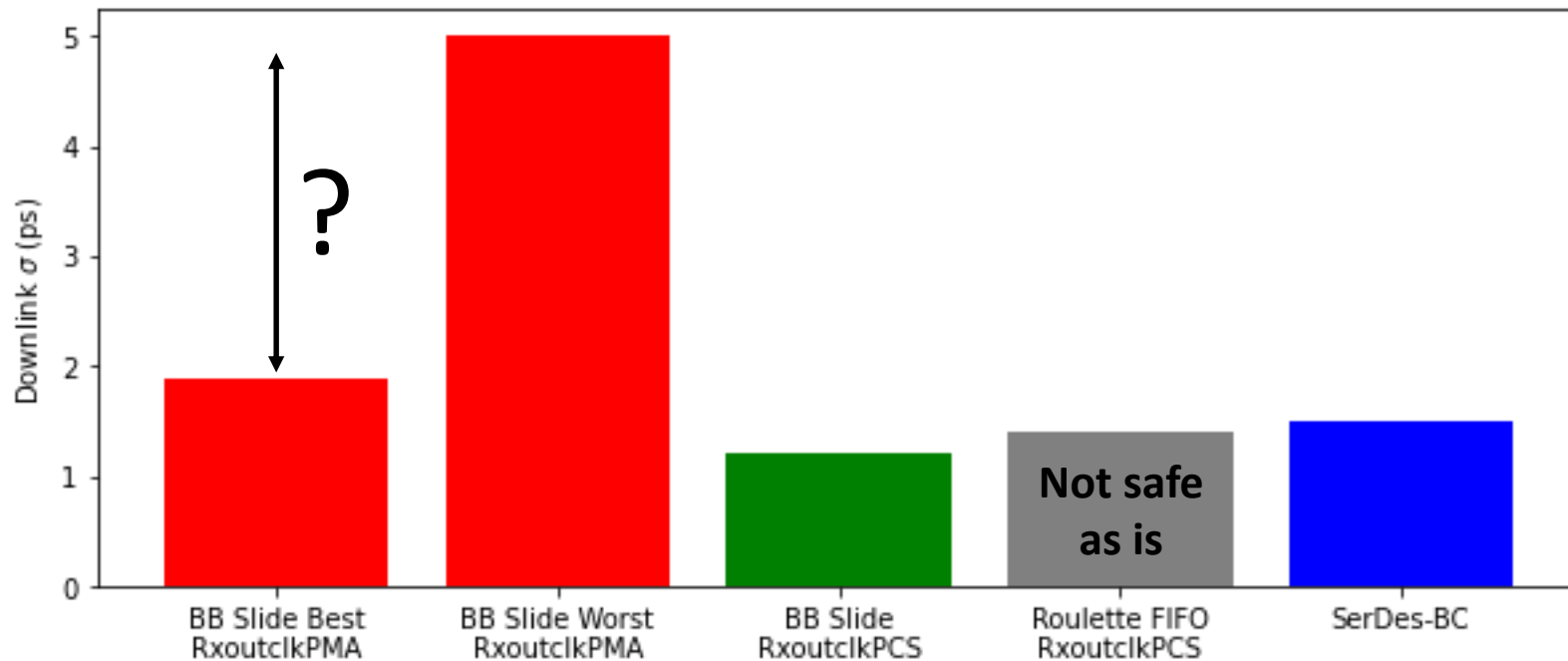
- Full-period jumps in metastability zone
- Phase depends on implementation & PVT



- This architecture **requires additional mitigation technique!**

# Summary

- Four different architectures were explored for receiver fixed-phase
  - Help needed
- Large variability observed seems related to clock-tree



- Hard to assess performance if we don't understand variability