BLM ASIC performance and future plans

Christos Zamantzas (SY-BI) on behalf of WP13.1

with contributions from: Francesco Martina, William Vigano', Ewald Effinger, Mathieu Saccani, Eva Calvo Giraldo, Anton Lechner, Belen Salvachua

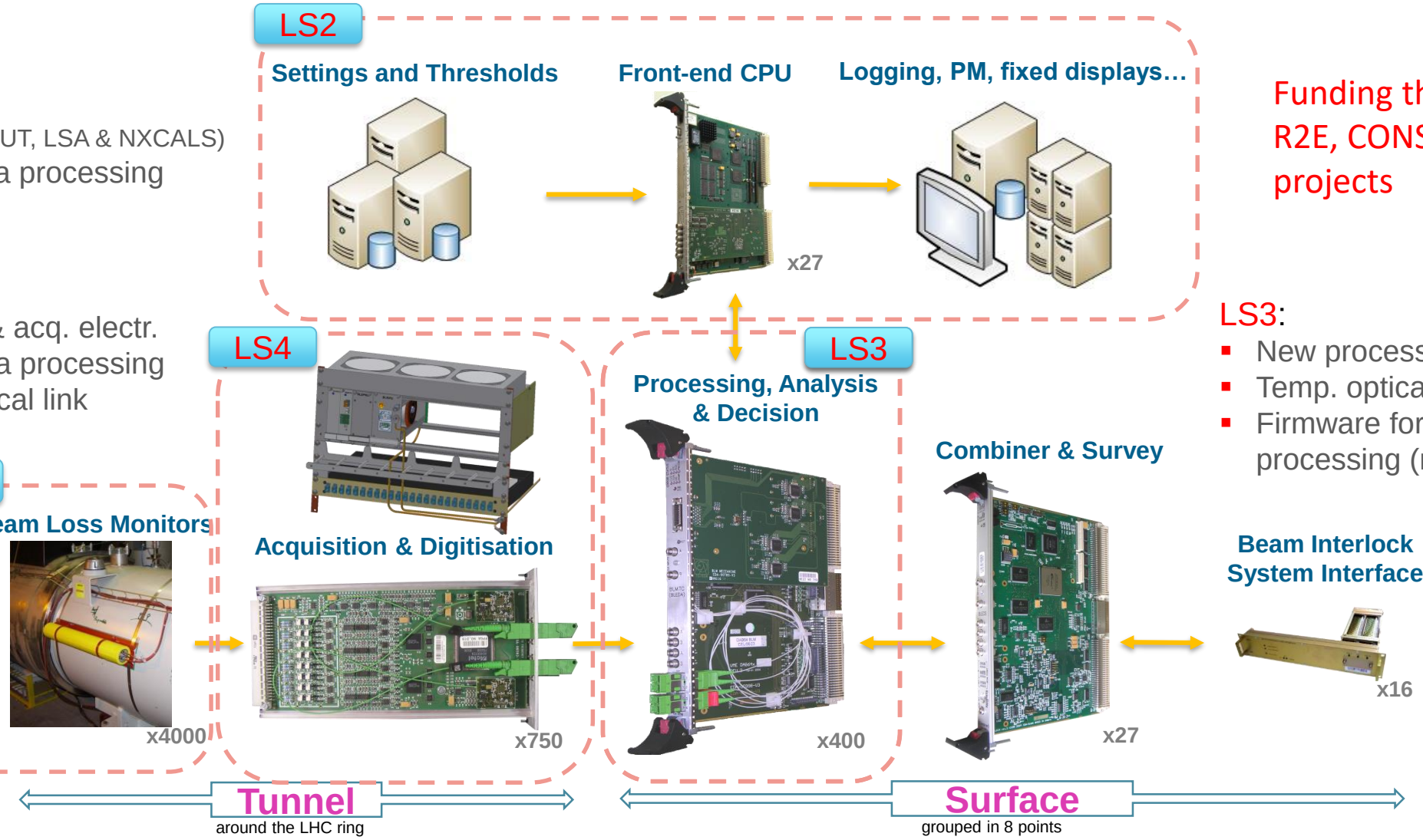
12th HL-LHC Collaboration Meeting, Uppsala (Sweden), 19-22 September 2022

LHC Beam Loss Monitoring System – Upgrades

LS2:
- New FESA & OS
- Databases (LAYOUT, LSA & NXCALS)
- Firmware for data processing

LS4:
- New mini-crate & acq. electr.
- Firmware for data processing
- Bidirectional optical link

LS3+:
- Detector production

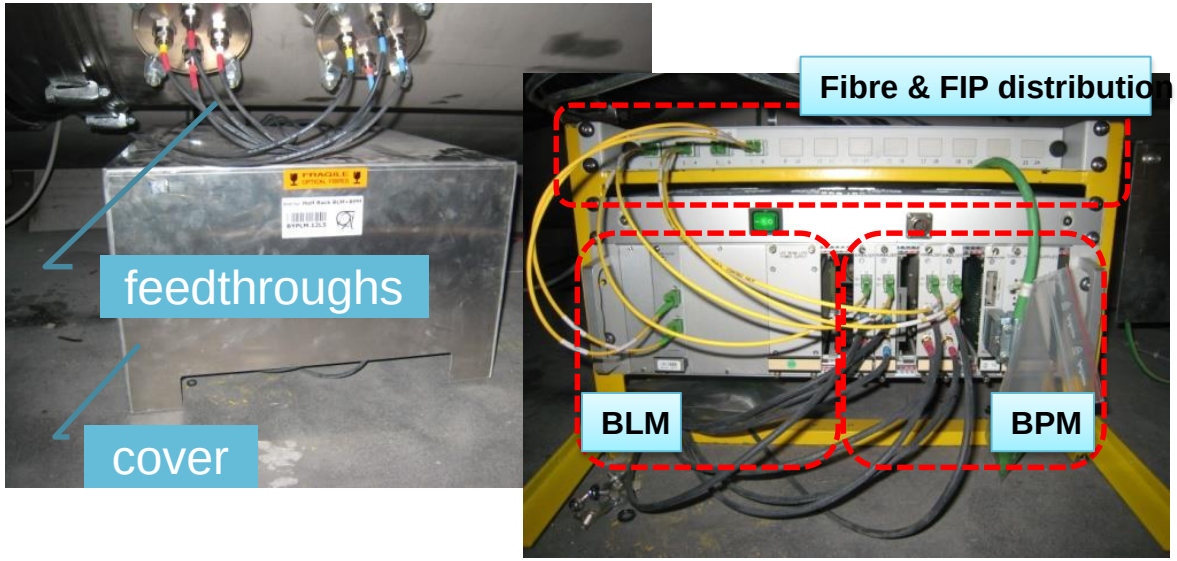


LS3:
- New processing electronics
- Temp. optical receivers
- Firmware for data processing (new FPGA)

Funding through R2E, CONS & HL-LHC projects

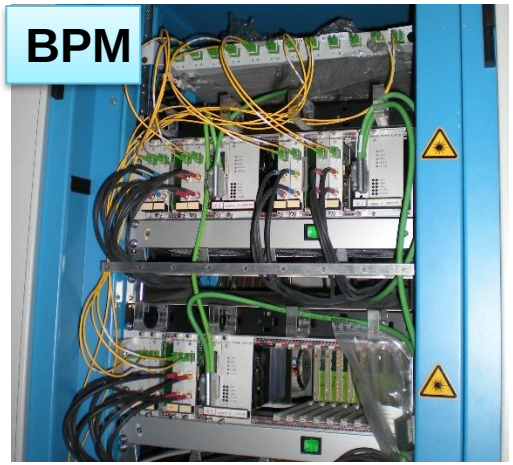
LHC Tunnel Installation

ARC electronics



- Installed under each Quadrupole
- Common mini-crate & fibre network
- Separate power supplies

DS & LSS electronics



- Localised in alcoves like UA, UJ or RR
- Same electronics in a different configuration
  - Exception the BLM power supply

Three variants of the mini-crate needed for LHC BPM & BLM systems

Development & Deployment Plans

HL-LHC BLM Development Plan

Development required for new:

- Rad-Tol card (BLEIC) to allow reduced cable lengths and improve S/N ratio
  - Hybrid COTS & ASIC version would be challenging and limited to < 1 kGy (study made; will keep as backup plan)
  - Rad-hard Application Specific Integrated Circuit (ASIC) under development to encapsulate all the analog-to-digital conversion.
- Crate and power supplies to host acquisition electronics
  - 3 variants required
  - ARC installations shared w/ BPM; LSS separate BPM & BLM installations
- Communication layer between tunnel and surface electronics
  - Multi-gigabit rad-tol bidirectional link
- Integration to the surface electronics
  - Processing and decision firmware
  - Control and supervision firmware

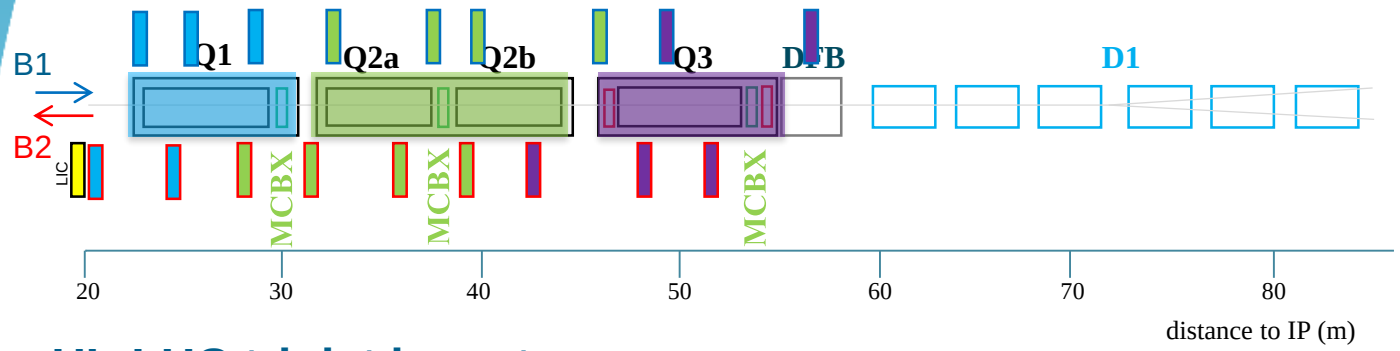
HL-LHC BLM Deployment Plan

- LS3
  - Extension of the current BLM system with additional detectors following HL changes
    - e.g. IP1 & IP5 Triplet, Collimation, BBLR, etc. areas
  - First deployment of the full new electronic stack at strategic locations in parallel to the current electronics
    - to complete and validate development
- LS4
  - Full deployment of new electronics
    - replacement of the complete tunnel electronics stack (mini-racks, crates, power supplies etc.).

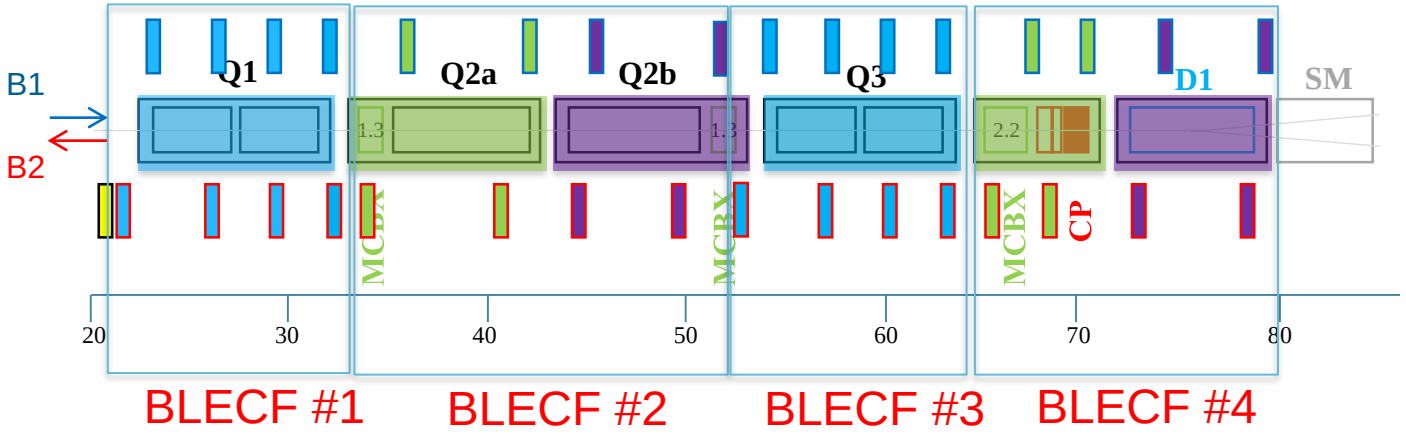
BLM detectors at LS3 Triplet Layout

Work in progress between SY-BL, SY-STI & WP15;
Final integration might change numbers

LHC triplet layout



HL-LHC triplet layout



Single multiwire cable per module
One BLECF or BLEIC module accepts 8 channels

During LS3 will extend the current system for the new topology and deploy the new system (BLEIC) in parallel in half of the locations.

Will allow validation for full deployment during LS4 and (some) redundancy in this critical area long-term.

Current system w/ BLECF // BLEIC/2 (Half channel redundancy)

Number of detectors: Total for IP1 + IP5 (both sides)			
	Present System Run 3	HL-LHC Upgrade Run 4	New in Run 4
BLECF – standard	72	128	56
BLEIC – new	0	**64**	64
Total IP1+IP5	**72**	**192**	**120**

BLM Detectors (IC) – Quantities Needed

- HL-LHC : 200 units
  - Cover new IP1 & IP5 triplet areas (~120 new channels) and
  - Several new locations to cover for Collimation, BBLR etc.
- LHC : 300 units
  - Replenish spares (LIU needs were x2 more than originally assumed)
- SPS : 500 units
  - Renovation of all ring and some TL during LS3
  - Includes needs for TDC2 (20 units) and ECN3 (50 units)

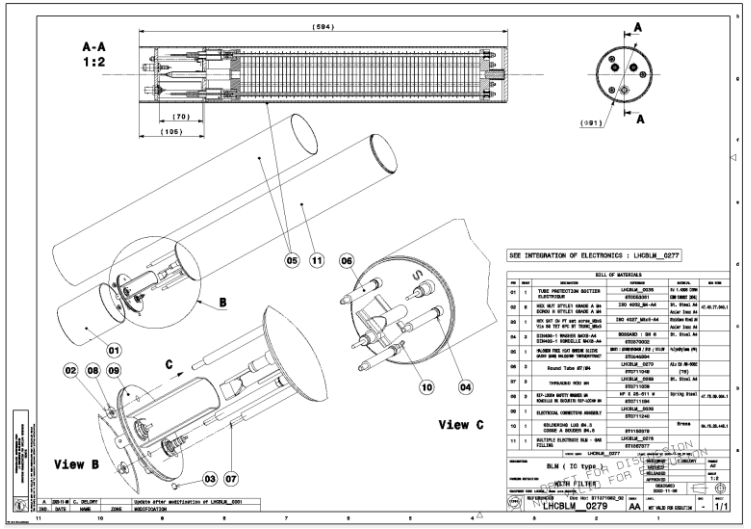
Missing Russian in-kind; new funding source is under discussion

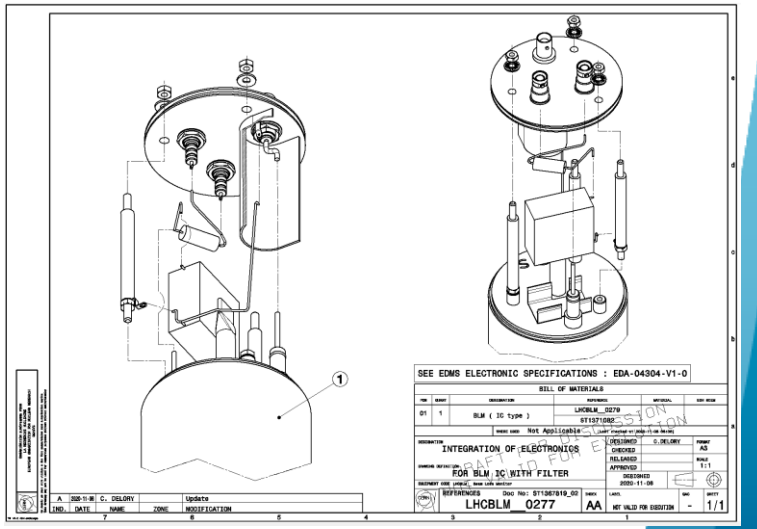
BLM Detectors (IC) – Production Plan

Work in progress between SY-BI, EN-MME & TE-VSC;

- 2021 – drawings for production
  - recheck all drawing and add parts missing
  - prepare them ‘for manufacturing’
- 2022 – prototype production at CERN (~ 5 units in total)
  - use spare parts (for the complex/long delivery parts)
  - verify new drawings and finalise production documents
- 2023 – planning, documentation and validation benches
  - agree on production plan (e.g. which parts to outsource)
  - order key/complex material (e.g. feedthroughts & ceramics)
  - design electrical & vacuum stands
  - award contract(s)
- 2023/4 – build the vacuum stand
- 2024/5 – Series Production (1000 units in total)
- 2025+ – Verification with beam (GIF++)

Under discussion; to be finalised



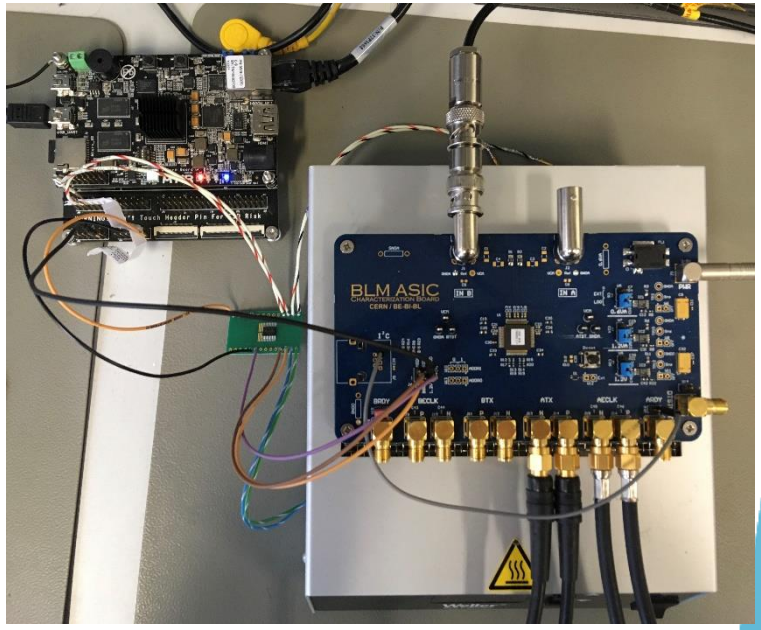


Development progress

BLM ASIC R&D Timeline

Prototype development timeline:

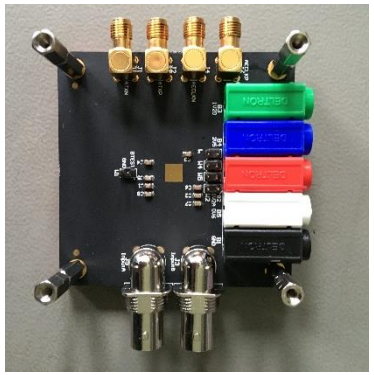
- 2018 Q1: project start; technology selection and feasibility
  - Parallel design of two methods:
    - CFC asynchronous better suited to handle large currents and quickly varying signals
    - Delta-Sigma ideal for high accuracy due to oversampling and filtering
- 2019 Q4: V1 delivery
  - Issue with internal power distribution and ESD protection
  - Could not test full range
- 2020 Q4: V2 delivery (some delays due to COVID)
  - Mostly functional;
  - Metastability issues with the sync between the analogue and digital domains
  - High current leakage of the input stage FETs; poor low current meas.
  - Decision to continue with the CFC asynchronous method only
- 2022 Q1: V3 delivery
  - Analogue & digital circuits fulfil needs; all currently known issues resolved
  - New minor issue w/ sync between CFC & ADC data; mitigation possible at the backend

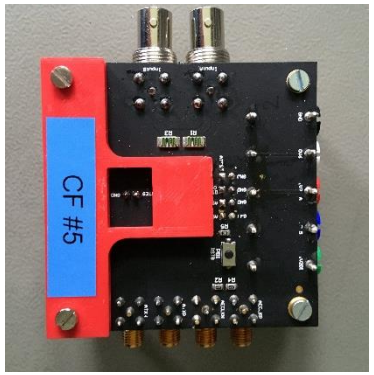


Development of custom ASIC verification testbench

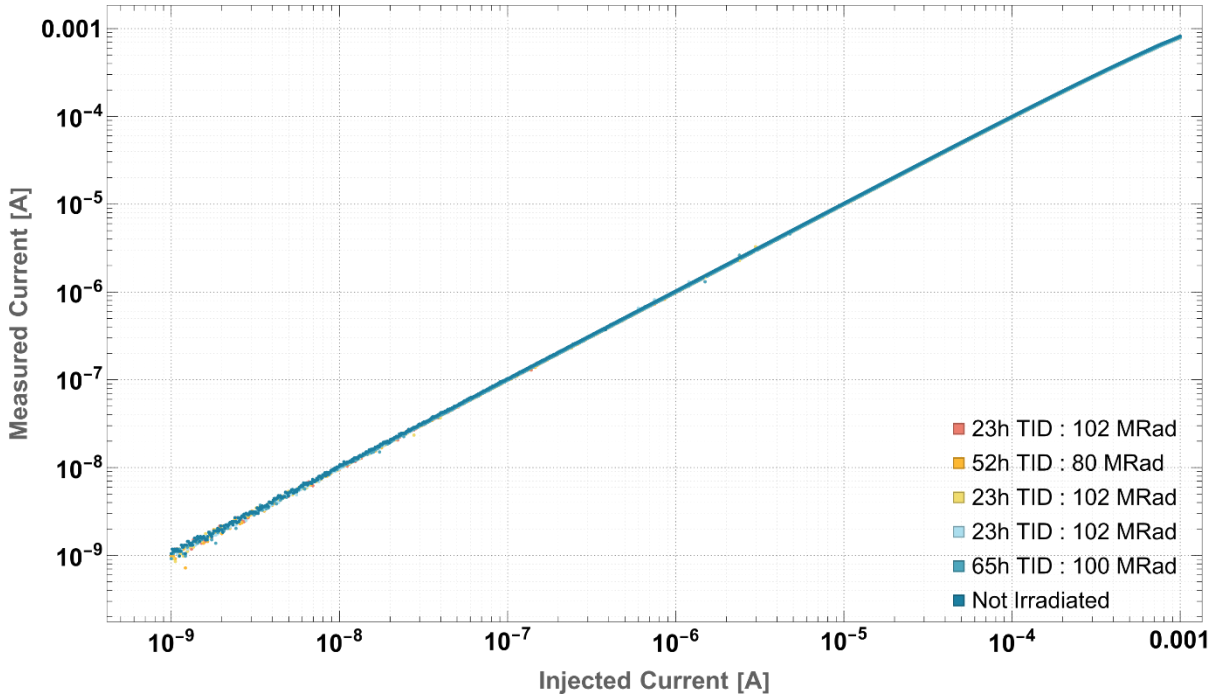
Irradiation Results – X-Rays

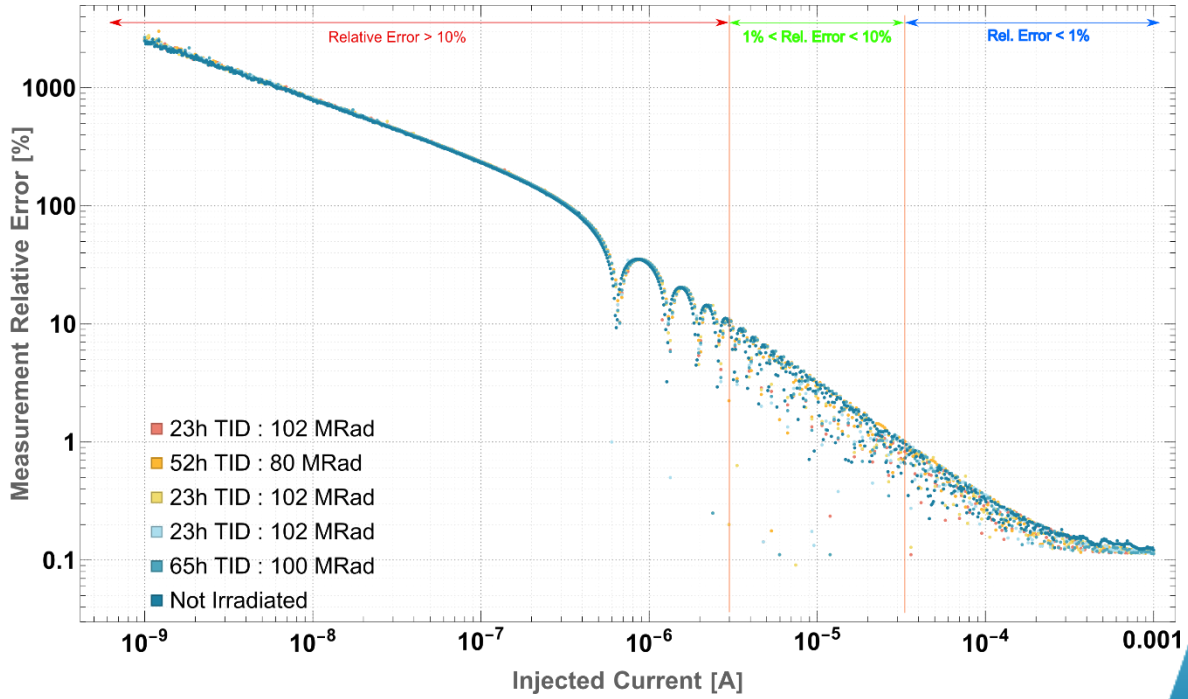
XRAYs	Flux [MRad / h]	Time [h]	TID [MRad]
CFC#0	Not Irradiated	0	0
CFC#1	4.43	23	102
CFC#2	1.54	52	80
CFC#3	4.43	23	102
CFC#4	4.43	23	102
CFC#5	1.54	65	100





Conversion characteristic (left plot) and relative errors (right plot) by a logarithmic current sweep of 500 values from 1 nA to 1 mA.
The averaging time window is set to 100 μs.





Printed Circuit Board Prototype (BLEIC)

New prototype PCB design complete

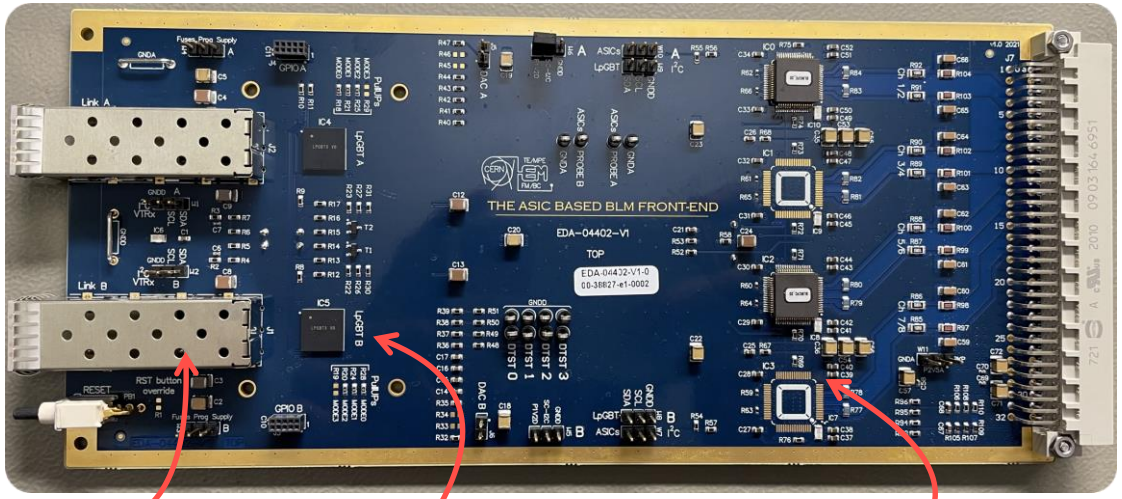
- Includes all functionalities expected from the final system
- Common digital parts, control and form with standard BLM acquisition board.
- Secured prototypes of the other custom parts, e.g. the SM-VTRx and LpGBT.

Prototype production completed and tested to be functional

- This board variant is able to accommodate both BLMASIC v2 & v3

Currently working on system integration (see also next slides)

- Development of back-end firmware for communication and control
- Next step, integration in the real-time data processing and decision making



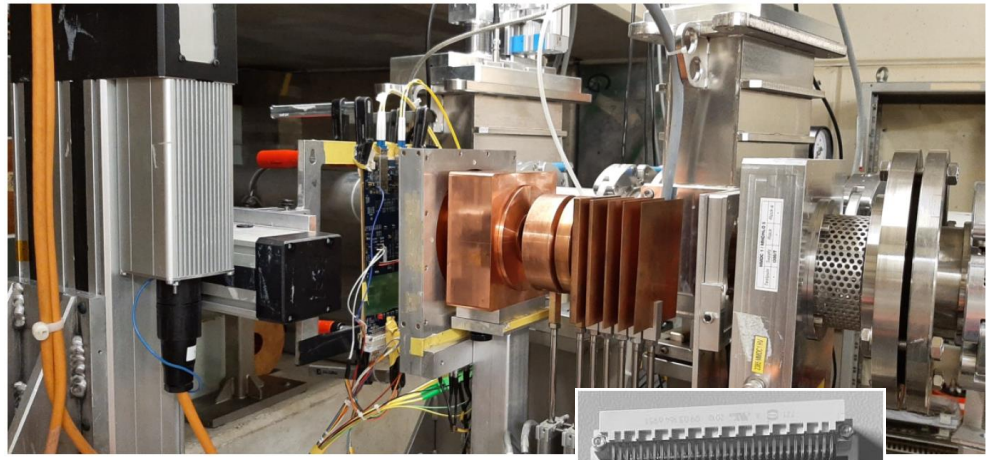
2 x SM-VTRx *2 x LpGBT* *4 x BLMASIC*

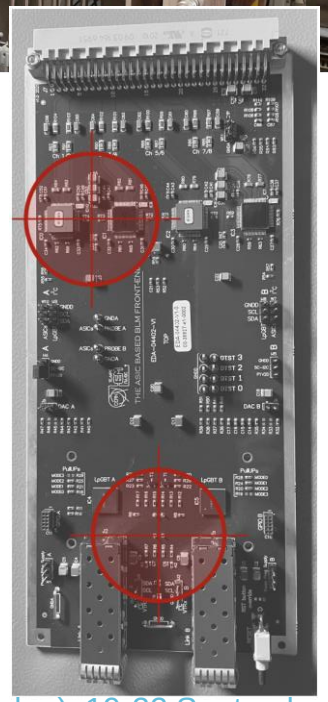
Comparison of old and new technology of radiation tolerant front-ends

	BLECF COTS & ASIC hybrid version	BLEIC ASIC version
Components	> 2000 parts	< 400 parts
Cost	> 3 kCHF/unit	~ 1 kCHF/unit

Irradiation – Protons (PSI)

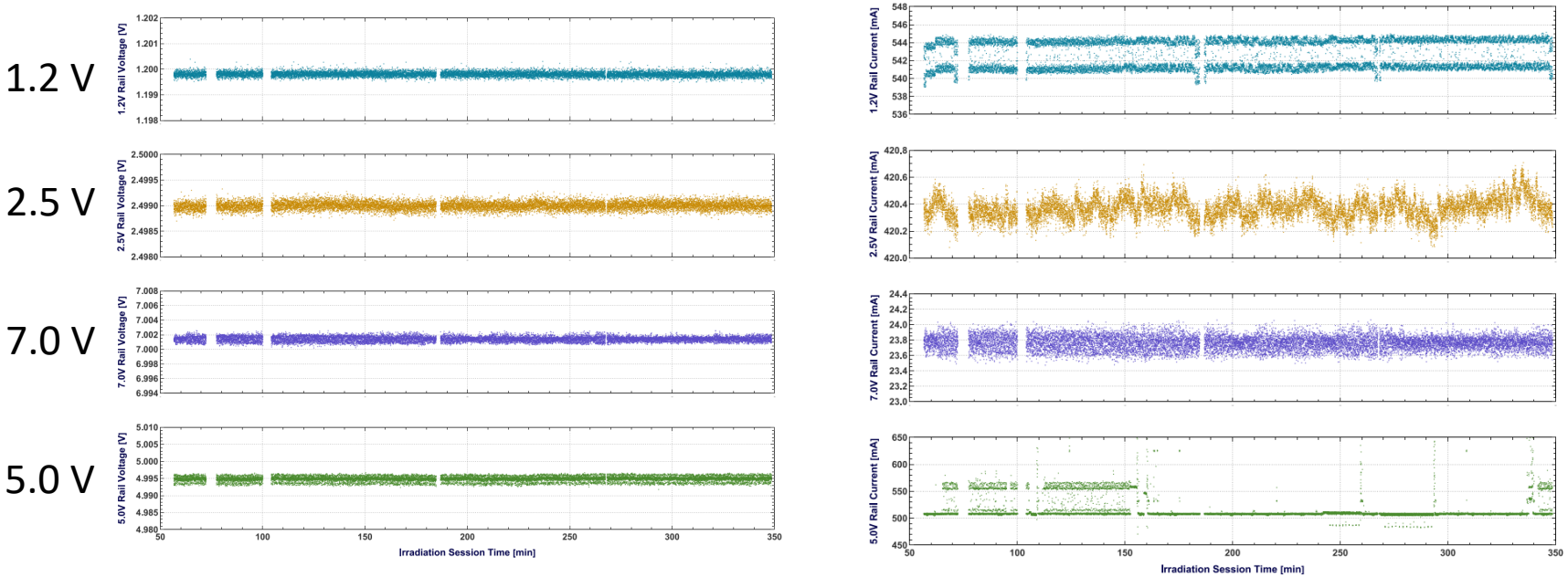
Run	Start Time	Stop Time	Beam Current [nA]	TID [Gy]	Target Area
1	*23:34*	*00:25*	1	50	IC0 / IC1
2	*00:30*	*00:46*	3	50	””
3	*00:51*	*01:14*	7	200	””
4	*01:17*	*02:39*	10	1k	””
5	*02:41*	*04:00*	10	1k	””
6	*04:02*	*05:22*	10	1k	””
7	*05:31*	*05:52*	10	200	Transceivers





- Beam energy of 200 MeV and
- Flux, at maximum current of 10 nA, was 3.7×10^8 p*cm^{-2}*s^{-1}
- Run 1-6 targeted two ASICs and linPOL12V reaching ~3.3 kGy
- Run 7 (short) targeted the transceivers with 200 kGy

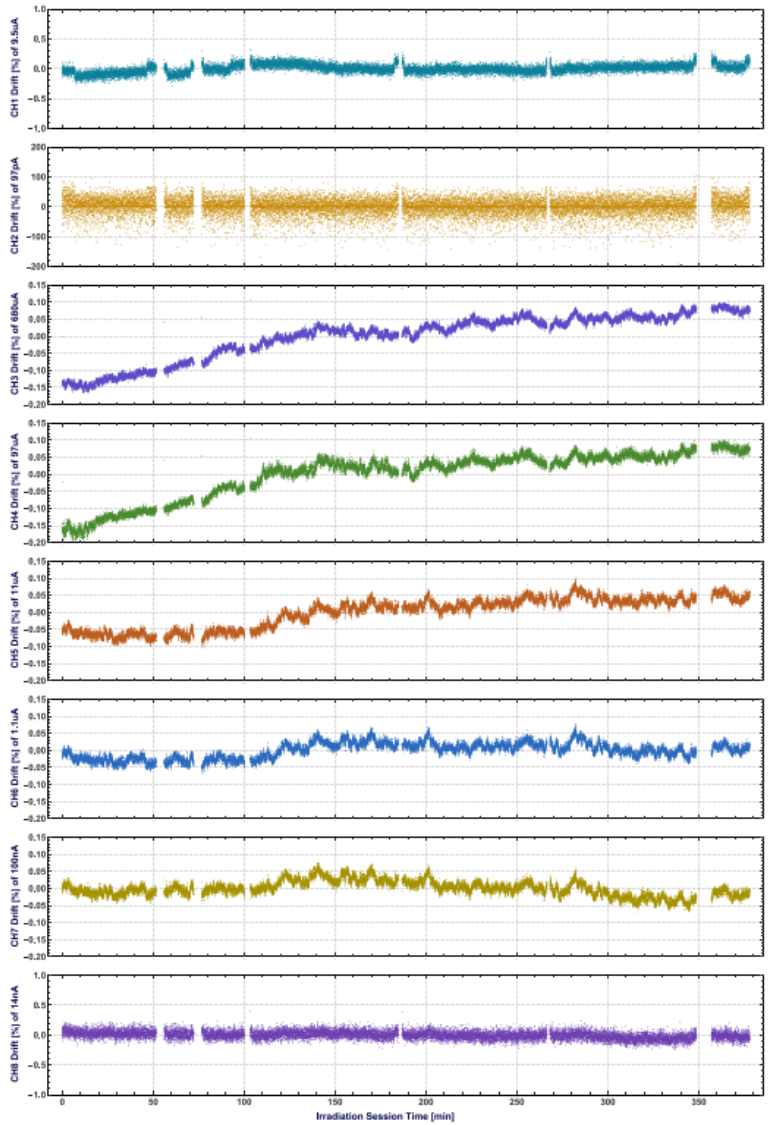
Irradiation – Protons (PSI)



Voltage (left) and Current (right) measurements of the supply rails

- The 1.2 V rail fluctuates into an interval of ≈ 3 mA. This is an intrinsic behaviour of the board that does not relate to radiation exposure nor to an abnormal condition
- No significant change observed. We conclude the onboard regulation is functional and has maintained stable supply throughout the session

Irradiation – Protons (PSI)



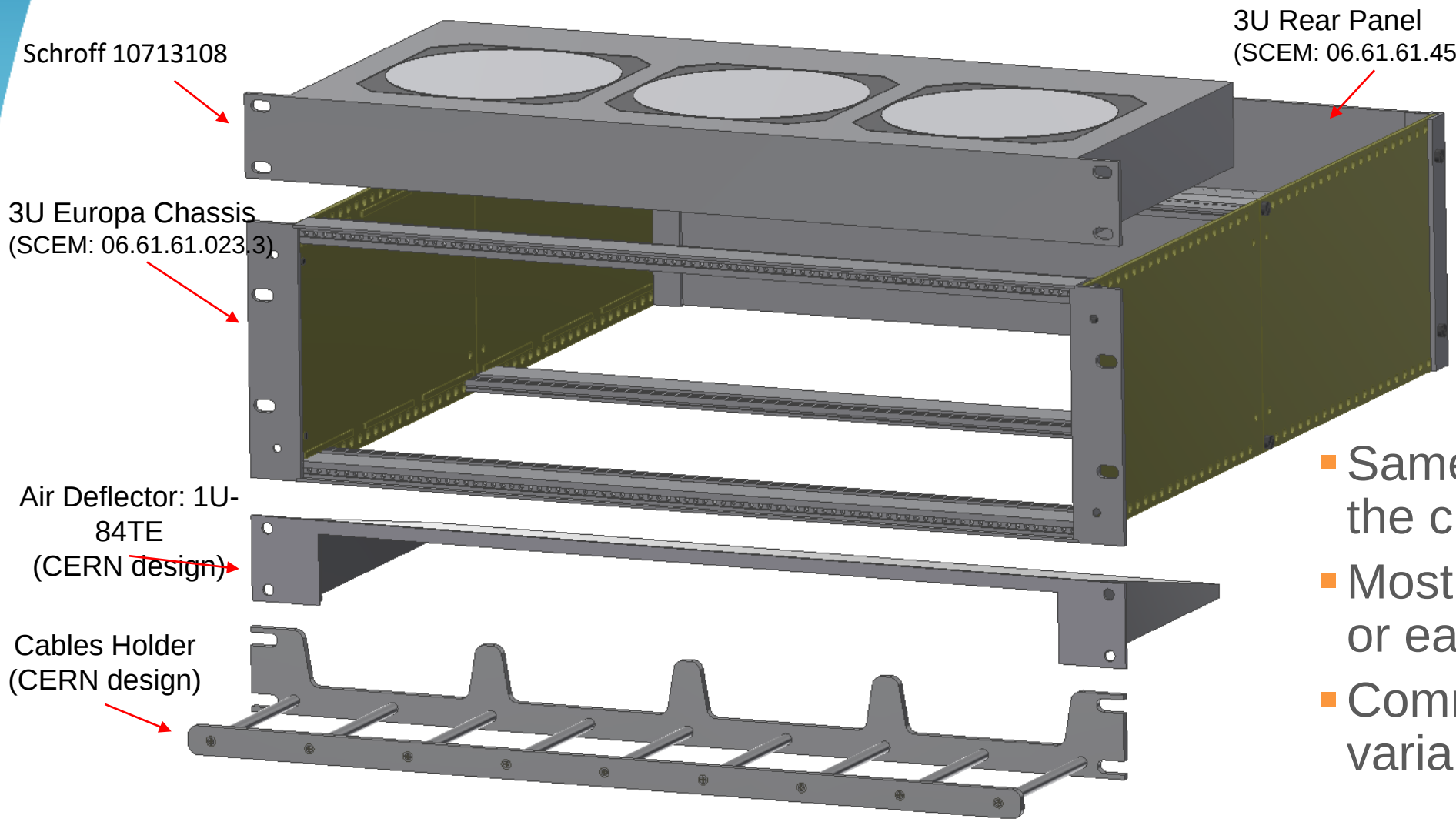
Percentage drifts of the current measurements during the irradiation session for each channel

- Channels 1-4 irradiated only
- Max. measurement deviations never exceed 0.5%

Digital domain check

- no errors detected in the 8b/10b coding and the frame parity check between the BLMASICs and the LpGBTs.
- continuity of samples was guaranteed
- no unexpected changes in the registers were observed in any BLMASICs.
- This means that even if SEUs might have occurred, the internal triple redundancy managed to mitigate it.

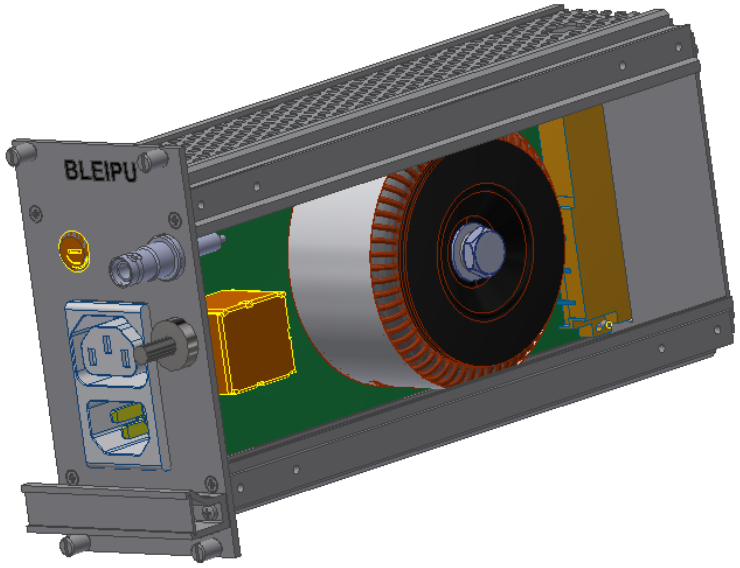
Tunnel crate: Mechanical parts



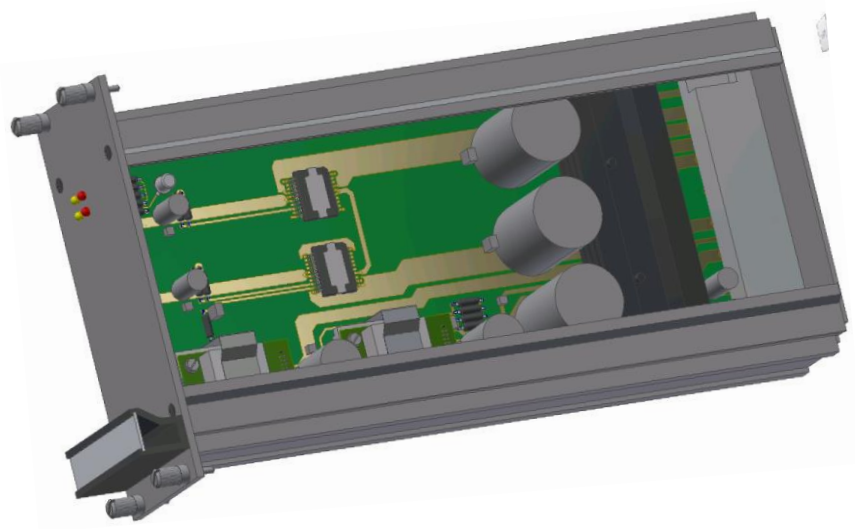
- Same part numbers with the current installation
- Most in the CERN store or easily procured
- Common parts to all variant designs

Power Supply Modules

- Input Power Unit (BLEIPU)
  - Front 230 VAC Inlet & Outlet
  - HV input connector
  - Rad-tol power transformer (custom design)

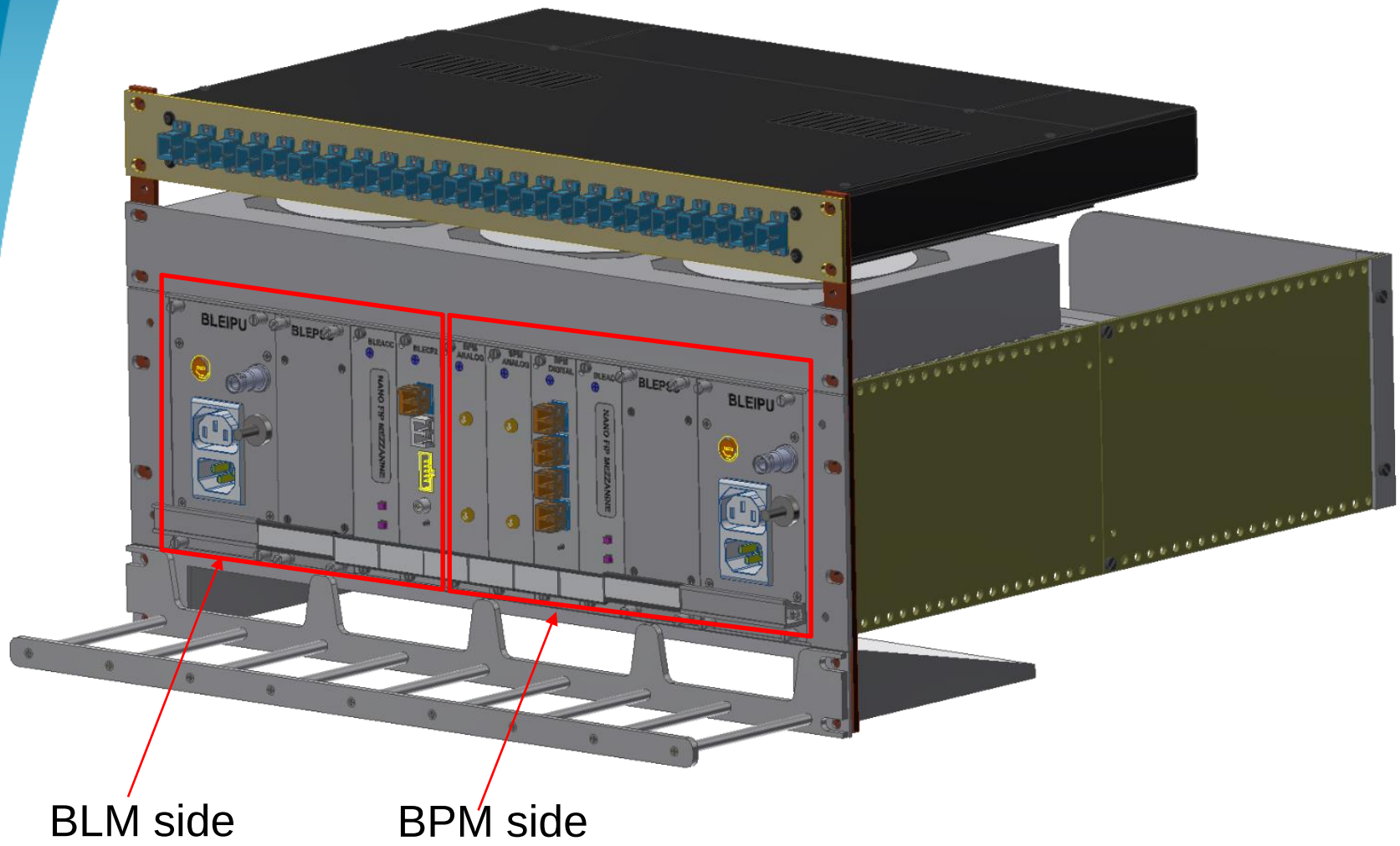


- Power Supply Unit (BLEPSU)
  - Schematic based on EDA-00691 (LHCPSU)
  - Generation of +5VDC, -5VDC, 2.5VDC and 1.5VDC
  - On/Off power supplies
  - Redesign ongoing due to obsolete components



See dedicated presentation at **RadWG Workshop** of 14/09/2022

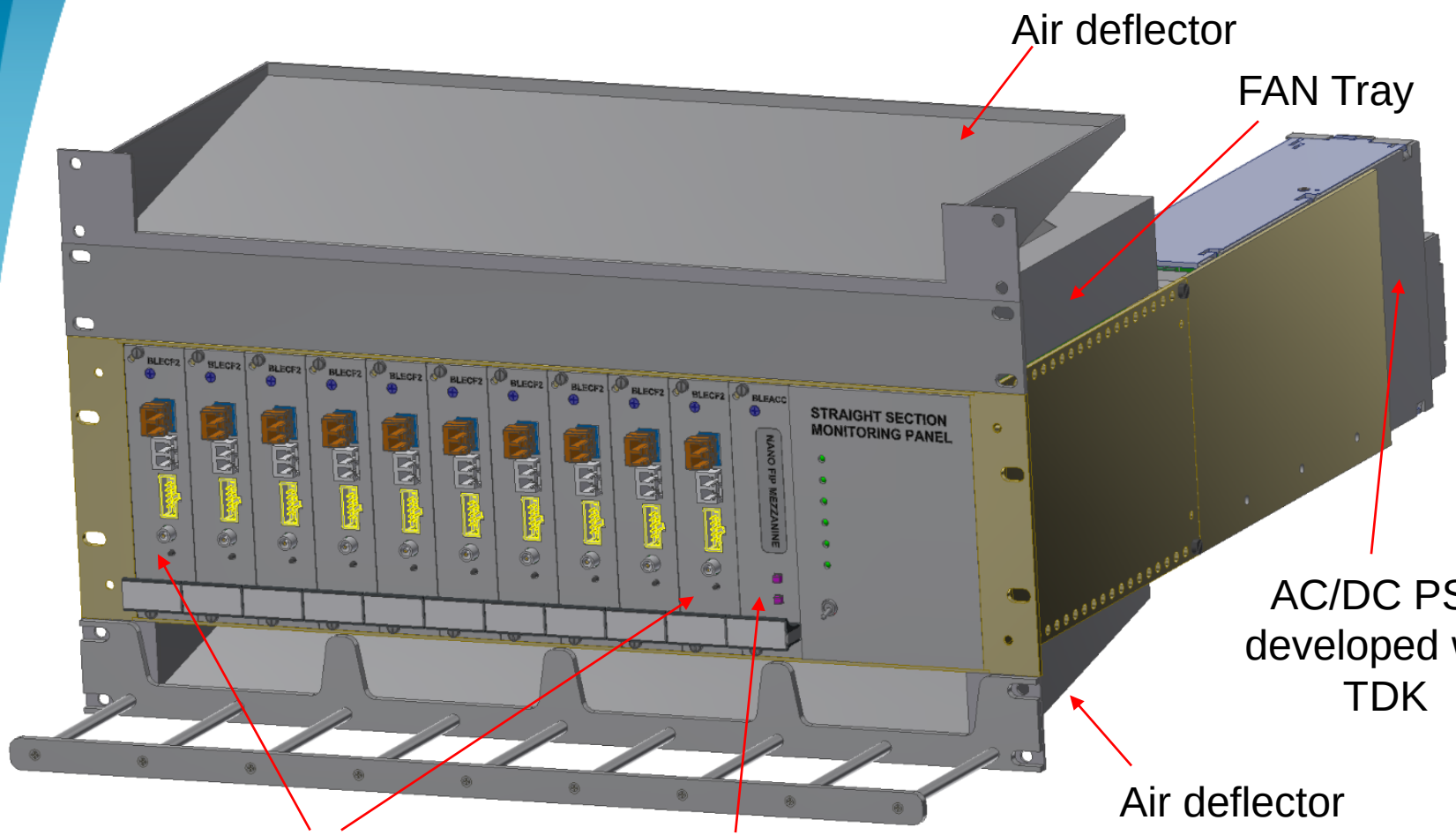
Common LHC (BPM & BLM) mini-crate



Characteristics:

- Common chassis
  - BPM & BLM shared
- Separate Power supply
  - Common part number
  - Isolate failures per system
- Separate backplane
  - Targeted design
  - Better cable management, i.e. for BLM 8x CB50 (coaxial) with BNC connectors & for BPM pass-through to digitiser

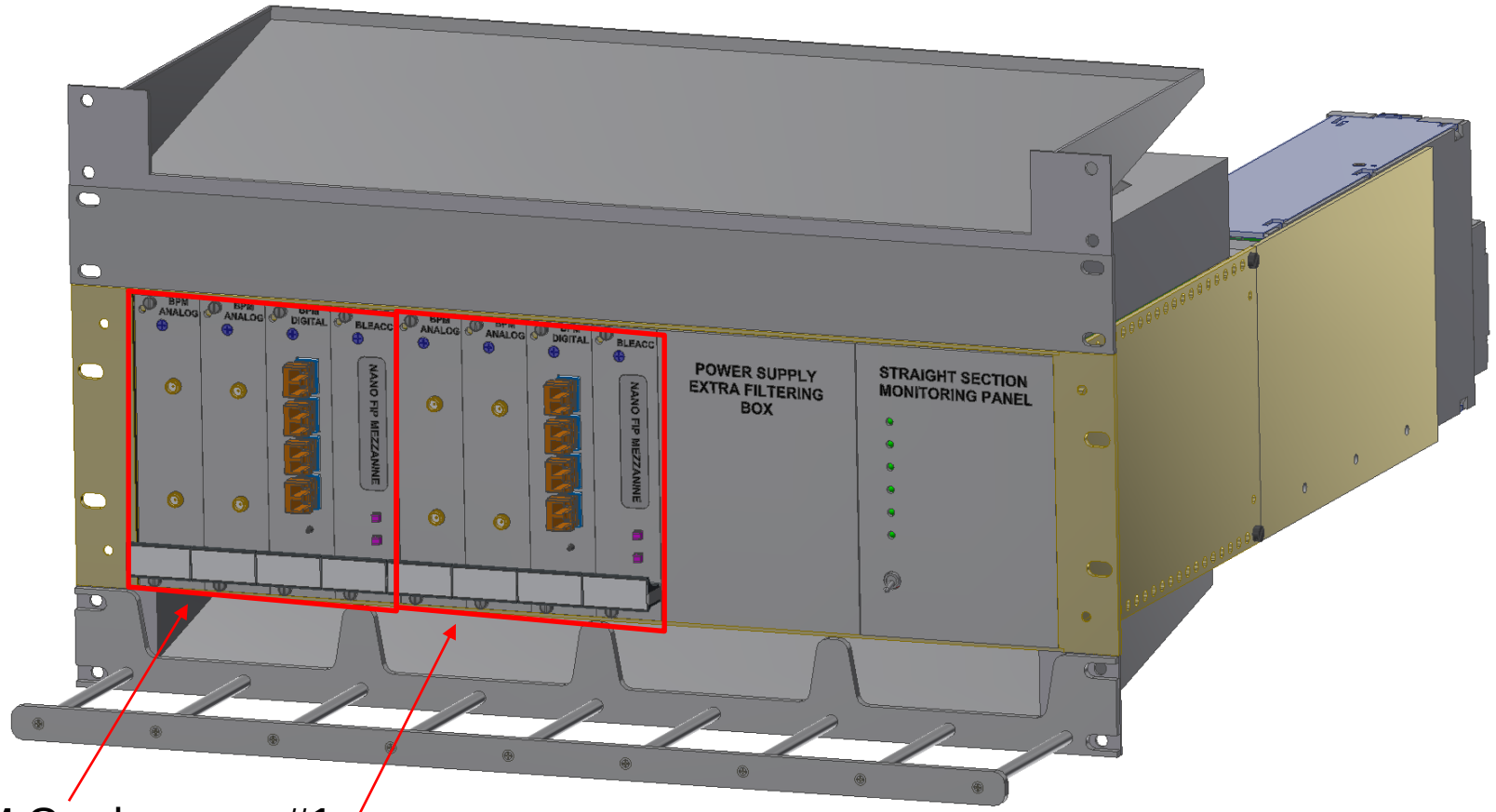
LHC BLM (LSS) mini-crate



Characteristics:

- Mini-crate inside a 45U rack
- Front connections
  - all modules and
  - all fibre connections
  - WorldFip
- Rear connections
  - All analogue signals
- Controller card
  - Redundant functionality
- Custom backplane
  - Targeted design
  - Completely passive
  - Better cable management, i.e. 10 x NES18 (multiwire) with Burndy connectors

LHC BPM (LSS) mini-crate

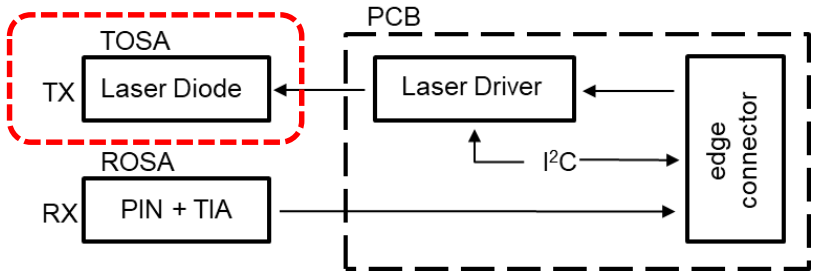


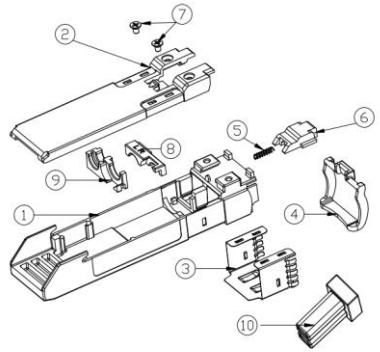
Characteristics:

- Front connections
  - all modules and
  - all fibre connections
  - WorldFip
- Rear connections
  - none
- Controller card
  - Unique functionality, i.e. control and re-programming
- Filtering module
  - Foreseen for the case COTS power supply too noisy.
- Custom backplane
  - Targeted design
  - Completely passive

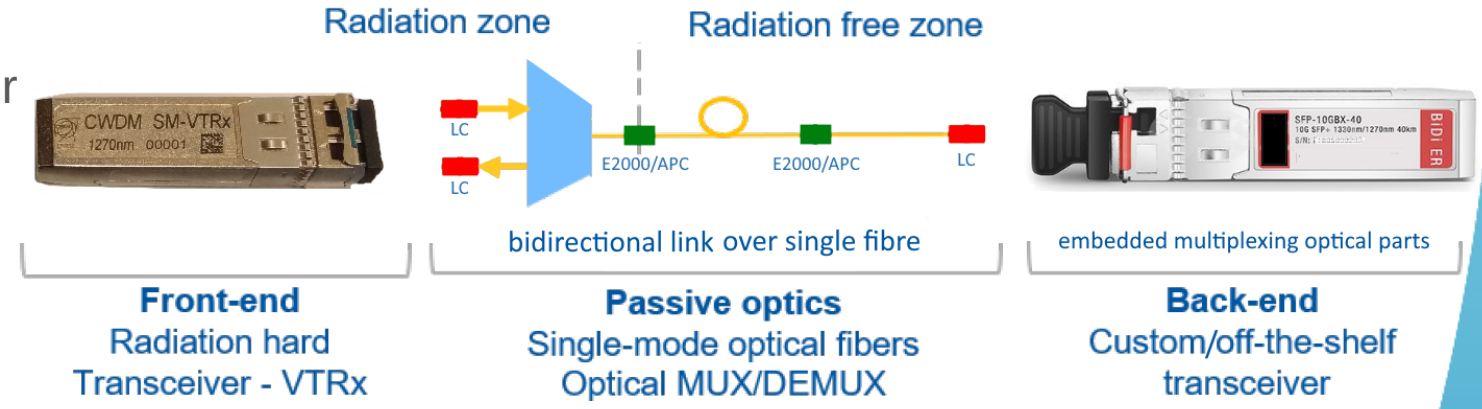
Rad-Tol Communication Layer

- Single-mode Versatile Link Transceiver - VTRx





- Custom design for SY-BI by EP-ESE
- Directly compatible with the LpGBT serialiser
- Bidirectional; operating from 4.8 to 10 Gbps
- Enclosed in SFP format
- Prototype qualified to 10 kGy

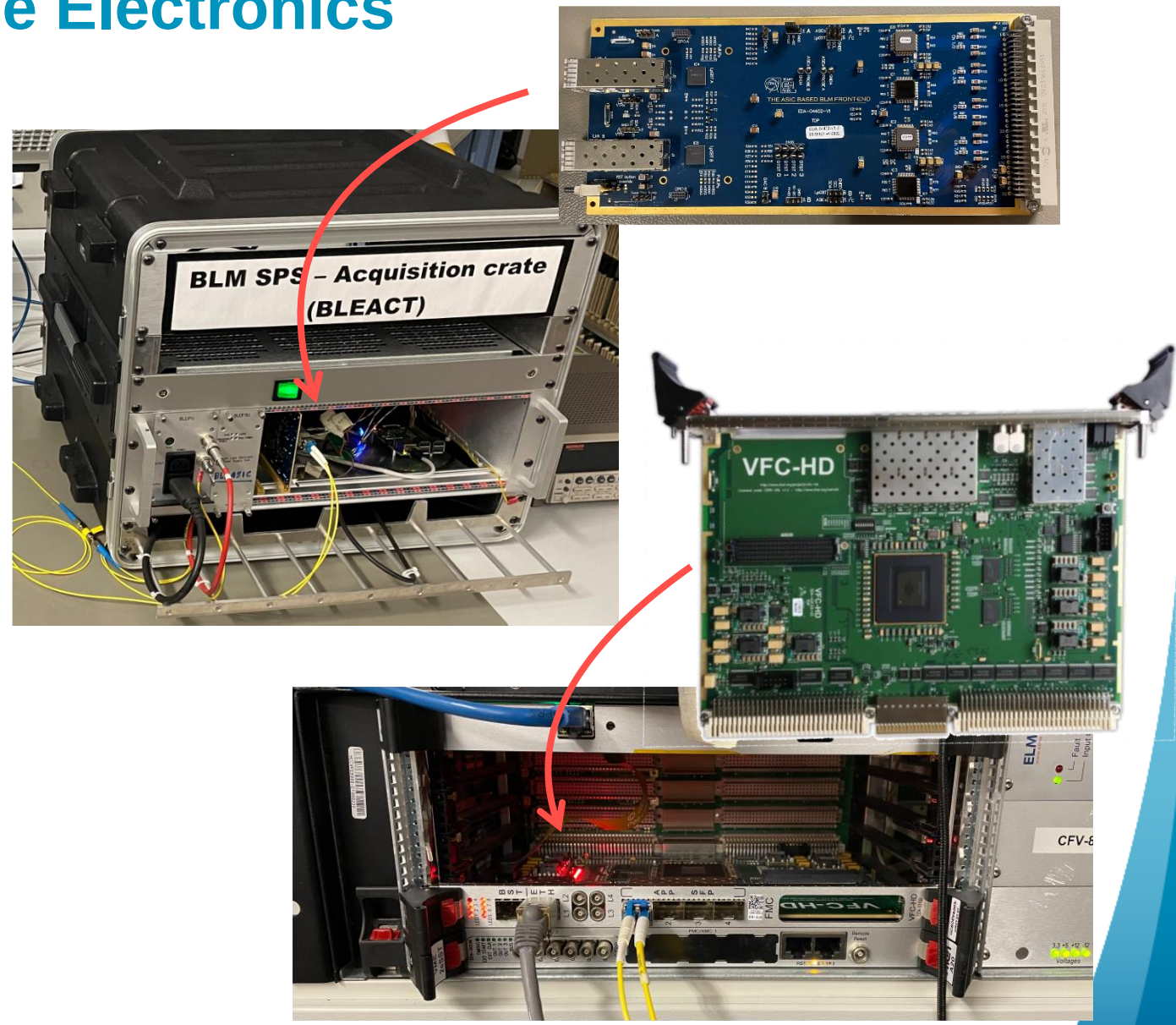


MS-4730/EP/ESE did not succeed / TOSA manufacturer retracted; new parts under qualification;
All other parts are being ordered and driver ASIC in manufacturing.

Surface Electronics

Integration to the acquisition & processing crates started

- Firmware development (back-end) needed for
  - Boot, setup and control over fibre link of the BLEIC
  - Reception & decoding of the measurement packets
  - On-demand self-diagnostic data
  - Real-time processing & onboard high frequency data recording



Conclusions & Acknowledgements

Summary

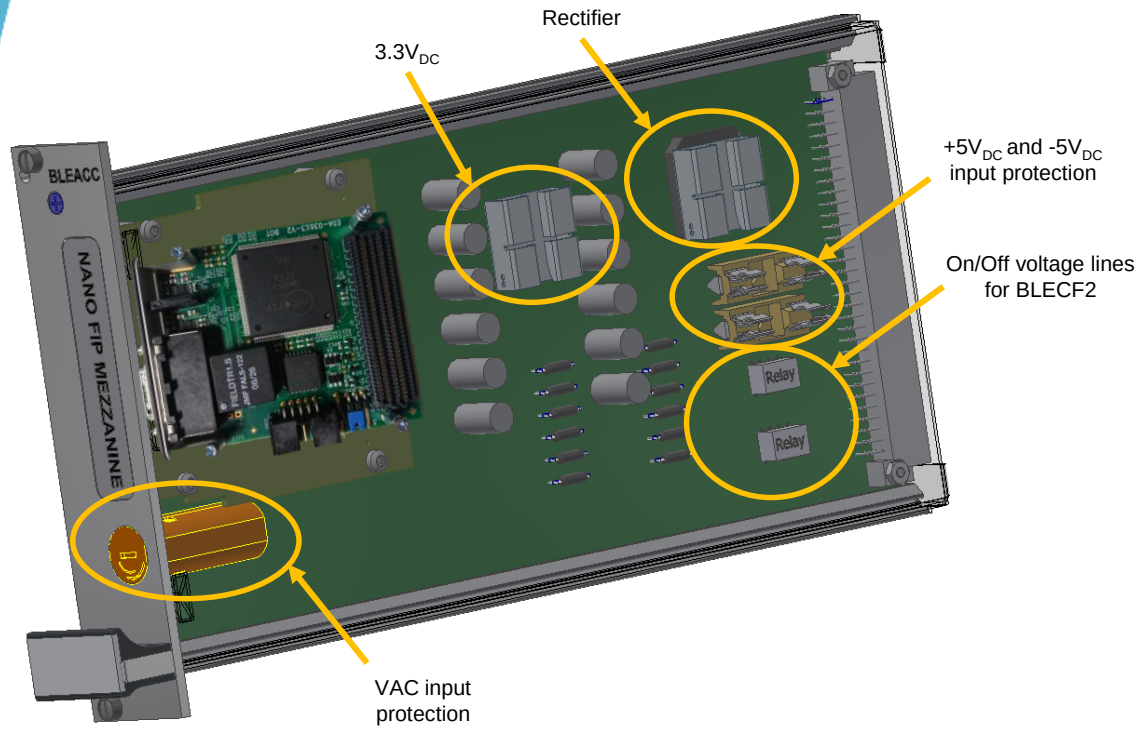
- Dedicated ‘Application-Specific IC’ (ASIC), currently testing v3
  - Extensive qualification for performance and radiation (X-Ray, protons and mixed-field) resistance almost complete
  - Significant cost optimisation with 5x fewer components than standard BLECF boards
- New prototype PCB design complete
  - Includes all functionalities expected from the final system
  - Prototypes of the other custom parts, e.g. the SM-VTRx and LpGBT have been secured
- New crate design (three variants) ready for production
  - Power supply redesign on-going due to obsolete rad-hard components
- Work started on system integration
  - Development of back-end firmware for communication and control
  - Next step, integration in the real-time data processing and decision making
- Next steps
  - Final review in Q1 2023 with ASIC fabrication expected in 2023-4
  - Agree on IC detector production funding (missing in-kind) & plan

Acknowledgements

- ADC & ASIC Production
  - Kostas Kloukinas
- BLMASIC
  - Jan Kaplon
  - Luca Giangrande
  - Pedro Vicente Leitao
- LpGBT
  - Daniel Hernandez Montesinos
  - Paulo Moreira
- SM-VRTx
  - Jan Troska
  - Carmelo Scarcella
  - Leonardo Marcon
- Fibre & Copper connections
  - Jeremy Blanc
  - Daniel Ricci
- Rad-Tol COTS
  - Rudy Ferraro
  - Salvatore Danzeca
- R2E
  - Giuseppe Lerner
  - Ruben Garcia Alia
- IC Manufacturing
  - Nicolas Sebastien Chritin
  - Thibaut Coiffet
  - Alessandro Dallocchio

Spare Slides

Crate Control Module (BLEACC)

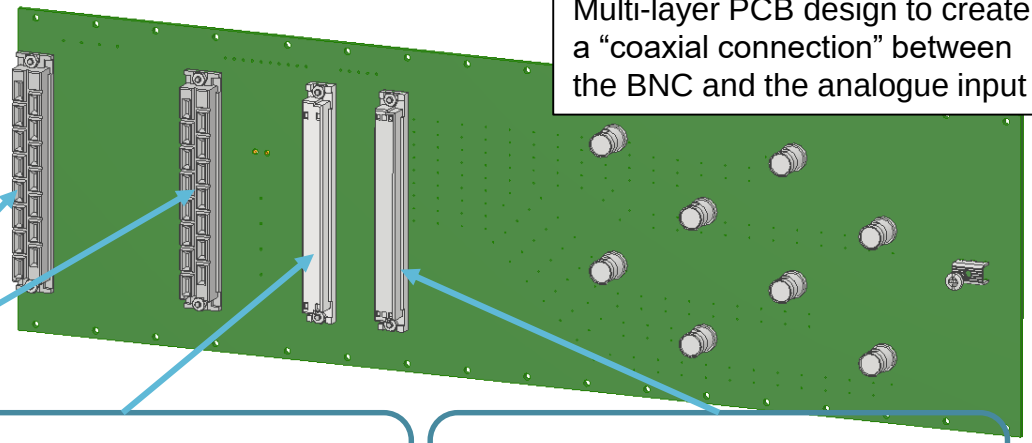


Design in collaboration with BE-CEM

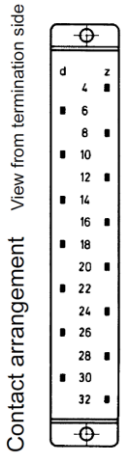
- Carrier to host the nanoFIP mezzanine
- Functionality:
  - Pass commands to acquisition module
  - Power cycle the acq. module through the PSU
  - Diagnostic collection for the PSU statuses
- New functionalities under design
  - Deliver bitstream & re-program FPGA

Backplane template

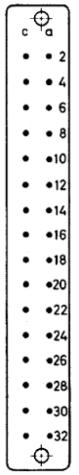
- PCB thickness = 2.2mm
- PCB materials = FR4
- Copper thickness = 35µm

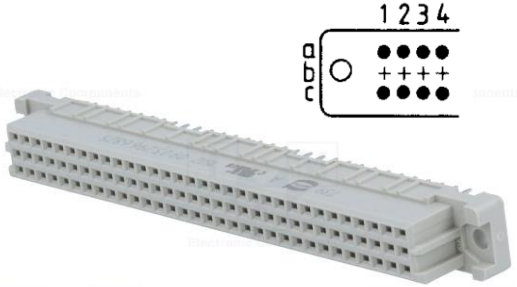


BLEIPU and **BLEPSU** connectors
(SCEM: 09.61.41.565.4
Harting: 09 06 215 2821)



BLEACC connector
(Harting: 09 04 232 2831)





BLECF2 connector
(Harting: 09 03 264 2825)

Best connector IEC 60603 class 1 (mating times up to 500)

Module Connectors

Connector selection to prevent erroneous module swap

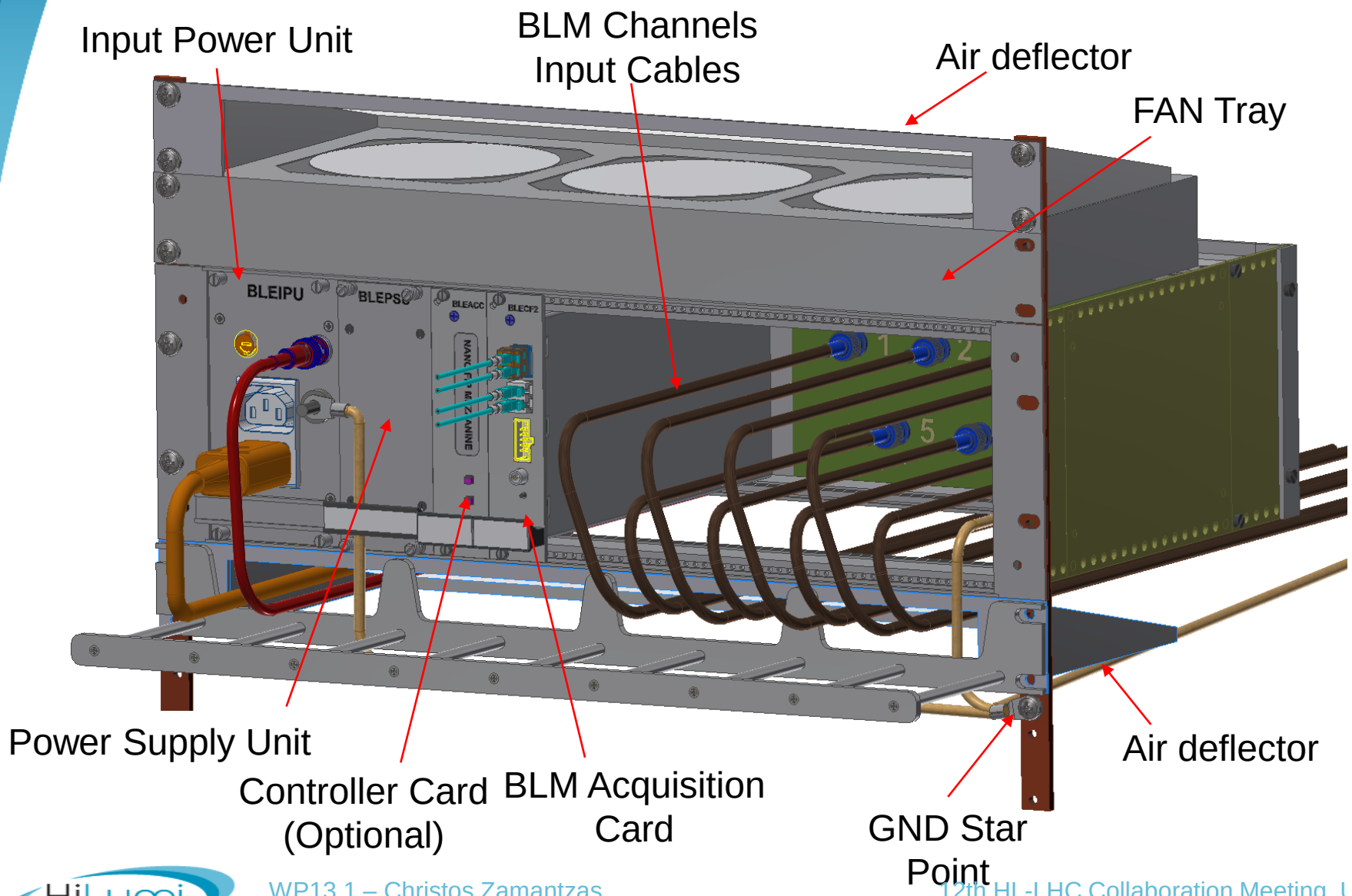
BLEPSU & **BLEIPU** connector
Harting: 09 06 115 2911

BLEACC connector
(SCEM: 09.61.36.015.4
Harting: 09 04 132 2921)

BLECF2 connector
(Harting: 09 03 164 2921)

Size difference prevents accidental swap between them.

SPS BLM mini-crate



Characteristics:

- Front access
  - SPS specific requirement
  - Applies to all connections and modules
  - Allows mini-crate to be installed at the wall side
- Controller card
  - Redundant functionality
  - Missing infrastructure at SPS
- Custom backplane
  - Targeted design
  - Completely passive
  - Better cable management, i.e. 8x CB50 (coaxial) with BNC connectors