WP18: Radiation-tolerant DI/OT platform

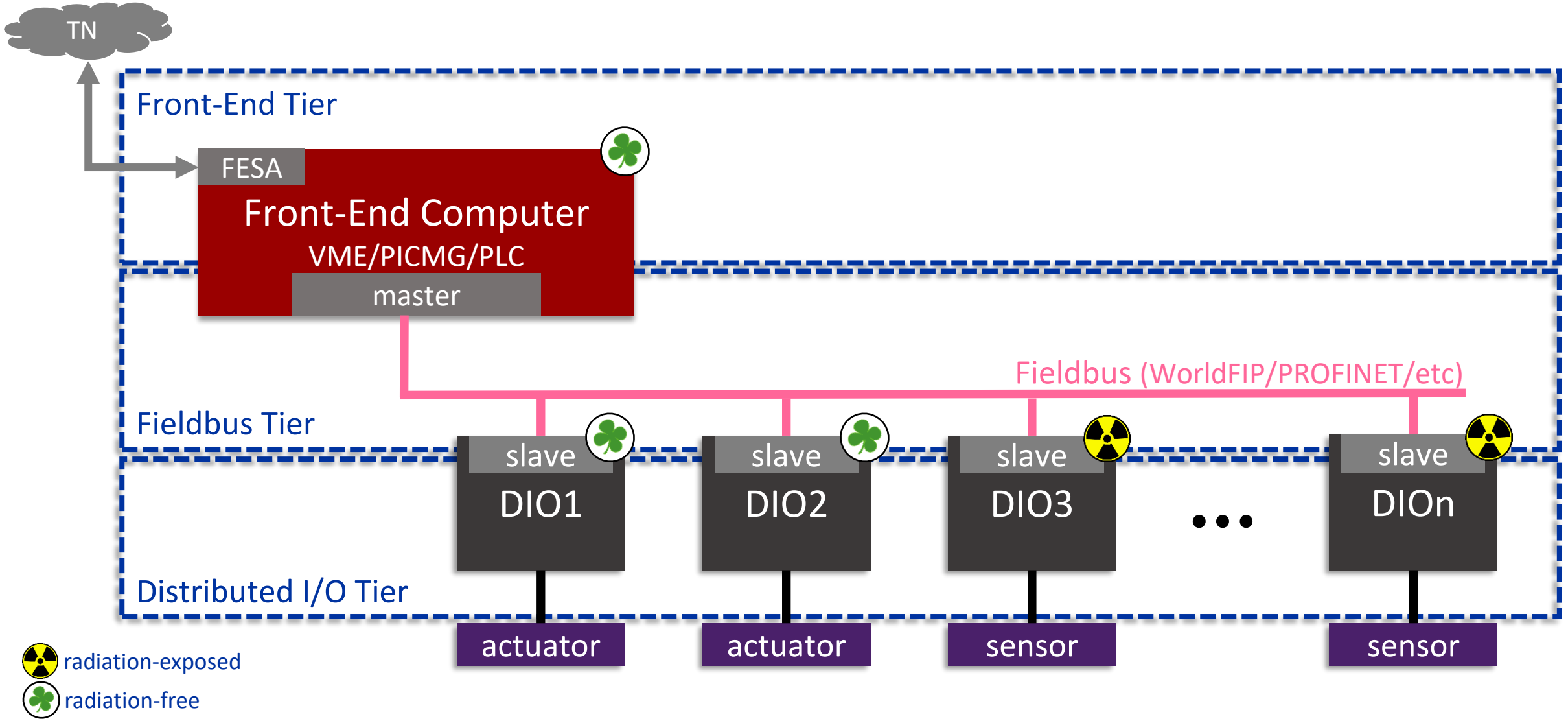
Greg Daniluk (BE-CEM)

on behalf of DI/OT team

12th HL-LHC Collaboration Meeting

21 Sep 2022

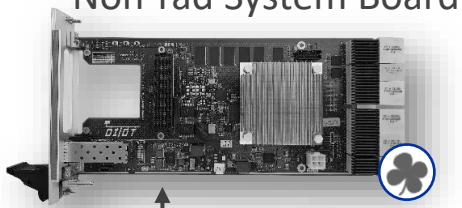
Custom electronics architecture



DI/OT project

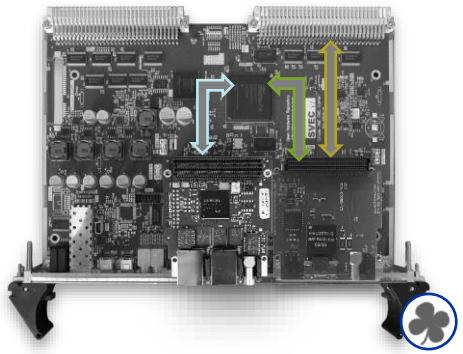
HiLumi HL-LHC PROJECT WP18

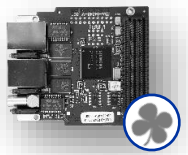
Non-rad System Board



Rad-tol System Board

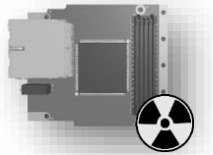
ProFIP





Profinet

WorldFIP



Powerlink

Reliability analysis

Validation tests

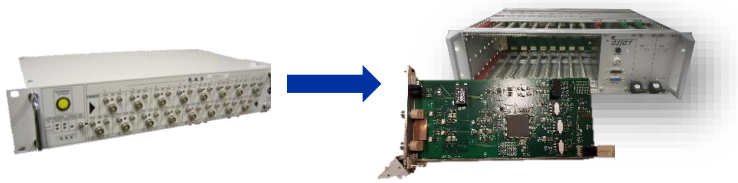
Production Tests (PTS)

Environmental Stress Screening

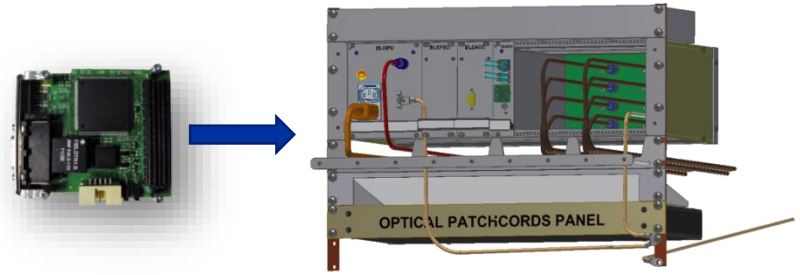
Reliability demonstration

Applications of rad-tol DI/OT

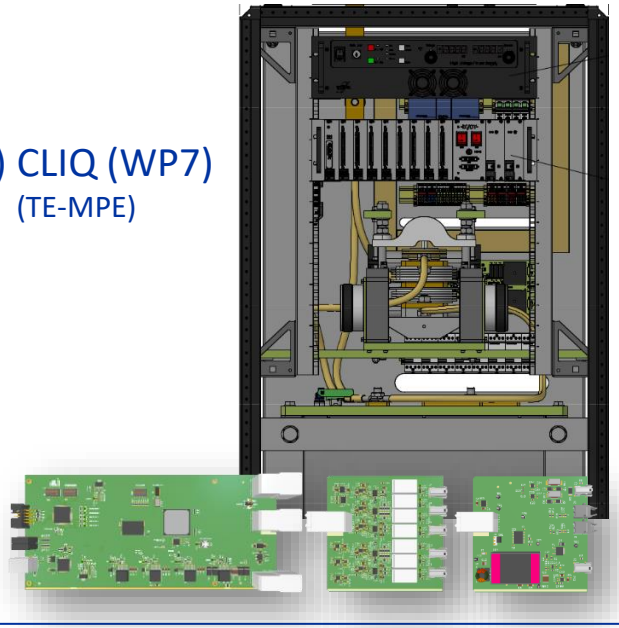
1) Wire Positioning Sensors (WP15.4)
(BE-GM)



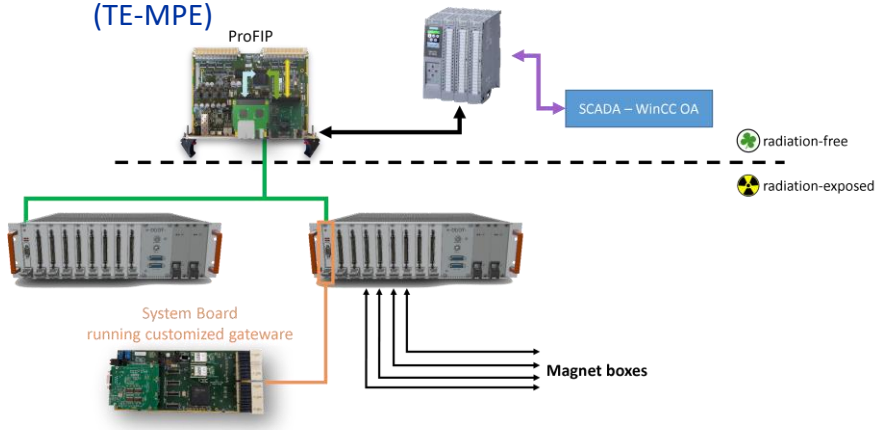
2) BLM & BPM electronics (WP13)



3) CLIQ (WP7)
(TE-MPE)



4) WIC v2
(TE-MPE)



Locations and radiation levels

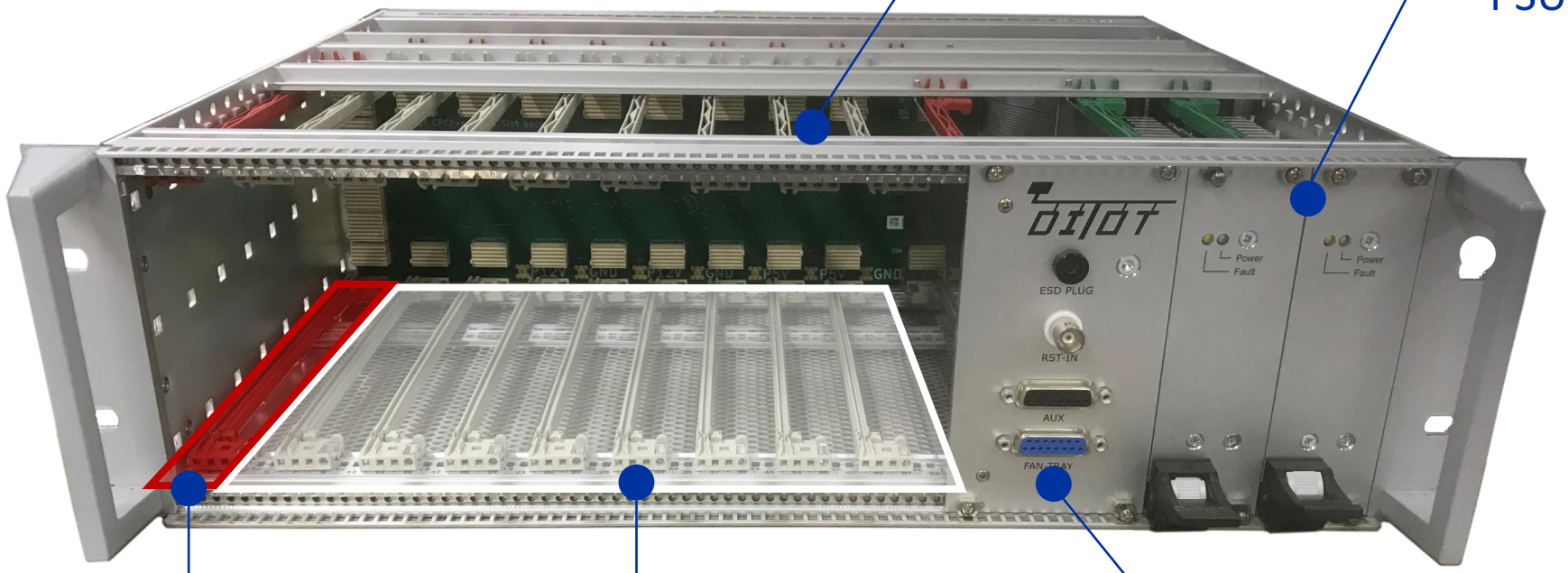
- RRs *3/*7 in P1, P5, P7
- UAs 13/18/53/57
- Transfer lines: Ti2, Ti8, TT41-43

Annual HL-LHC radiation levels[1]

	TID [Gy]	HEH [cm^{-2}]	1MeVn-eq [cm^{-2}]
RR13-17-53-57 L1	25	$1.4 * 10^{10}$	$7 * 10^{10}$
RR13-17-53-57 L0	15	$1 * 10^{10}$	$7 * 10^{10}$

[1] *EDMS No. 2302154 V1.0 Radiation Level Specifications for HL-LHC*

3U Crate



Produced by:

creo TECH Instruments S.A.

ELMA Your Solution Partner

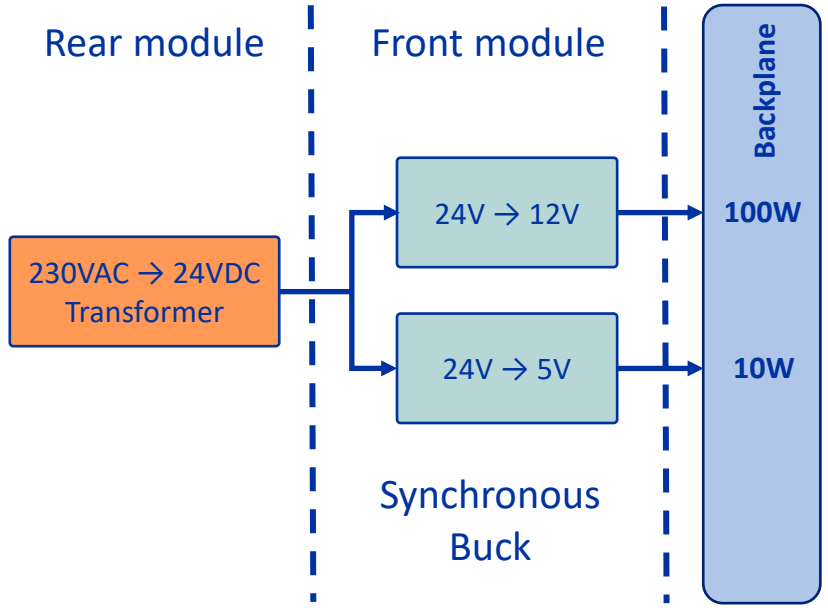
nVent SCHROFF

Fan Tray


3x San Ace 9G1212G101
Tested up to 500Gy
FAN TRAY
DIDT
12V, 5V, PMBus
Monimod-FanTray

RaToPUS v2

- Split in two modules



RaToPUS v2

- Split in two modules
- RaToPUS-Rear: 230VAC → 24VDC
  - Transformer + rectifier
  - 24VDC is industrial standard voltage

P. Peronnard

RaToPUS v2

- Split in two modules
- RaToPUS-Rear: 230VAC → 24VDC
  - Transformer + rectifier
  - 24VDC is industrial standard voltage
- RaToPUS-Front: 24VDC → 12VDC; 24VDC → 5VDC
  - Simpler, non-isolated
  - Synchronous buck topology for both DC/DC
  - Reduced BOM, already qualified for RaToPUS v1
  - Relaxed voltage constraints on MOSFETs
  - Better efficiency of DC/DC stages

P. Peronnard

RaToPUS v2

CHARM tests

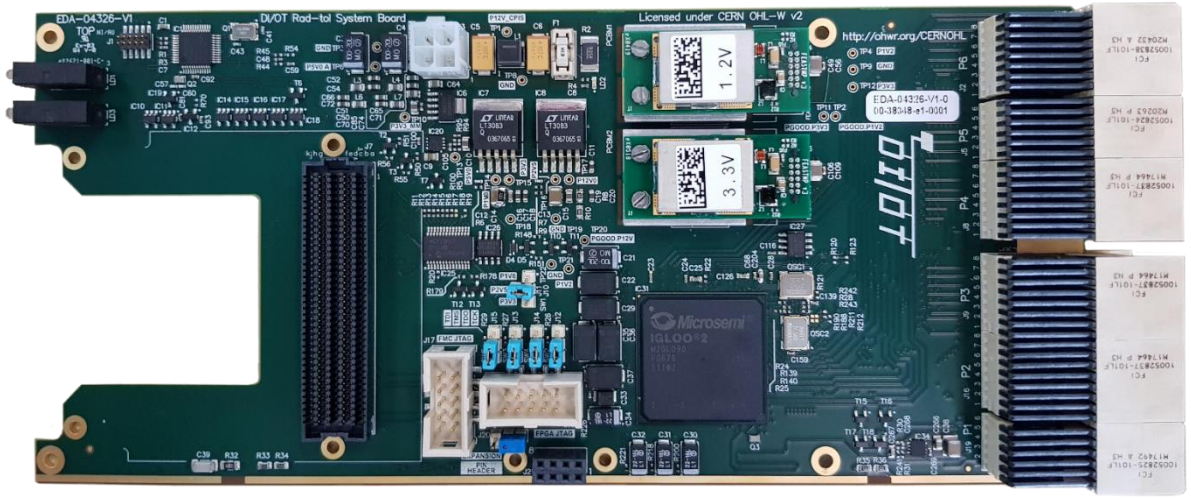
- 3 radiation campaigns of DC/DC front stage so far (2 + 2 + 2 units) in CHARM position 13

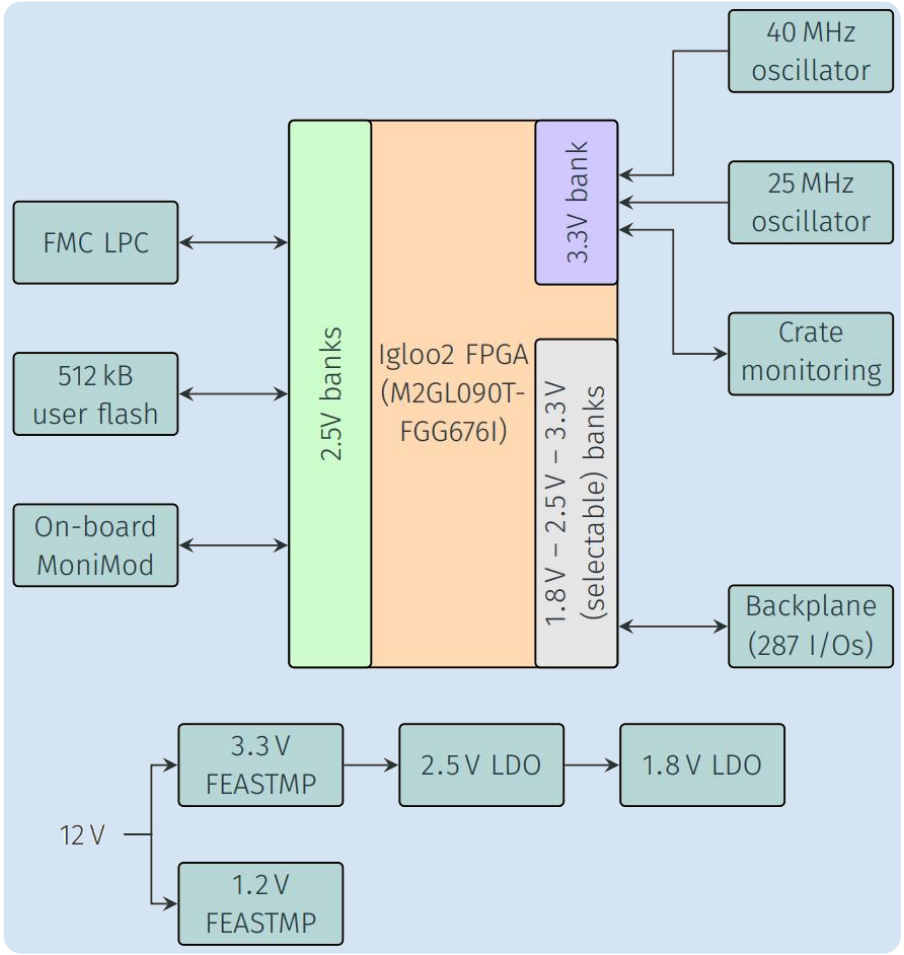
RaToPUS v2
CHARM tests

- 3 radiation campaigns of DC/DC front stage so far (2 + 2 + 2 units) in CHARM position 13
- Campaign 1:
  - Observed early failure of PWM controller *UC2843* -> decision to go back to *TL2843*
  - TL2843 initially excluded due to misbehaviour >65 °C
  - … but in RaToPUS v2 heat dissipation is no longer an issue (contrary to v1)
- Campaign 2:
  - Both units survived **620Gy**
  - Failure due to *TL2843* internal reference
- Campaign 3:
  - Tested synchronous rectification
  - … but both units failed ~200Gy (short in rectification MOSFET, probably due to *NCP5183* MOSFET driver failure)
- (Future) Campaign 4:
  - AC/DC rear stage
  - DC/DC front stage: use external voltage reference instead of internal TL2843 reference.

System Board

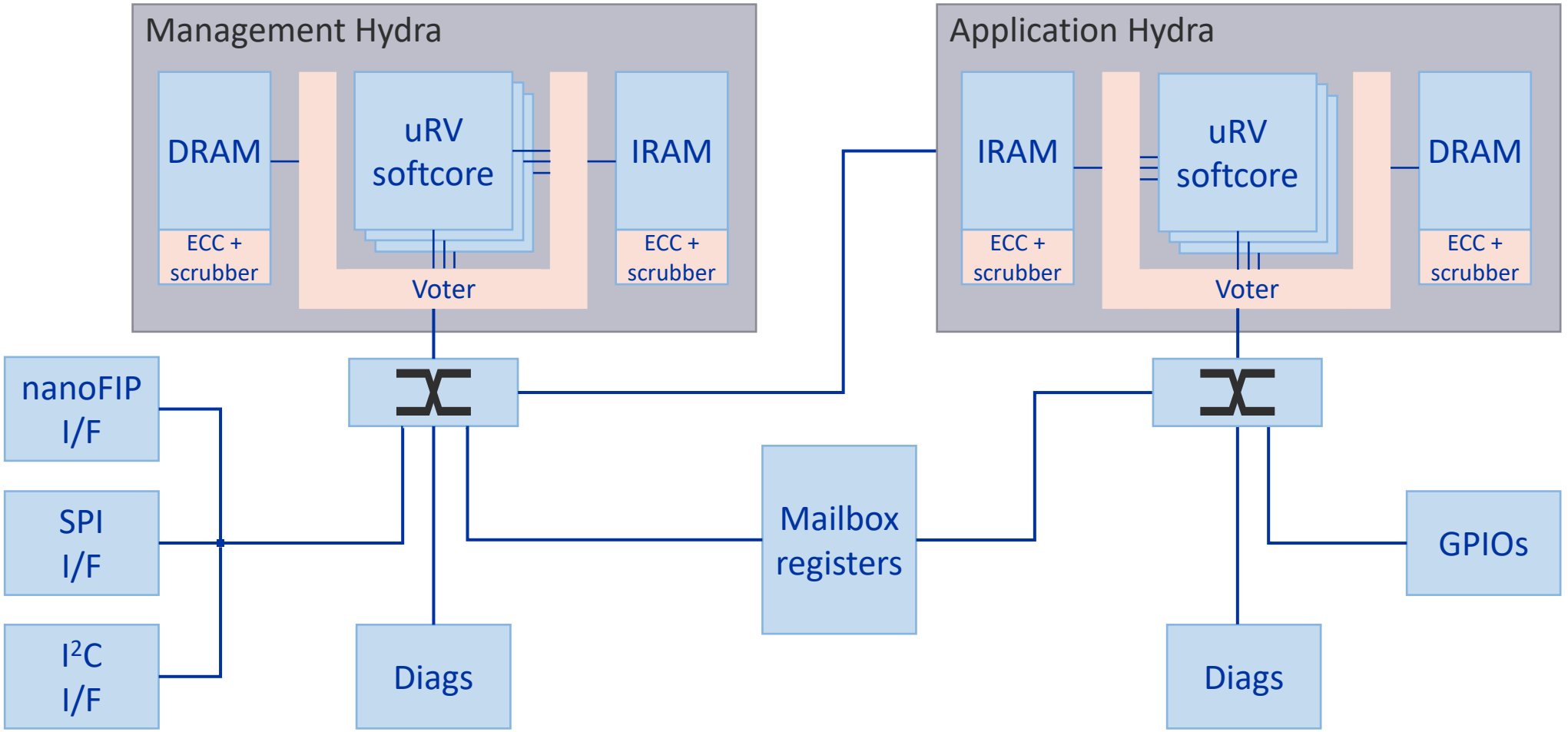
- Crate control + communication via FMC
- Based on IGLOO2 FPGA
- Powered by FEASTMP (to be replaced with bPOL12V)
- Successful functional validation





C. Gentsos

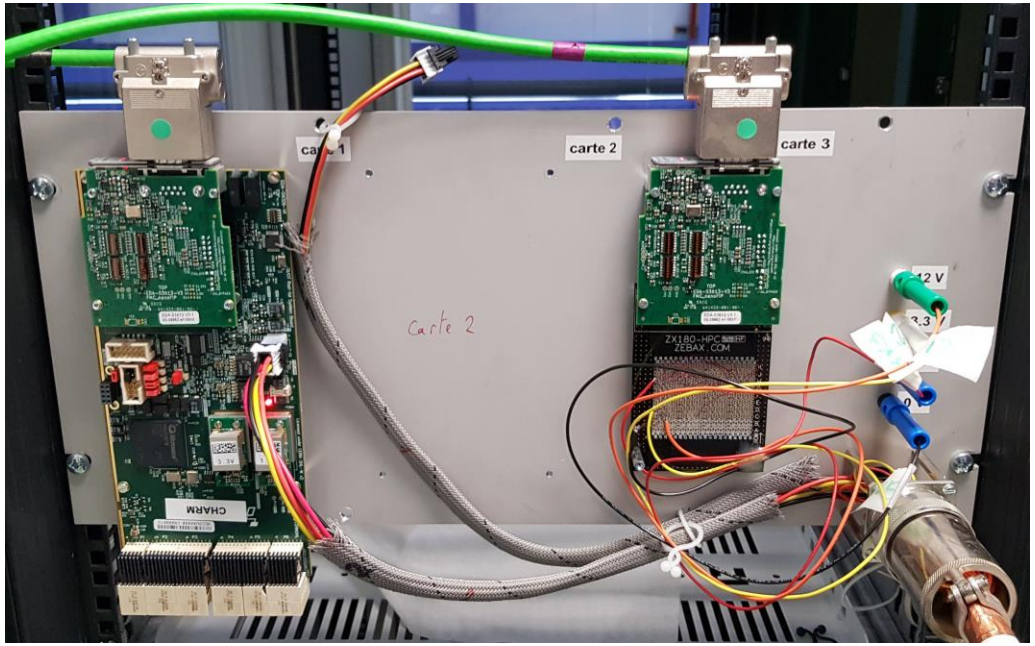
System Board reference gateware



T. Gingold

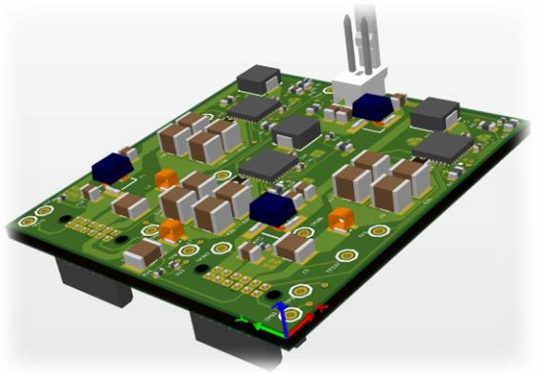
Hydra & System Board irradiations

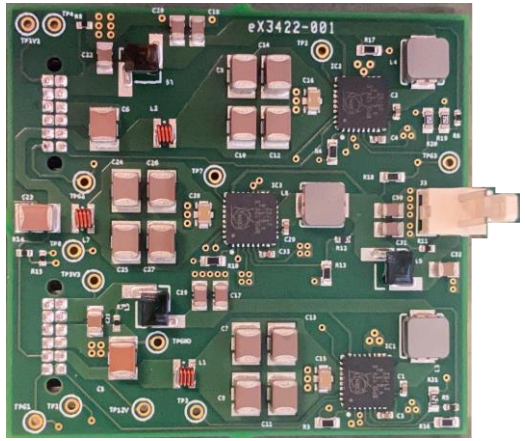
- 2 radiation campaigns (1+1 unit) in CHARM position 13
- The only hardware failure in both campaigns: *LT3083* after ~200Gy
  - Will be replaced with bPOL12V
- Campaign 1:
  - many power cycles due to Hydra freezes
- Campaign 2:
  - No freezes in Management CPU until 500Gy
  - > 2500 single errors corrected in RAM; no double errors
  - Many Application CPU freezes (which was purposedly not block-TMRed)
  - 4 power cycles due to Monimod hangs (power cycling circuit?)



Hydra & System Board irradiations

- (Future) Campaign 3:
  - 3-bPOL12V module to replace FEASTMPs and LT3083
  - Block-TMR for Application CPU
  - Additional Application CPU to test ECC in register file (no Block-TMR)
  - Investigate power control of ATSAMD21 (Monimod)

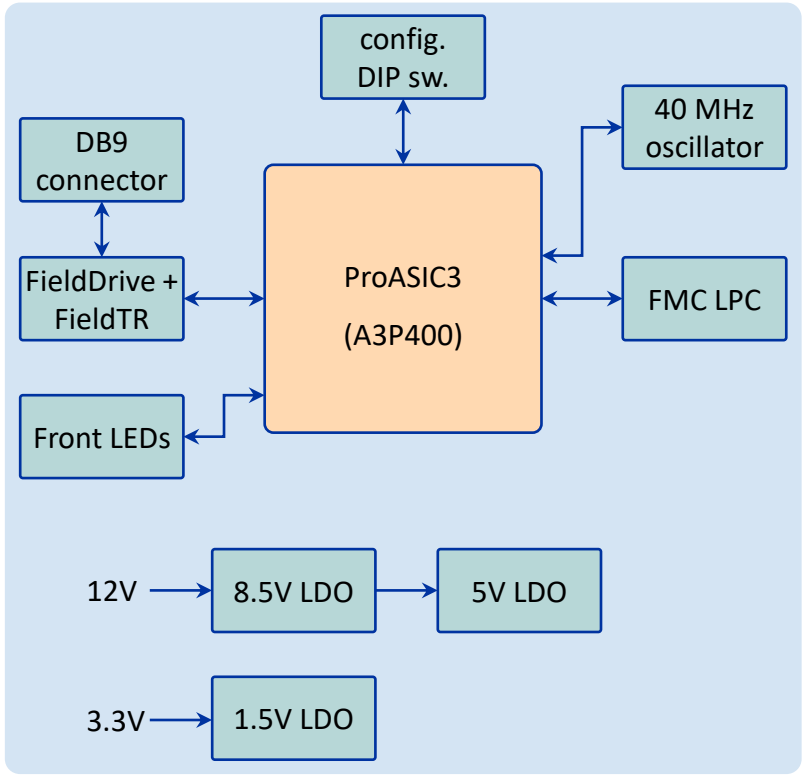




FMC nanoFIP

- WorldFIP communication up to 2.5Mbps
- Based on nanoFIP @ ProASIC3
- Support for hosted and standalone modes
- Successful v3 redesign and prototype validation

- 4 units irradiated at CHARM position 13
  - 2x 2.5Mbps in stand-alone mode on a passive carrier
    - First data errors at 494Gy and 550Gy
  - 2x 1Mbps in memory mode on DI/OT System Board
    - No data errors until 518Gy



Summary

- **Modular** platform for **custom** electronics for HL-LHC
- Based **on 3U crate with standardised, generic modules**
- **Final** design phase
- **Functionality** of all hardware prototypes successfully validated
- Numerous **CHARM tests performed** with very good results
- Remaining **improvements and radiation validation** until the end of 2022

https://ohwr.org/project/diot/wikis