Symmetrical quench detection and QDS threshold management for HL-LHC

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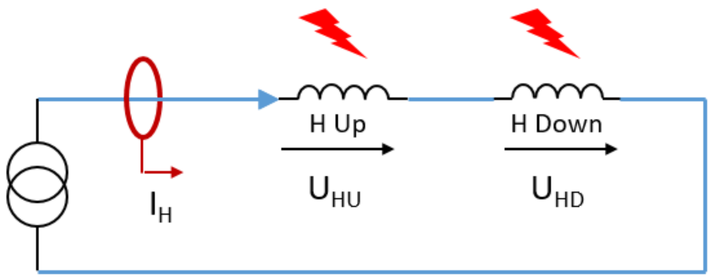
Outline

- **Symmetric quench detection for HL-LHC magnet circuits**
  - Inner Triplet
  - D1
  - D2
  - IT correctors
  - D2 correctors
  - Summary
- **Configuration management for HL-LHC QDS**
  - Digital quench detectors
  - Proposed solution
  - Summary

Symmetric quenches in a nutshell: definition

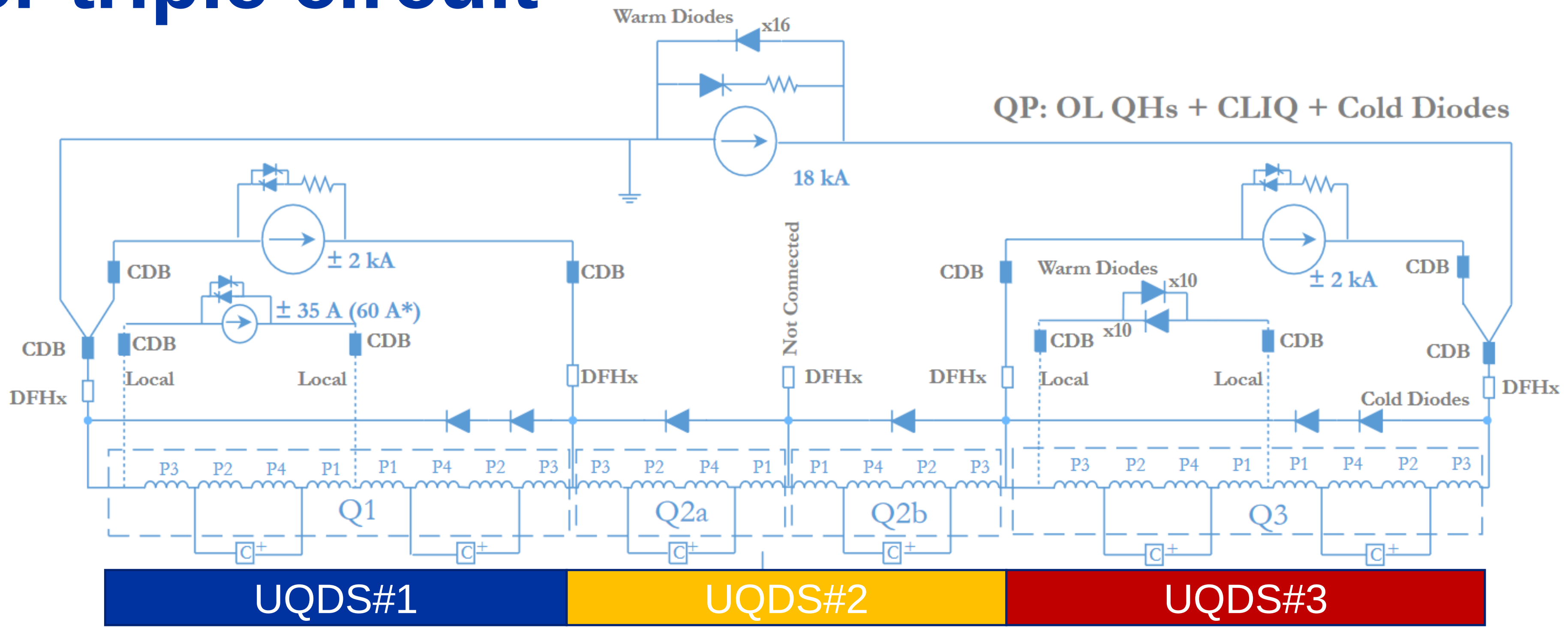
- **From quench detection point of view a quench is considered symmetric if multiple observed parts of the magnet quench in a simultaneous way**
- **Bridge type quench detectors or simple comparison will not detect in a reliable way**
- **Symmetric quench detection algorithms can be deployed in addition* to standard QD, allowing different thresholds**



$U_{quench} = U_{HU} - U_{HD}$ → insensitive to quench voltage if present on both coils

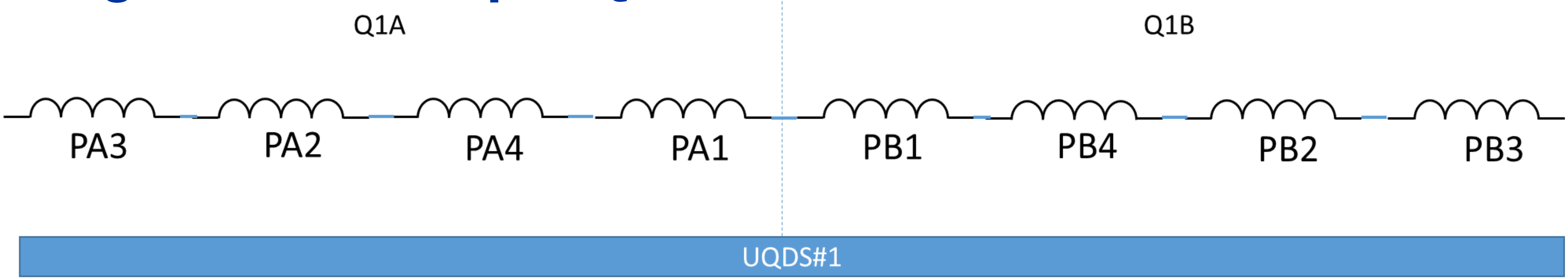
* Except for MCBRD

Inner triple circuit



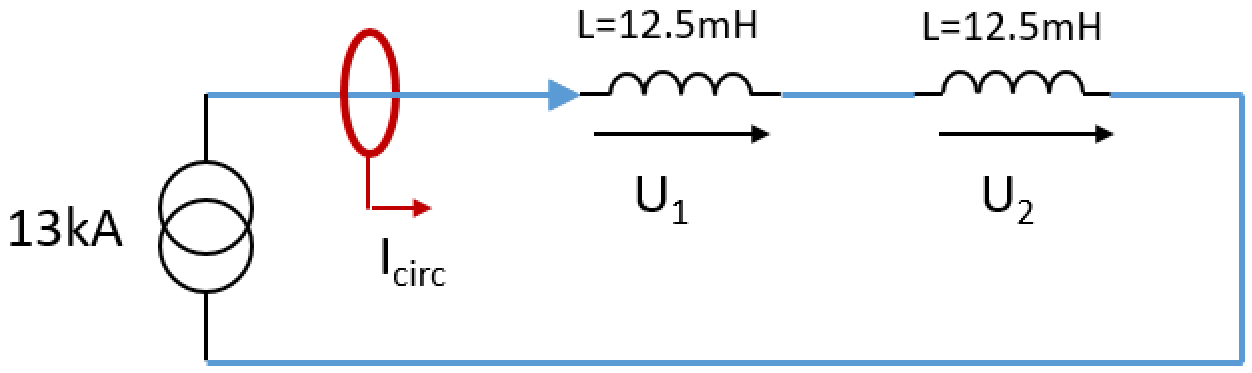
- **Each UQDS observes all magnet poles with identical current (except Q1)**
- **Comparison among poles detect asymmetric and symmetric quenches (Simultaneous quench of 8 consecutive poles considered extremely unlikely)**

Inner triplet circuit symmetric quench detection algorithm example Q1



- **Within one magnet, compare poles of the two magnet halves which each other: PA3 - PB3, PA2 - PB2, PA4 - PB4, PA1 - PB1**
- **Due to trim in Q1A, inductive voltage per pole can differ up to +/-28.64mV per pole between Q1A and Q1B (Based on max di/dt of 3.32A/s and 8.625mH pole inductivity)**
- **This would be still compatible with a threshold of 100mV.**
- **Additional comparison within Q1A and Q1B could run with a lower threshold**

D1 circuit



di/dt max: 12 A/s
$Uind_{max}$: 150 mV

- **Only two pole voltages accessible,**
- **Two solutions for symmetric quench detection**
  - Absolute voltage detection: if any pole voltage exceeds 200mV
  - L*di/dt algorithm

D1 symmetric quench detection

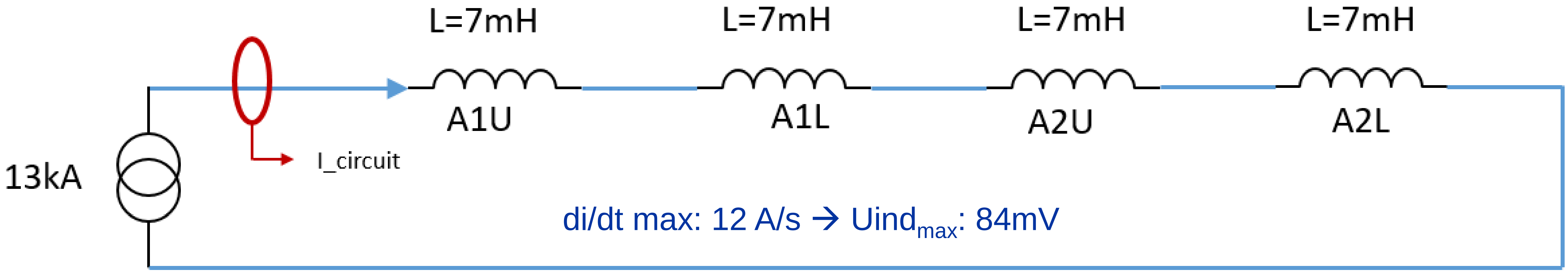
Absolute voltage threshold

- **Pro**
- Simple
- Robust
- Inexpensive current monitoring
- **Con**
- Threshold needs to be lifted during PC start up at low current < $I_{min\ op}$
- Minimum threshold per pole ca 200mV

L * di/dt Algorithm

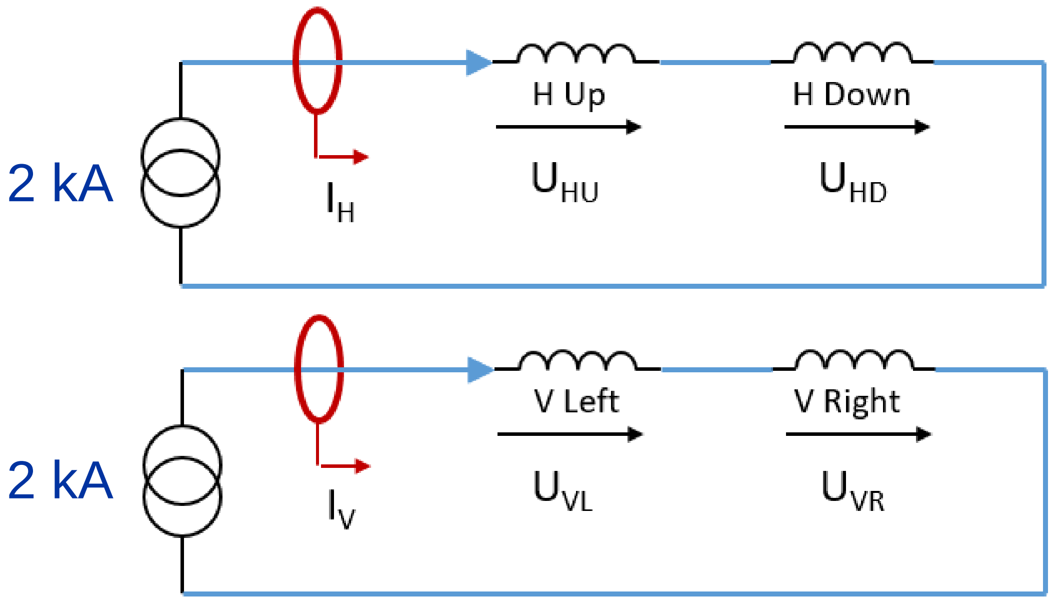
- **Pro**
- Lower thresholds achievable
- **Con**
- DCCT-based current measurement required to achieve thresholds < 200mV
- 13kA DCCT would be expensive 20…50k
- Algorithm very sensitive to smoothness of current

D2 symmetric quench detection



- **For the unlikely case that both apertures quench a total voltage threshold per coil could be used**
- **Absolute coil threshold of ~ 120 mV could be realistic**
- **Current measurement to detect low current regime required**
- **For asymmetric quenches, std. coil comparison algo.**

MCBXF(A/B)



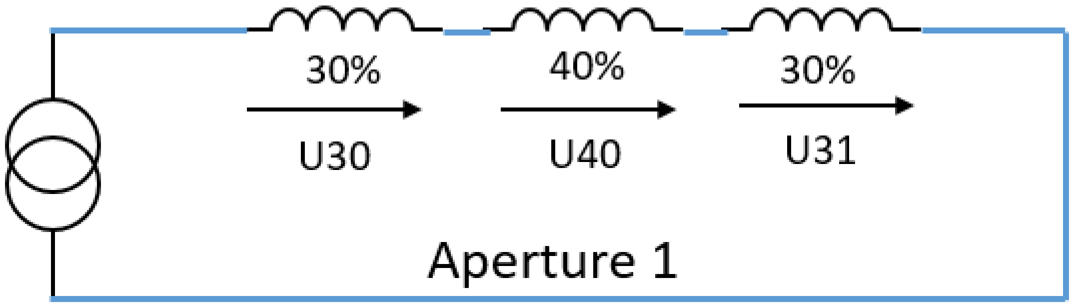
di/dt_{max}: 15 A/s
Lcircuit: 58mH .. 232 mH
$Uind_{max}$: 870 .. 3480 mV

$Ures = (U_{HU} + U_{HD}) – (L^* di/dt)$

- **Inductance is too large for an absolute voltage based algorithm**
- **L*di/dt based algorithm to detect symmetric quenches**
- **Current measurement by DCCT on ¼ of current**
- **QD scheme tested in SM18**

MCBRD

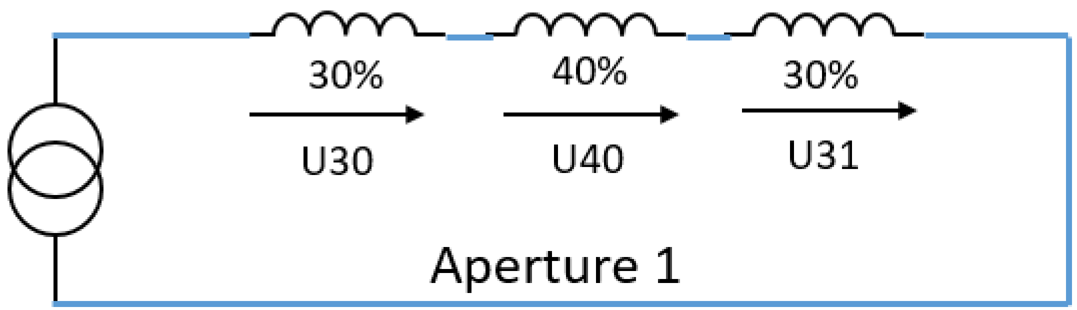
I_{nom} = 394 A



$L_{circuit}$ = 920 mH

- **Due to construction, magnet tends do quench symmetrically**
- **Asymmetric split of coil voltages (voltage taps at: 30% and 70% of inductance)**
- **Hybrid QD algorithm, detects symmetric and asymmetric quenches with single threshold**
- **Due to high inductance L*di/dt compensation algorithm difficult**

MCBRD



Ures = 3/2 * U40 – (U30 + U31)

Quenching element voltage	Effective threshold	Effective threshold (T= 50mV)
U30, U31	T	50 mV
U40	T / 1.5	33 mV
U30 & U31	T / 2	25 mV
U30 & U40	T * 2	100 mV
U31 & U40	T * 2	100 mV
U31 & U40 & U31	T * 2	100 mV

- **Hybrid algorithm for asymmetric and symmetric quenches**
- **Comparison algorithm with scaling allows to detect symmetric quenches as resistive voltage doesn’t scale the same way as inductive voltage**
- **Effective thresholds depend on number and location of quenching elements**
- **Scheme tested in SM18**

Summary of symmetric quench detection methods

Circuit	Current	QD algorithm	comment
Q1, Q2, Q3	18 kA	Coil comparison across magnets	Only one magnet half quenches in a symmetric way at the same time
MCBXFA/B	2 kA	L*di/*dt inductive compensation	Algorithm always work, beware of discontinouites in current
MQSXF	120 A	L*di/dt inductive compensation	“ ”
D1	13 kA	Absolute voltage threshold	Simple and robust
D2	13 kA	Absolute voltage threshold	Simple and robust
MCBRD	2 kA	Coil comparison with scaling	Robust

Conclusion

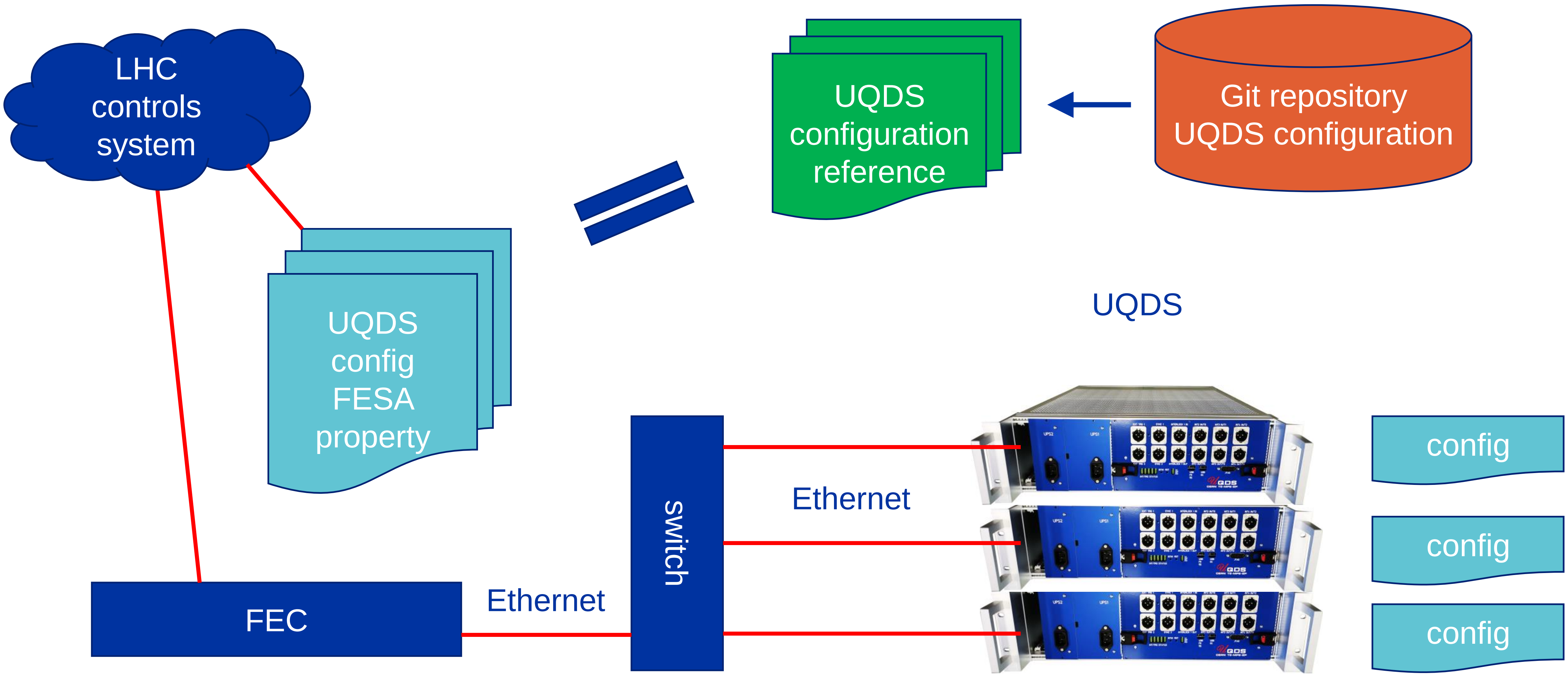
- **Symmetric quench detection algorithms defined for all HL-LHC magnets**
- **Design choice for D1 & D2 to be decided**
- **Most of the concepts already tested on the respective magnet prototypes on the test benches**

QDS configuration management

Configuration management

- **Digital quench detectors can be remotely configured (in limits)**
- **Remotely changeable thresholds and filters have been very useful in the past**
- **Configurable parameters require supervision to prevent errorneous settings**
- **HL-LHC QD controls system is designed with configuration management in mind**
- **Configuration management allows:**
  - Continious supervision of critical parameters
  - Re-configuration of hardware after intervention
  - Controlled modification of parameters due to protected repository
  - Tracking of changes via Git history

Configuration management – Architecture



Configuration management – layered approach

- Checksum inside UQDS register file (column parity) ensures integrity on low level (wrong values open interlock)
- Periodic transmission of register file through controls system and exposure as FESA property
- Periodic comparison of FESA property with reference from repository
- FESA property can also be pushed down to UQDS crate in case of new configuration or hardware exchange
- Changes to configuration initiated on repository level only → full traceability and safety
- Configuration tables are stored as human-readable text files for full traceability

Conclusion

- **Low level, checksum-based integrity check inside FPGA protects against bit-flips and corruption**
- **Full exposure of configuration allows to run permanent software based checkers which detect non-conformal configuration**
- **Storage of configuration in Git repository adds traceability and full control about configuration**
- **System to be tested peu-a-peu on test benches and then IT string**

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