DAQ systems for WP7

Tomasz Podzorny
On behalf of the TE-MPE EDAQ team

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Contents

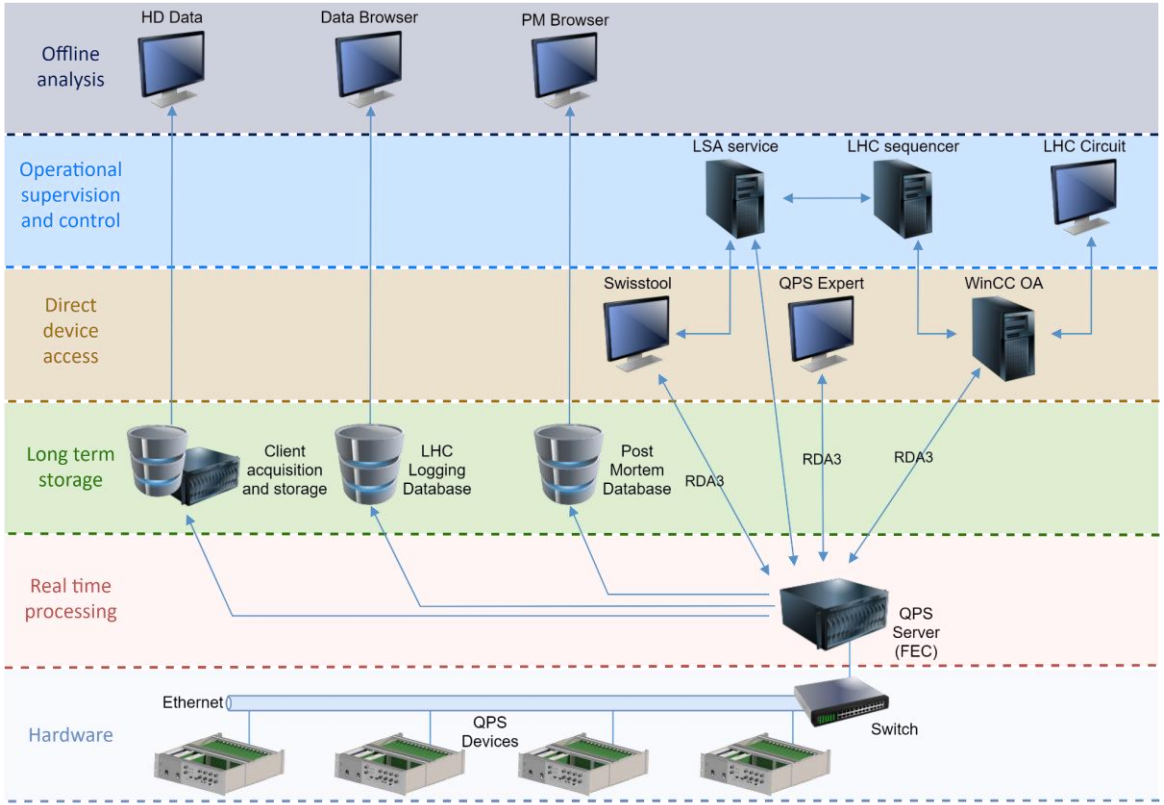
HL-LHC quench protection system

- UQDS based systems are the baseline for quench detection
  - Highly configurable with extensive processing capabilities
  - **High definition data available**
- **Only QDS enables detailed analyses of effects occurring in superconducting circuits**
  - SM18 tests have demonstrated that protection of Nb_3Sn magnets is demanding
  - Powering of HL-LHC circuits is expected to be non-trivial
  - Efficient commissioning and operation will require high quality data
- **Data acquisition is a key to reliable and smooth operation**
  - High quality data is mandatory for automatic analysis of events
- DAQ design considerably benefits from HL-LHC radiation shielded areas

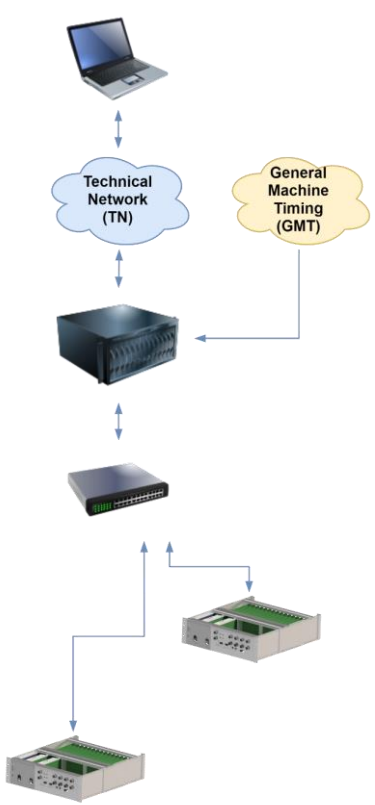
Requirements for QPS data acquisition

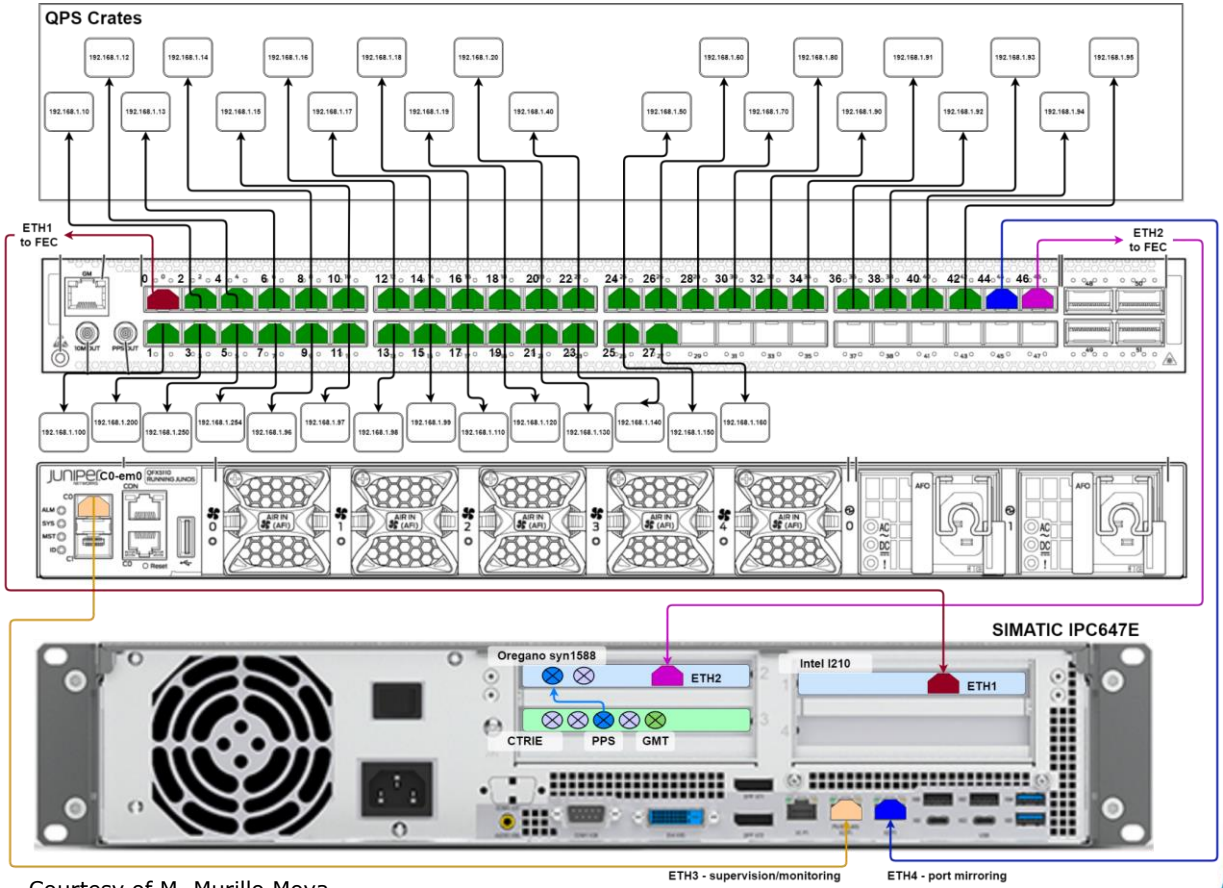
- High data bandwidth: 1-20 Mbps per node
- Number of nodes per network segment: up to 40
- High accuracy timestamping: ≤1 us
- Decoupled hardware from the controls infrastructure
  - Eases hardware and software upgrades
  - Guarantees long-term obsolescence management
- Low to moderate complexity
  - Lightweight communication stack
  - Portability between hardware platforms
- Industrially accepted solutions
  - Key for flexibility and scalability and eases maintenance and training experts
  - Reduces risk of accumulation of the technical debt

QPS system architecture



DAQ infrastructure configuration

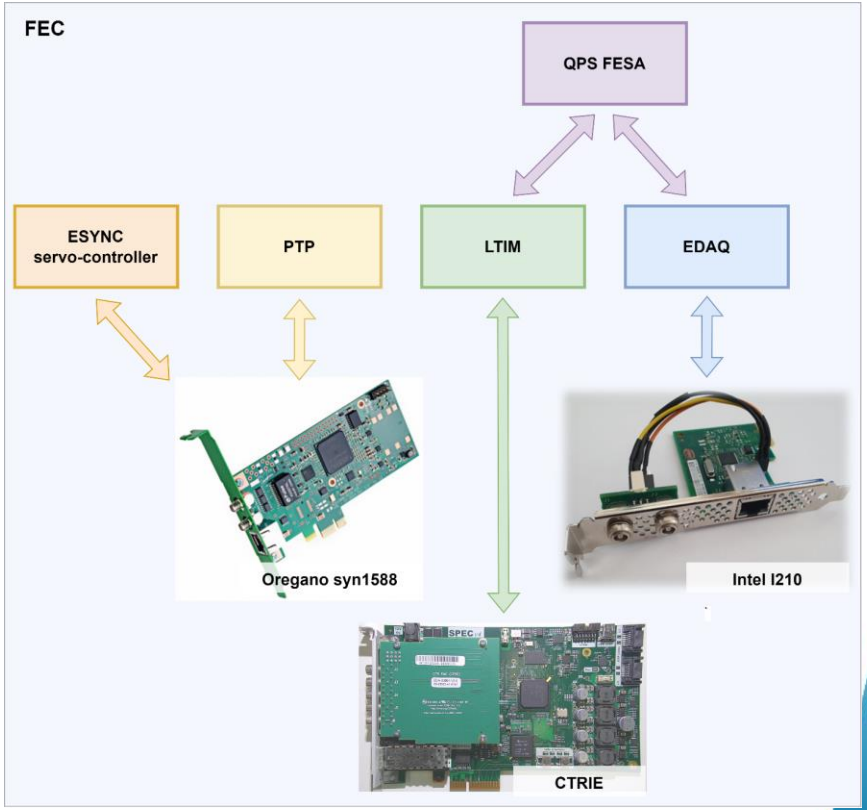




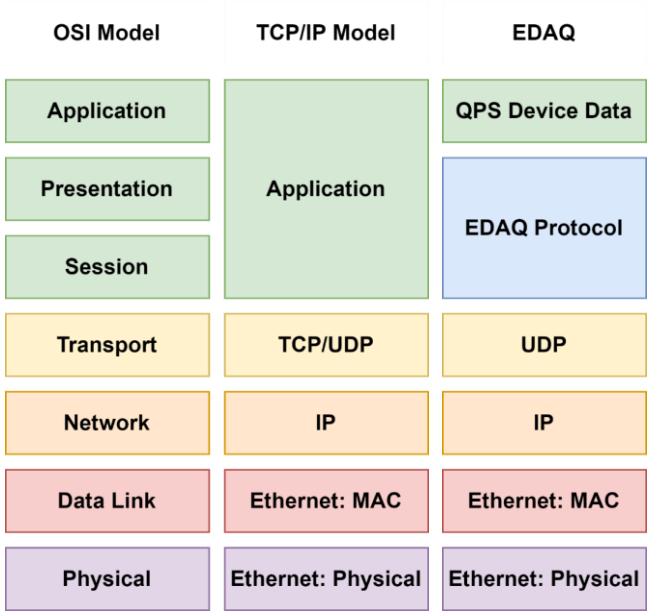
Courtesy of M. Murillo Moya

Front-end computer configuration

- Hardware
  - NIC#1: Intel I210
  - NIC#2: Oregano Systems syn1588 PCIe
  - CTRIE: CERN GMT receiver
- Configuration
  - Static IPs and constrained packet routing
  - Specific buffer sizes for Ethernet sockets
- Synchronisation services
  - PTP server
  - LTIM with custom configuration
  - CTRIE to NIC#2 servo-controller
- DAQ services
  - Communication server – EDAQ driver
  - FESA controls application – DQAmEth

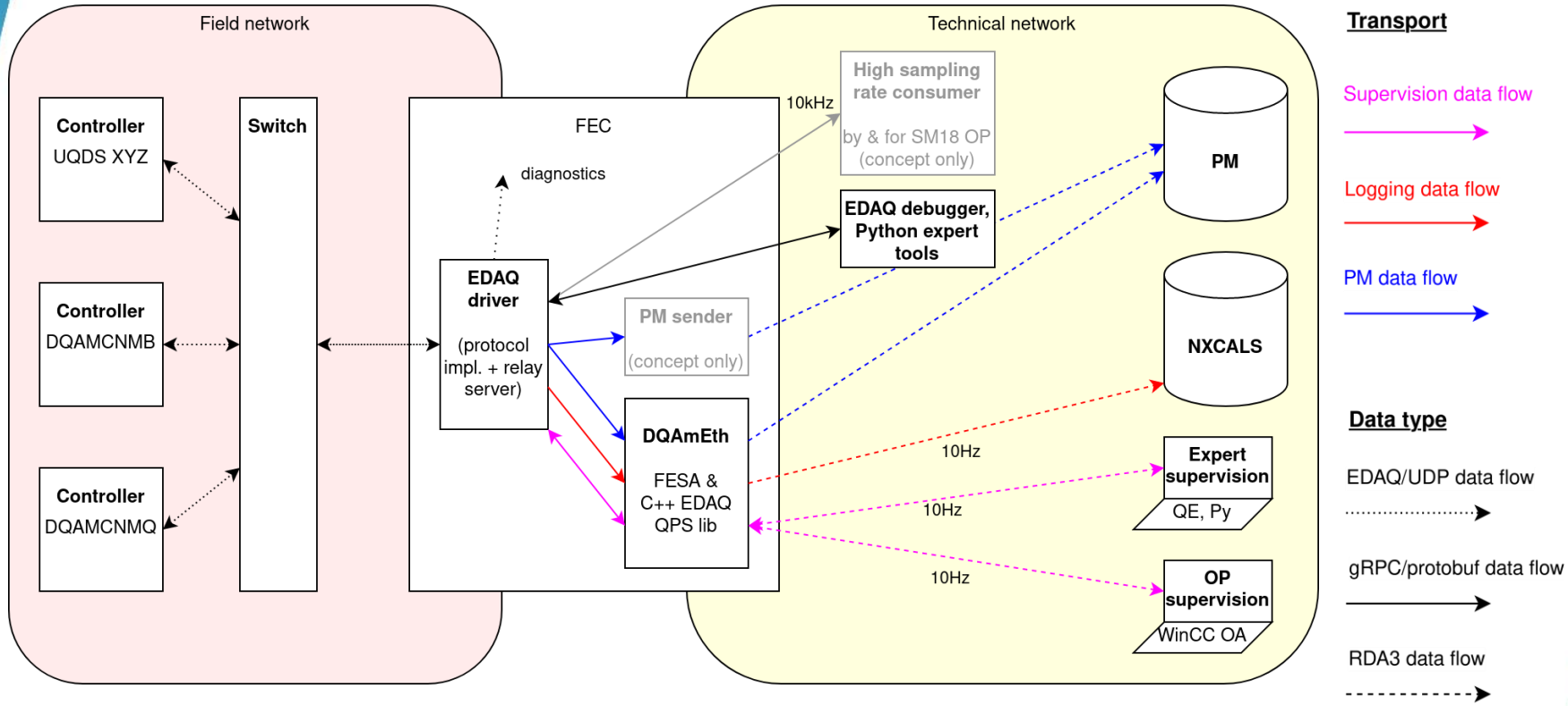


EDAQ communication protocol



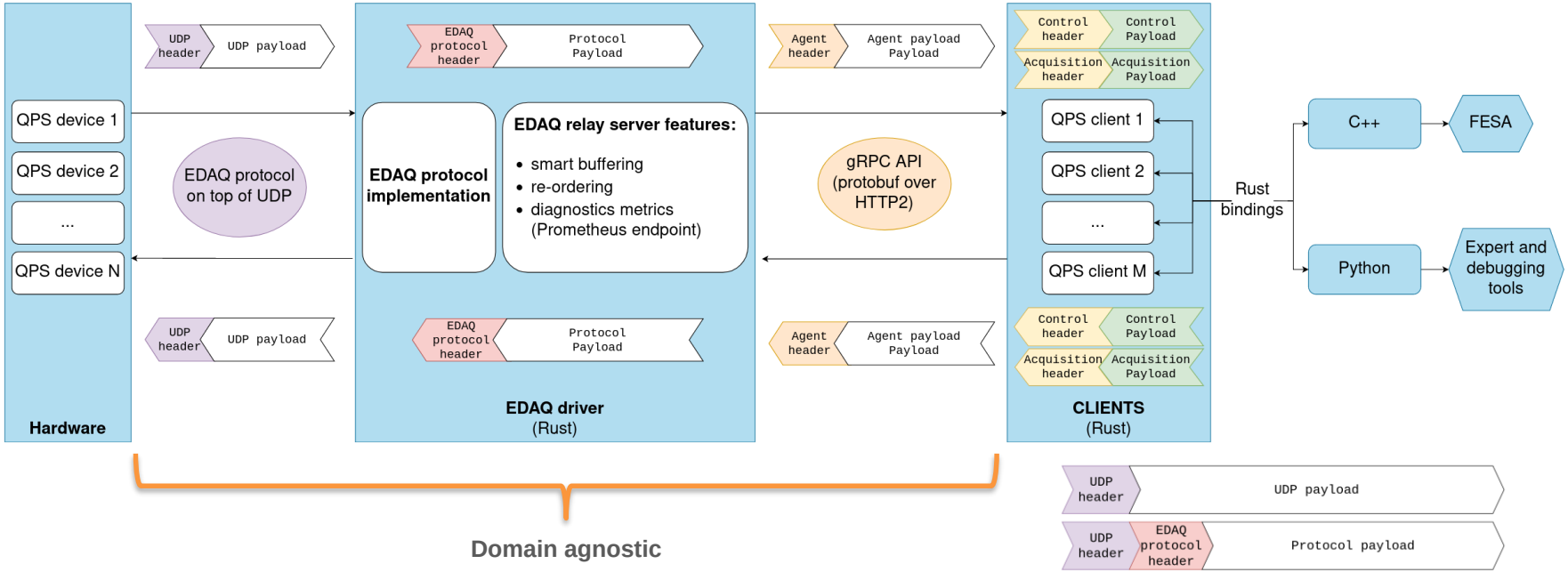
- Protocol uses UDP for transport
  - Limited buffering available on devices' side
  - Lighter implementation with facilitated porting
- Protocol without time constraints
  - Data emission initiated by both server and client
  - Deterministic transactions enable real time control
- Protocol implements:
  - Buffering on the server side
  - Transactions with different delivery guarantees
  - Data ordering, loss detection and retransmission
  - Data corruption detection
- Strict layered architecture
  - Protocol is application agnostic
  - Facilitated definition of devices types

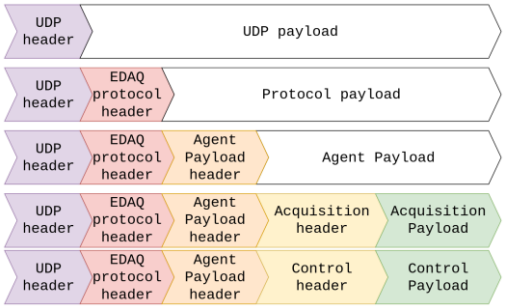
QPS DAQ stack overview



Courtesy of M-A Galilee and MPE-CB

Dataflow diagram





Courtesy of L. Rayon and MPE-CB

QPS Ethernet hardware

- **Reference design**
- Microcontroller based
  - Performant Cortex M4F architecture
  - Rich peripheral set, and large FLASH and RAM memories
  - 100 Mbps Ethernet with HW PTP timestamping
  - Full speed USB (12 Mbps)
  - SPI or QSPI internal communication interface
- TCXO oscillator
- Adaptable and modular bare metal firmware
  - Implements PTP and EDAQ modules
  - Controls local time for accurate timestamping
  - Implements data acquisition and device specific control
- **Data throughput up to 22 Mbps**
- **Continuous logging rate up to 10 kHz**

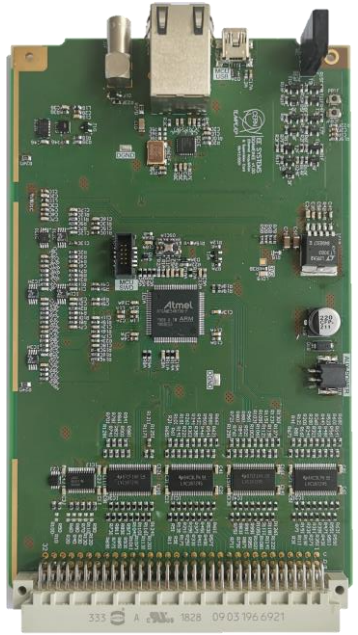
Communication cards

Reference DAQ card

- UQDS 2.0 and generic use cases
- Integration very advanced
  - Development methodology and toolchain is fully established
  - Core firmware modules developed
  - Stable data acquisition and control processes

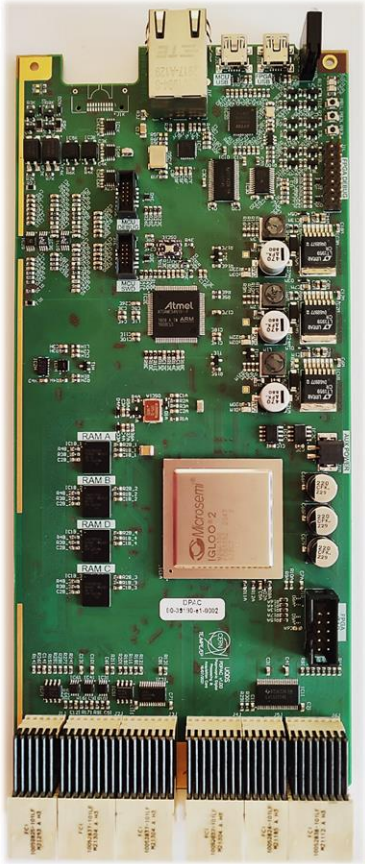
HL-LHC Energy Extraction systems

- Rapid design cycle
- Card partially validated
- Features
  - Core functionality as the reference card
  - Analog: 5 inputs
  - Digital: 56 inputs and 5 command outputs



DSP and communication card

- Applications
  - UQDS 3.0 versatile digital platform
  - PDSU main processing unit
  - CLIQ data acquisition and control unit
- Identical microcontroller subsystem as the reference card
  - Shared development methodology, modules and toolchain
- Slight evolution of UQDS FPGA subsystem
  - High performance and DSP optimized IGLOO2
  - 32 MB RAM memory
  - 288 general purpose IO ports
  - Shared development methodology, modules and toolchain
- Features
  - **Streamlined development for high performance applications**
  - **Compact crate layout and superb design flexibility**



Software benchmarks

EDAQ driver stress-testing

Objective

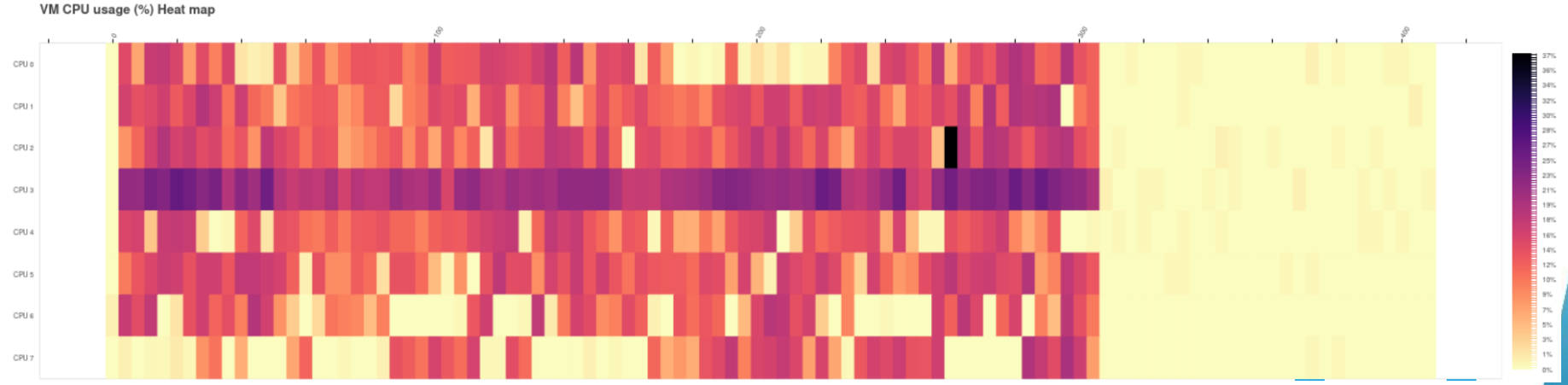
Monitor the driver process with varying workloads from simulated devices.

Test Conditions

- 4 simulated devices
- **20kHz** sampling rate
- **1 Gbps total throughput**

Monitored metrics

- CPU utilization
- Memory consumption
- Dropped messages



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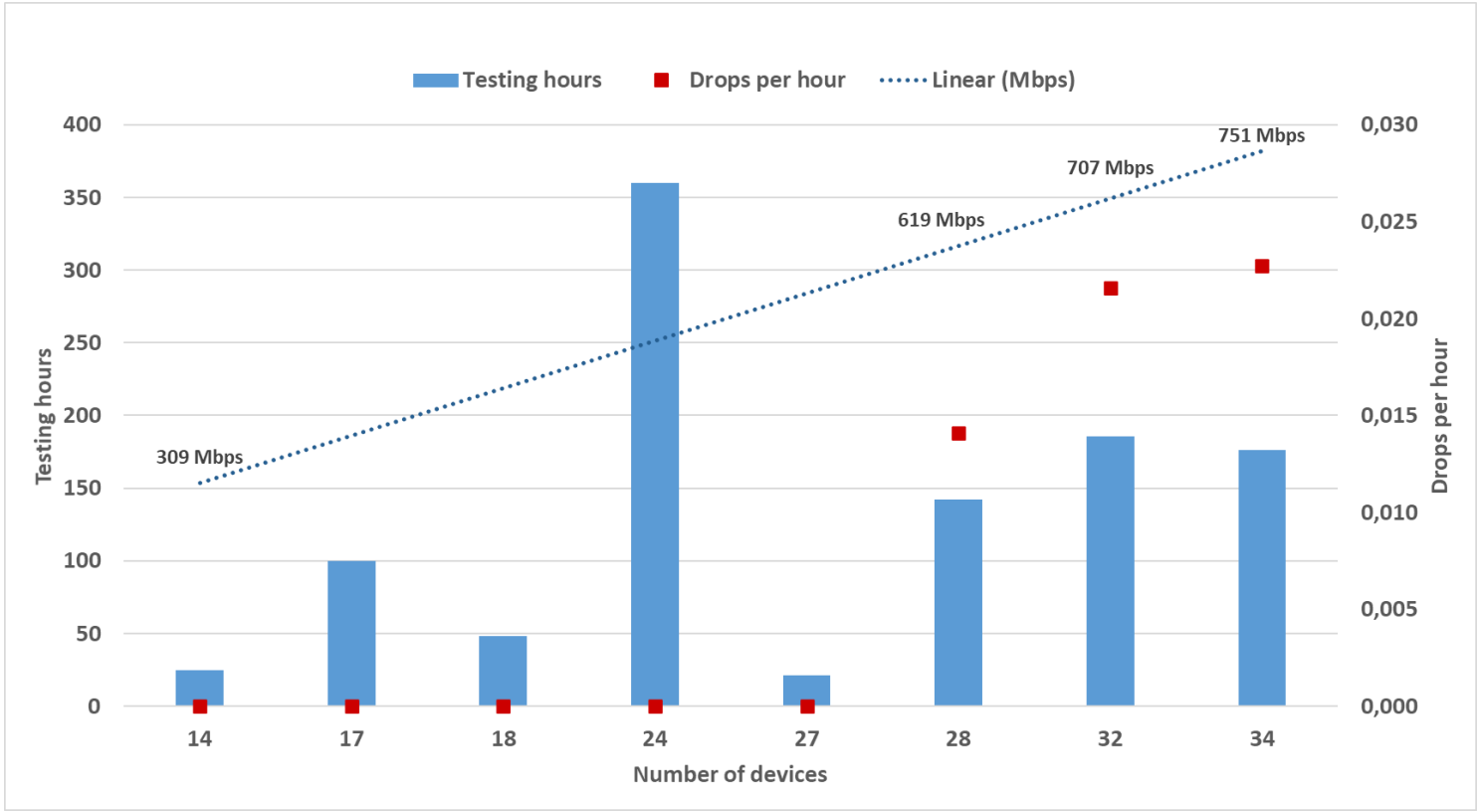
Data throughput and scalability



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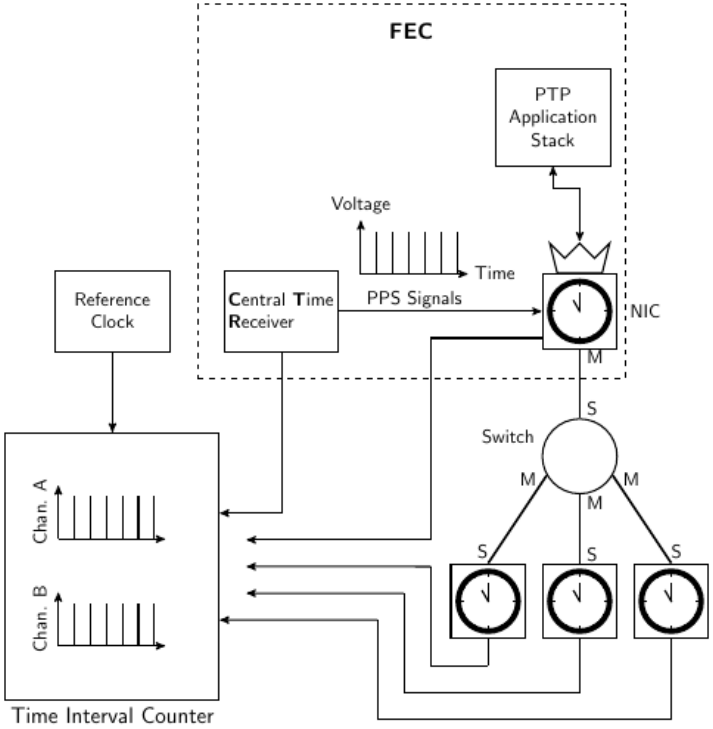
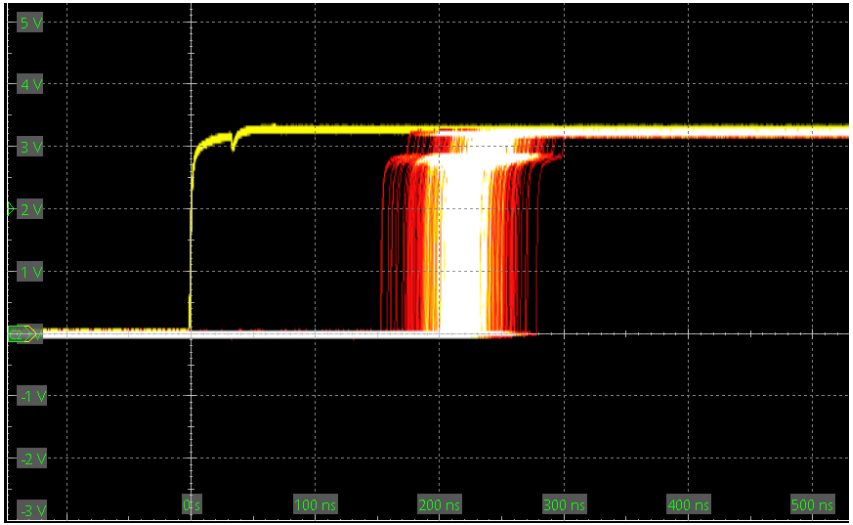
Synchronization performance

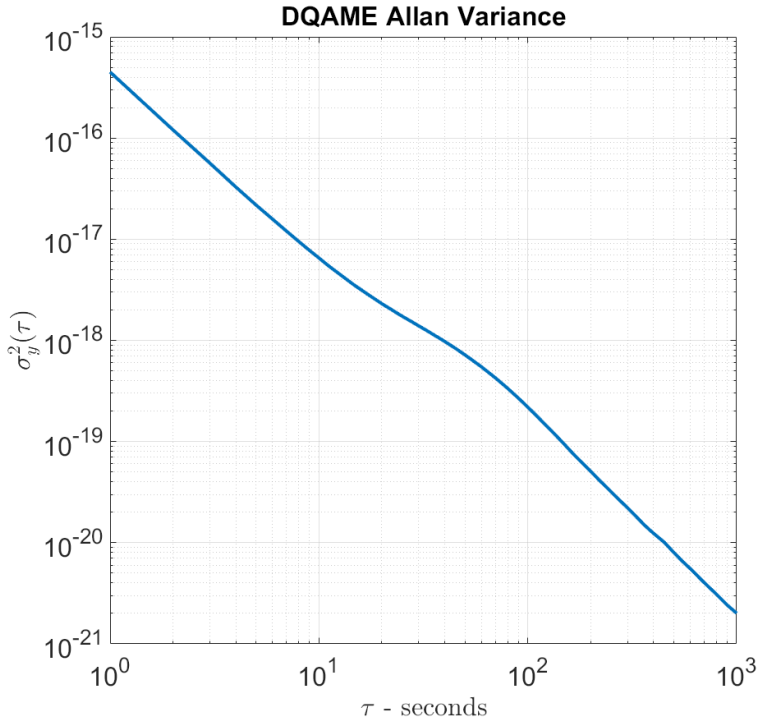


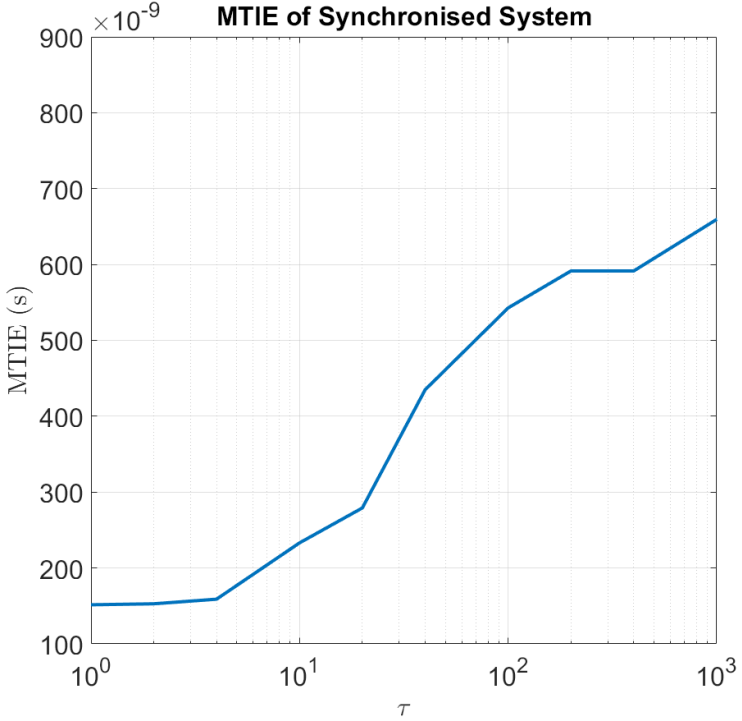
Synchronized PPS output stability



Courtesy of M. Christensen and M. Murillo Moya

Synchronization performance





Courtesy of M. Christensen and M. Murillo Moya

Summary

- Great interest in high data throughput for QPS
  - **High quality data is mandatory for automatic analyses of events**
  - **Ethernet will be the baseline for developments underway**
- Reference hardware design validated
  - Firmware development methodology and toolchain established
  - Core functional modules stable and operational
- Selected communication architecture tested
  - Configuration of the system and communication protocol specified
- Low level software stack operational and mature
  - Stable firmware and EDAQ driver, QPS clients library and C++/ Python bindings
- **All required technologies validated and available**
  - Requirements are fulfilled
  - Standard solutions throughout the entire operational stack

Thank you!

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